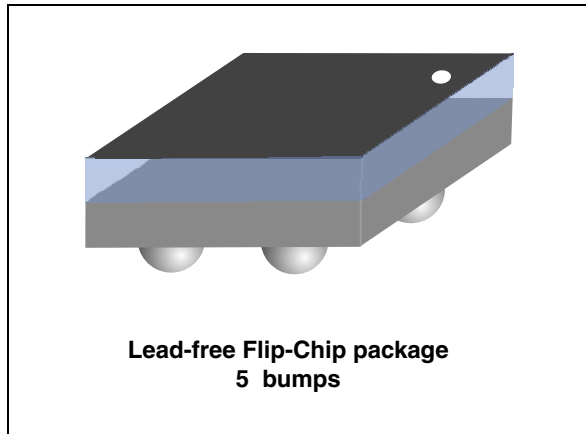


50 Ω nominal input / conjugate match balun to CW1250/CW1260/CW1150/CW1160, with integrated harmonic filter



Datasheet – production data

Features

- 50 Ω nominal input / match ST-Ericsson RF IC CW1250, CW1150, CW1260, CW1160
- Low insertion loss
- Low amplitude imbalance
- Low phase imbalance
- DC blocking access on single RF input
- Small footprint: < 1.2 mm²

Benefits

- Extremely low profile (< 550 μ m after reflow)
- Integrate matching network
- High RF performance
- RF components count and area reduction

Applications

- Balun with integrated matching for ST-Ericsson RF IC CW1250, C1150, CW1260

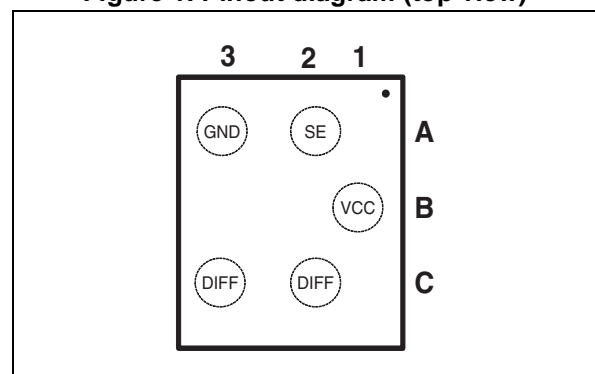
Description

STMicroelectronics BAL-CW1250D3 is a balun (balanced/unbalanced device) designed to transform a single ended signal to differential signals in WLAN application.

This BAL-CW1250D3, with low insertion losses in the bandwidth 2400 MHz to 2500 MHz, has been customized for CW1250, CW1150, CW1260, CW1160 transceiver. The differential output embeds an integrated matching network adapted to the transceiver.

The BAL-CW1250D3 has been designed using STMicroelectronics IPD (integrated passive device) technology on non-conductive glass substrate to optimize RF performance.

Figure 1. Pinout diagram (top view)



1 Characteristics

Table 1. Absolute maximum ratings (limiting values)

| Symbol | Parameter | Value | | | Unit |
|-----------|--|------------|-----|-----|-------------|
| | | Min | Typ | Max | |
| P_{IN} | Average power RF_{IN} | | | 24 | dBm |
| V_{ESD} | ESD ratings MIL STD883C (HBM: C = 100 pF, R = 1.5 k Ω , air discharge) | 2000 | | | V |
| | ESD ratings charged device model (JESD22-C101-D) | 500 | | | |
| | ESD ratings machine model (MM: C = 200 pF, R = 25 Ω , L = 500 nH) | 200 | | | |
| T_{OP} | Operating temperature | -30 to +85 | | | $^{\circ}C$ |

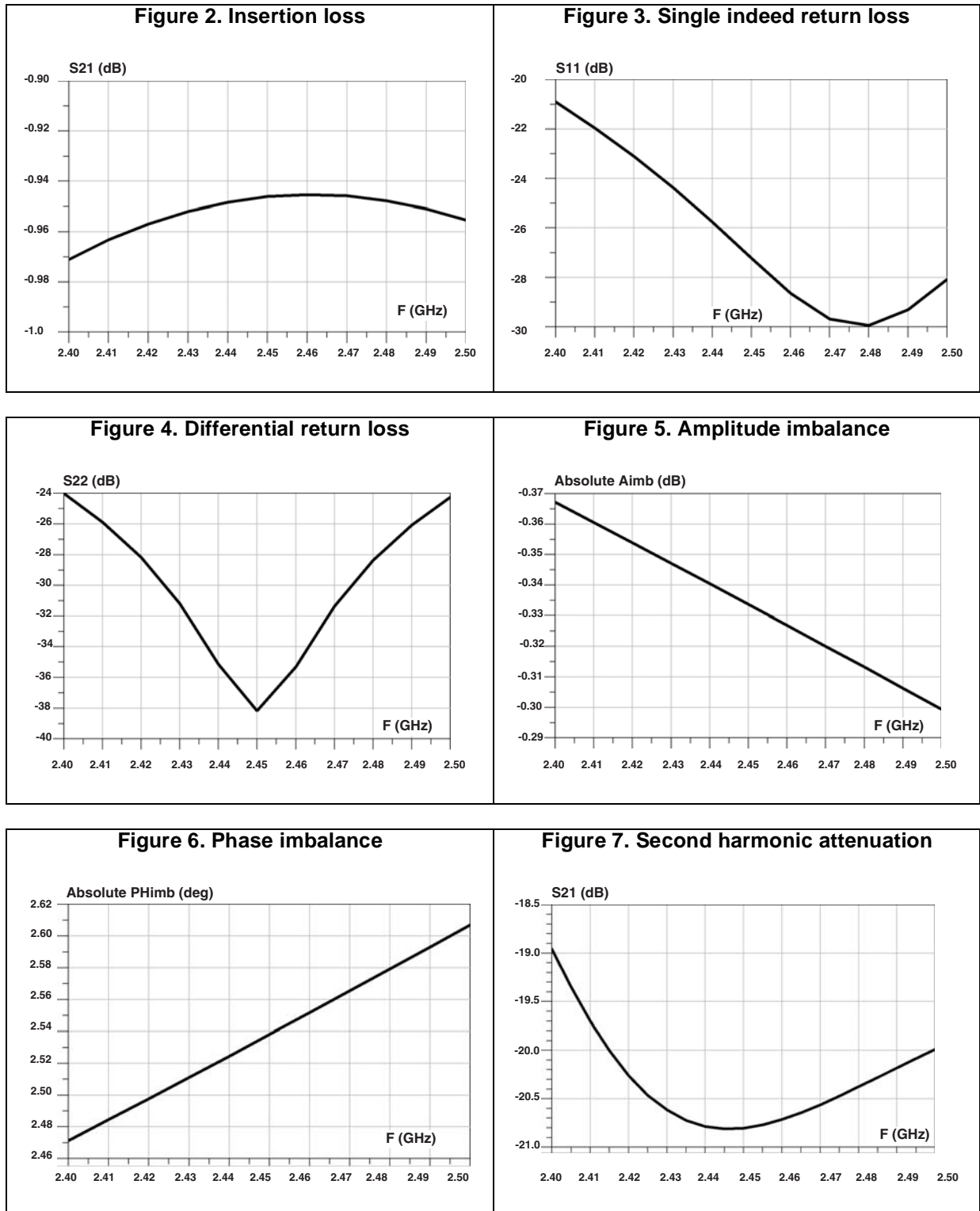
Table 2. Impedances ($T_{amb} = 25^{\circ}C$)

| Symbol | Parameter | Value | | | Unit |
|-----------|---------------------------------------|-------|---------|-----|----------|
| | | Min | Typ | Max | |
| Z_{OUT} | Nominal differential output impedance | | matched | | Ω |
| Z_{IN} | Nominal input impedance | | 50 | | Ω |

Table 3. RF performance ($T_{amb} = 25^{\circ}C$)

| Symbol | Parameter | Value | | | Unit |
|--------------|---------------------------------------|-------|------|------|------------|
| | | Min | Typ | Max | |
| F | Frequency range (bandwidth) | 2400 | | 2500 | MHz |
| IL | Insertion loss in bandwidth | | 0.97 | | dB |
| RL_{SE} | Single ended return loss in bandwidth | | -21 | | dB |
| RL_{DIFF} | Differential return loss in bandwidth | | -24 | | dB |
| ϕ_{imb} | Phase imbalance | -10 | | 10 | $^{\circ}$ |
| Aimb | Amplitude imbalance | -1 | 0.1 | 1 | dB |
| Att_{2f_0} | 2nd harmonic attenuation | | -19 | | dB |

1.1 Measurements



2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 Flip-Chip package information

Figure 8. Flip-Chip package outline

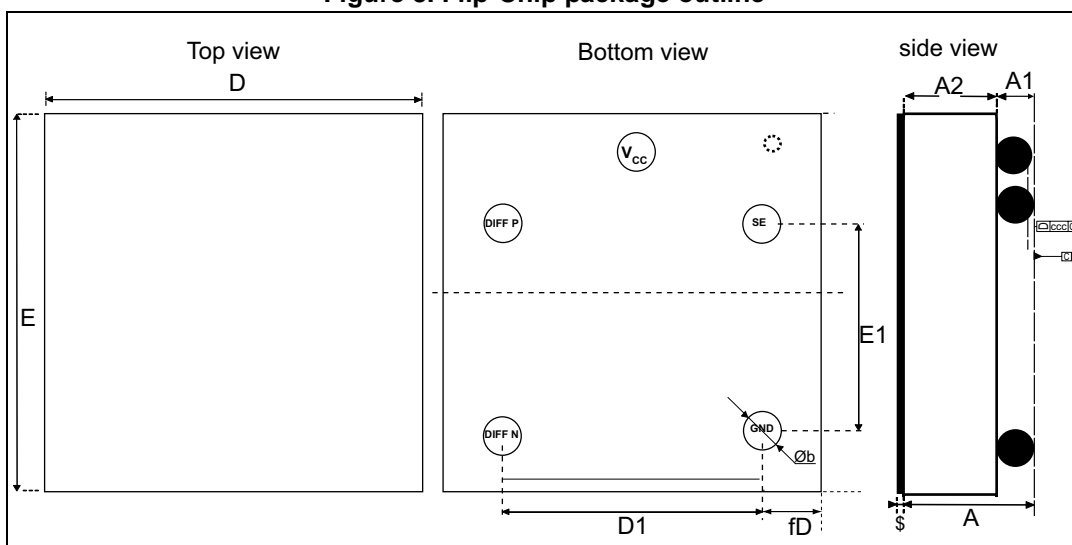


Table 4. Flip-Chip package mechanical data

| Parameter | Description | Min. | Typ. | Max. | Unit |
|-----------|---|-------|-------|-------|------|
| A | Bump height + substrate thickness | 0.570 | 0.630 | 0.690 | mm |
| A1 | Bump height | 0.155 | 0.205 | 0.255 | mm |
| A2 | Substrate thickness | | 0.400 | | mm |
| b | Bump diameter | 0.215 | 0.255 | 0.295 | mm |
| D | Y dimension of the die | 1.150 | 1.200 | 1.250 | mm |
| D1 | Y pitch | | 0.760 | | mm |
| E | X dimension of the die | 0.940 | 0.990 | 1.040 | mm |
| E1 | X pitch | | 0.400 | | mm |
| fD | Distance from bump to edge of die on Y axis | | 0.105 | | mm |
| ccc | | | | 0.05 | mm |
| \$ | | | 0.025 | | mm |

Figure 9. Footprint

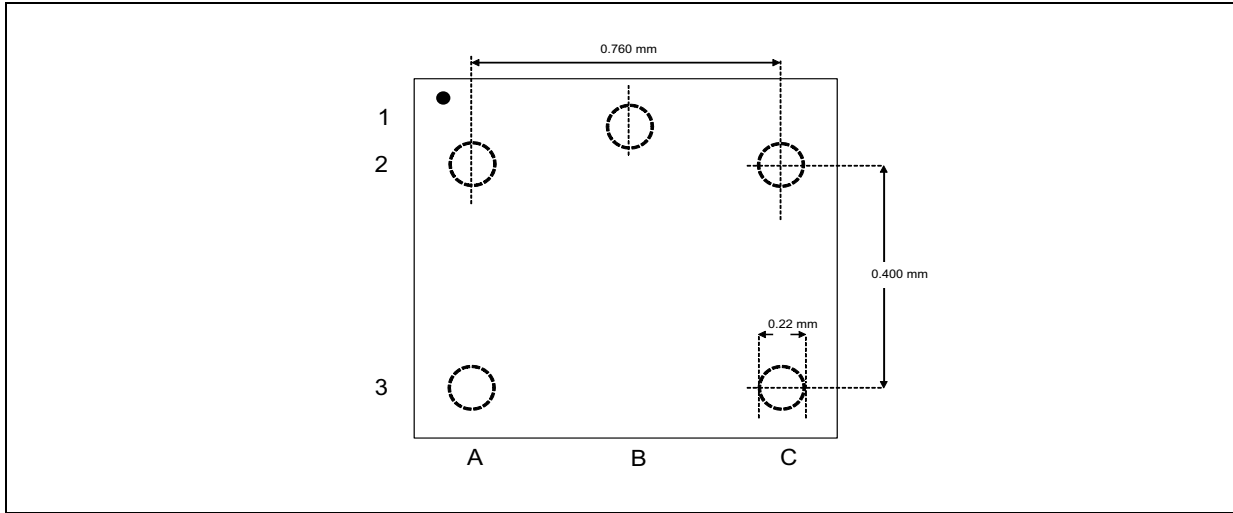


Figure 10. Footprint - 3 mils stencil - non solder mask defined

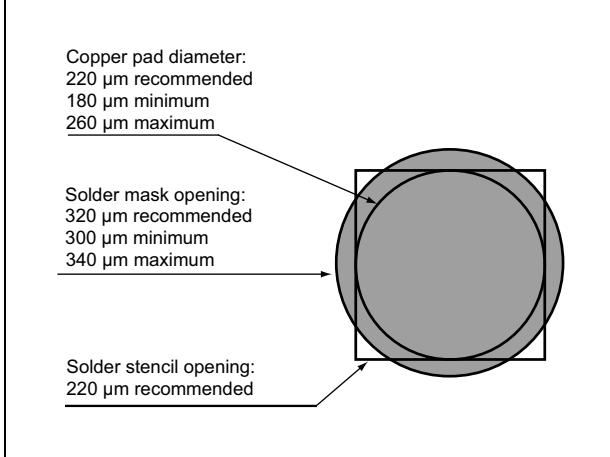


Figure 11. Footprint - 3 mils stencil - solder mask defined

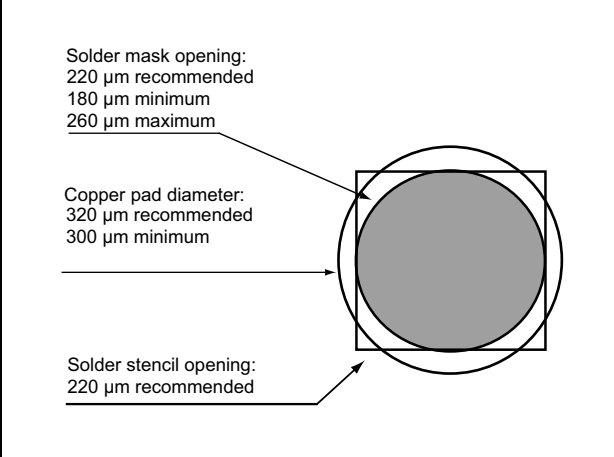


Figure 12. Footprint - 5 mils stencil - non solder mask defined

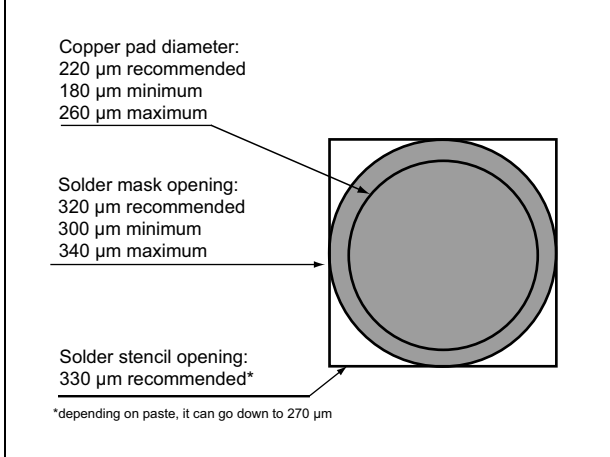


Figure 13. Footprint - 5 mils stencil - solder mask defined

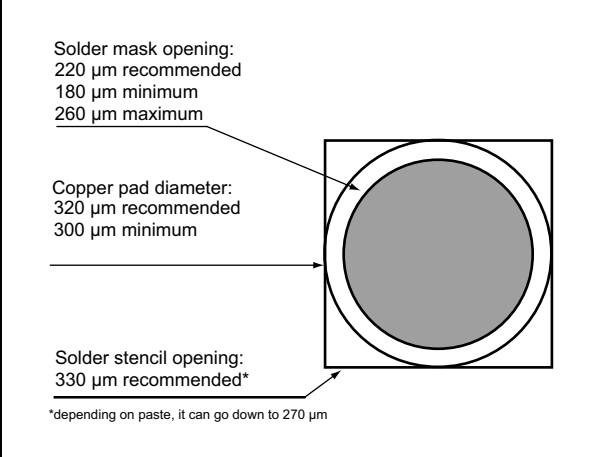


Figure 14. Recommended land pattern (used for balun characterization)

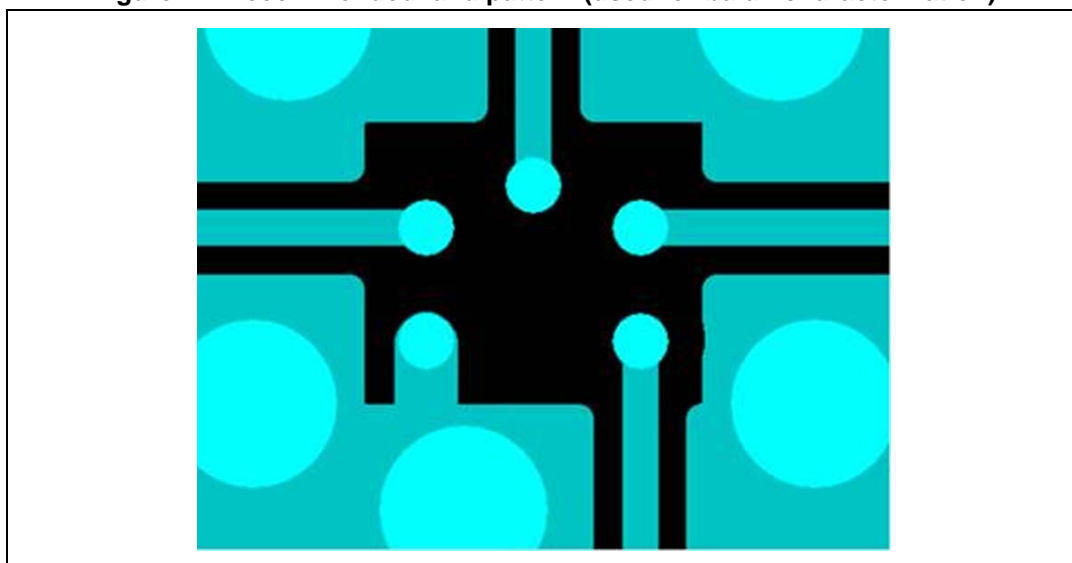


Figure 15. Marking

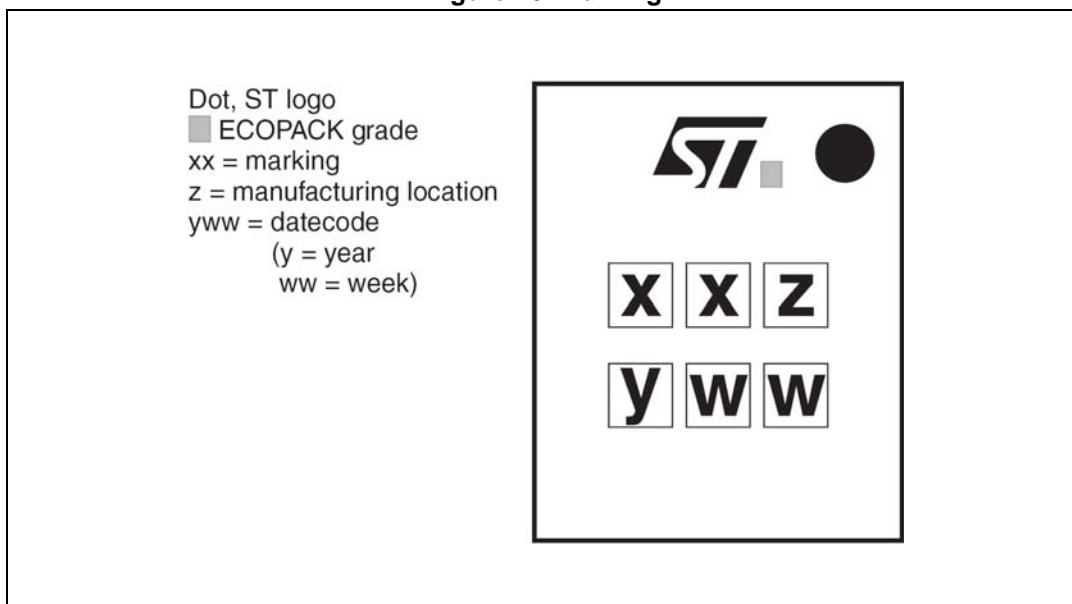
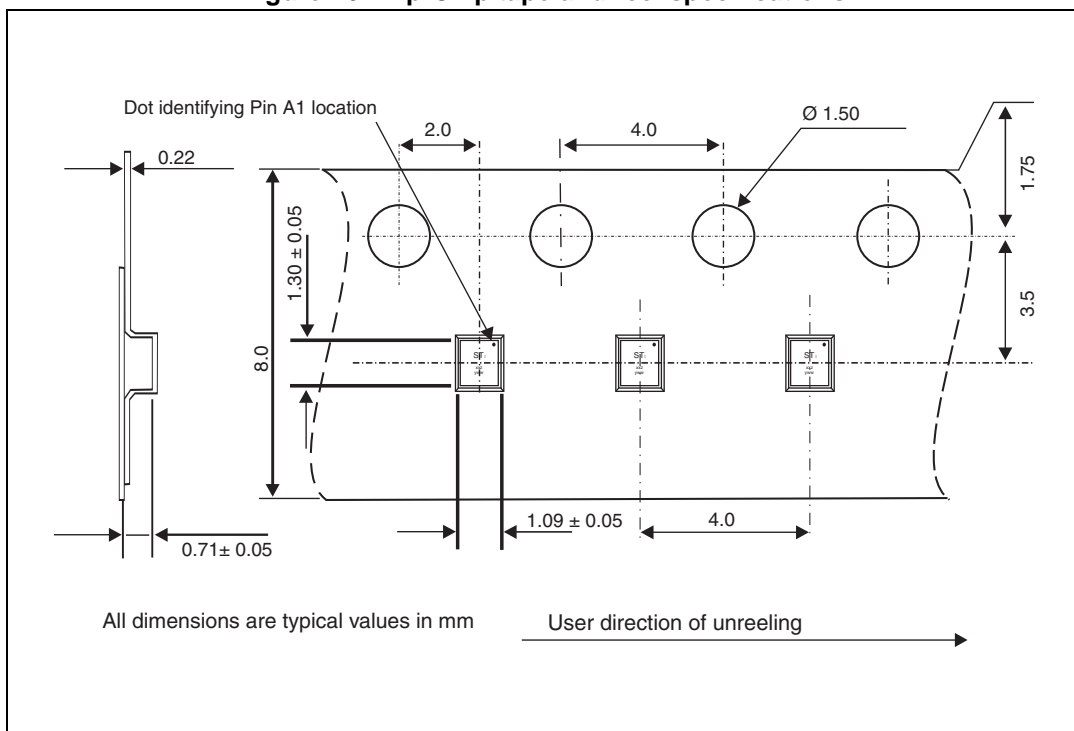


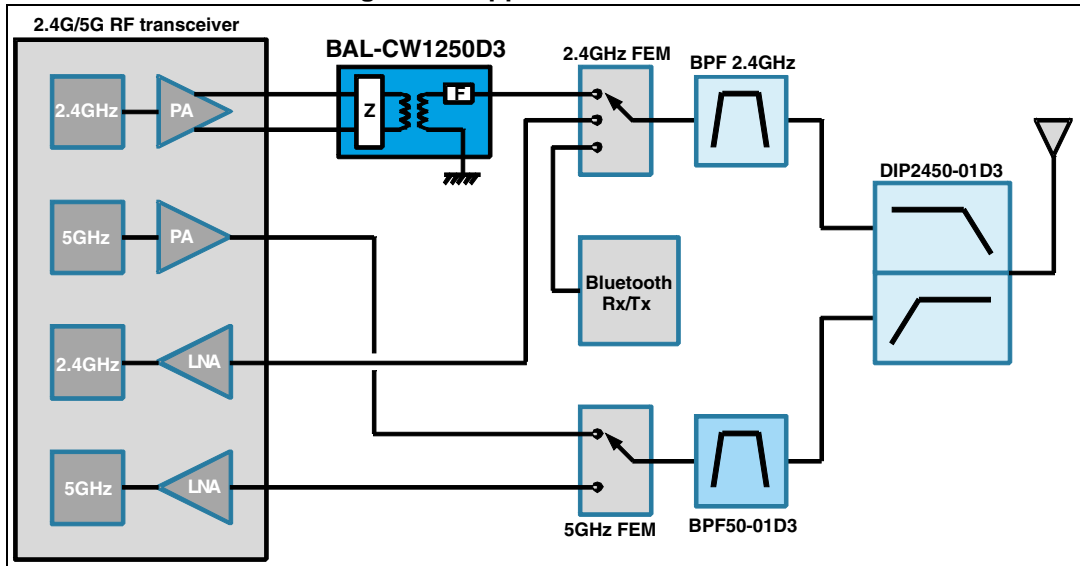
Figure 16. Flip-Chip tape and reel specifications



Note: More information is available in the STMicroelectronics Application note: AN2348 Flip-Chip: "Package description and recommendations for use"

3 Application information

Figure 17. Application schematic



Note: More information is available in the application notes:
 AN2348 Flip-Chip package description and recommendations for use

4 Ordering information

Table 5. Ordering information

| Part Number | Marking | Package | Weight | Base Qty | Delivery Mode |
|--------------|---------|-----------|---------|----------|-------------------|
| BAL-CW1250D3 | SG | Flip-Chip | 1.46 mg | 5000 | Tape and reel(7") |

5 Revision history

Table 6. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 23-May-2013 | 1 | Initial release. |
| 23-Sep-2015 | 2 | Updated Figure 8 . Added Figure 10 , Figure 11 , Figure 12 , Figure 13 and Table 4 . Reformatted to current standards. |

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