3.3V CMOS 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

IDT74ALVCF162835A

FEATURES:

- **0.5 MICRON CMOS Technology**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **V_{CC} = 3.3V ± 0.3V, Normal Range**
- **V_{CC} = 2.7V to 3.6V, Extended Range**
- **V_{CC} = 2.5V ± 0.2V**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-Rail output swing for increased noise margin**
- **Available in TSSOP and TVSOP packages**

DRIVE FEATURES:

- **Balanced Output Drivers: ±18mA**
- **Low switching noise**

APPLICATIONS:

- **SDRAM Modules**
- **PC Motherboards**
- **Workstations**

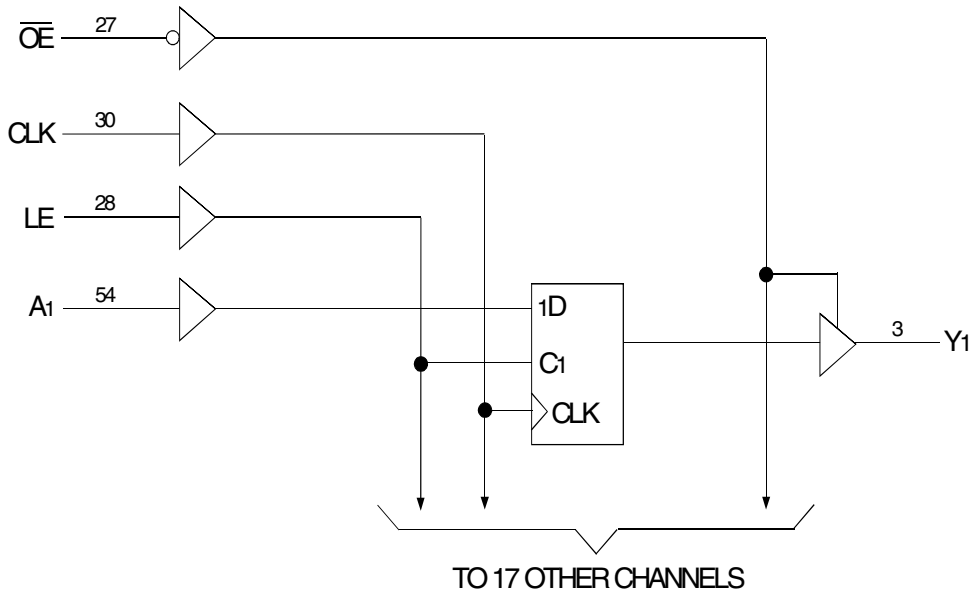
DESCRIPTION:

This 18-bit universal bus driver is built using advanced dual metal CMOS technology. Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

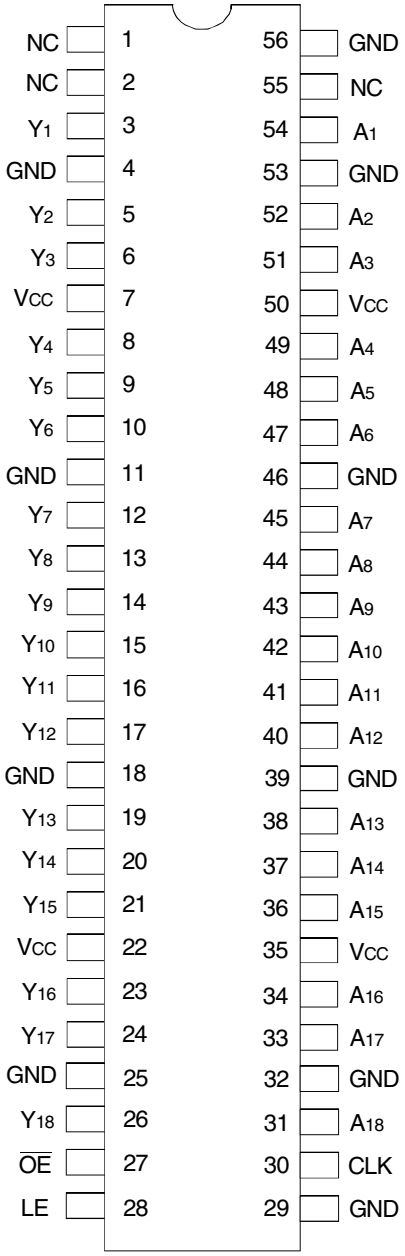
The ALVCF162835A has series resistors in the device output structure which will reduce switching noise in 128MB and 256MB SDRAM modules. Designed with a drive capability of ±18mA, the ALVCF162835A is a mid-way drive between the ALVC162835 (±12mA) and ALVC16835 (±24mA).

The ALVCF162835A is a faster version of the ALVCF162835 or ALVC162835. It is suitable for PC133 applications and particularly SDRAM Modules clocked at 133 MHz.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
CLK	Register Input Clock
LE	Latch Enable (Transparent HIGH)
Ax	Data Inputs
Yx	3-State Outputs

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	±50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4	5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	7	9	pF
C_{OUT}	I/O Port Capacitance	V_{IN} = 0V	—	7	9	pF

NOTE:
1. As applicable to the device type.

FUNCTION TABLE(1)

Inputs				Outputs
$\overline{OE}$	LE	CLK	Ax	Yx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y_0(2)
L	L	L	X	Y_0(3)

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition
2. Output level before indicated steady-state input conditions were established, provided that CLK is HIGH before LE went LOW.
3. Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	±5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	±5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	1.9	—	
			I_{OH} = – 8mA	1.7	—	
		V_{CC} = 2.7V	I_{OH} = – 6mA	2.2	—	
			I_{OH} = – 12mA	2	—	
		V_{CC} = 3V	I_{OH} = – 8mA	2.4	—	
			I_{OH} = – 18mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 8mA	—	0.55	
		V_{CC} = 2.7V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.6	
		V_{CC} = 3V	I_{OL} = 8mA	—	0.55	
			I_{OL} = 18mA	—	0.8	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	Vcc = 2.5V ± 0.2V	Vcc = 3.3V ± 0.3V	Unit
			Typical	Typical	
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	30	35	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		12.5	14	

SWITCHING CHARACTERISTICS(1)

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}		150	—	150	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to Yx	1	4	—	4.6	1	3.5	ns
t_{PLH} t_{PHL}	Propagation Delay LE to Yx	1.3	5.5	—	5.4	1.3	4.6	ns
t_{PLH} t_{PHL}	Propagation Delay CLK to Yx	1.4	5.9	—	5.6	1.4	3.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yx	1.4	5.9	—	6	1.1	5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Yx	1	4.7	—	4.6	1.3	4.2	ns
t_W	Pulse Duration, LE HIGH	3.3	—	3.3	—	3.3	—	ns
t_W	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t_{SU}	Set-up Time, data before CLK↑	1.8	—	1.5	—	1	—	ns
t_{SU}	Set-up Time, data before LE↓, CLK HIGH	1.9	—	1.6	—	1.5	—	ns
t_{SU}	Set-up Time, data before LE↓, CLK LOW	1.3	—	1.1	—	1	—	ns
t_H	Hold Time, data after CLK↑	0.6	—	0.6	—	0.6	—	ns
t_H	Hold Time, data after LE↓, CLK HIGH or LOW	1.4	—	1.7	—	1.4	—	ns
$t_{SK(O)}$	Output Skew(2)	—	—	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

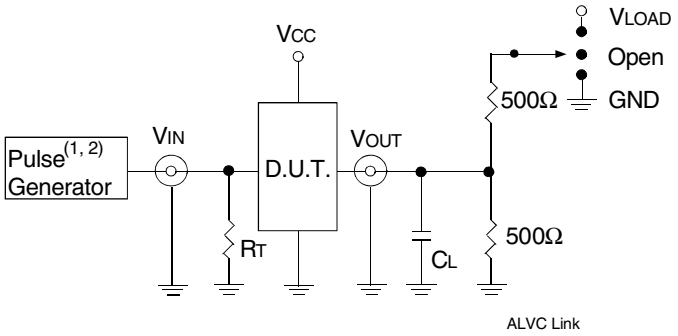
SWITCHING CHARACTERISTICS FROM 0°C TO 65°C, C_L = 50pF

Symbol	Parameter	Vcc = 3.3V ± 0.15V		Unit
		Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay CLK to xYx	1.8	3.5	ns

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V±0.3V	$V_{CC}^{(1)}$= 2.7V	$V_{CC}^{(2)}$= 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



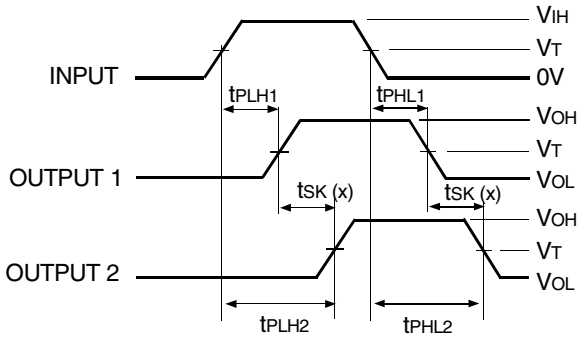
Test Circuit for All Outputs

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2ns; t_R ≤ 2ns.

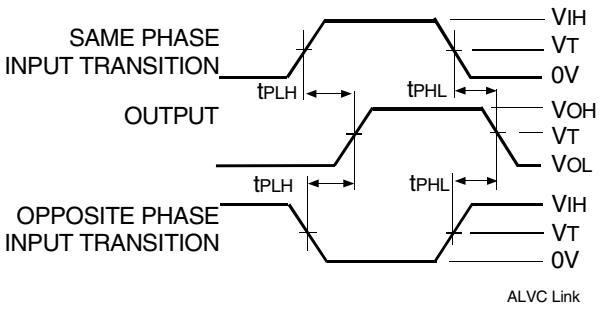
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open

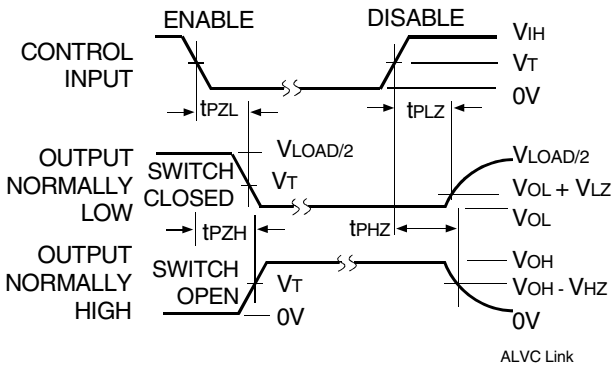


Output Skew - $t_{SK}(x)$

NOTES:
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

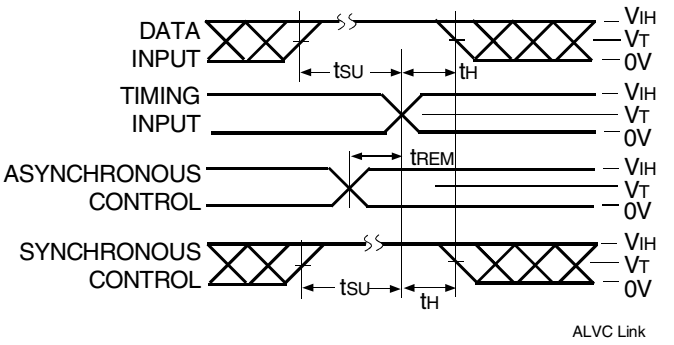


Propagation Delay

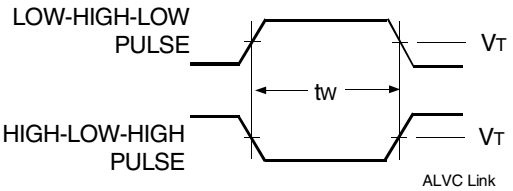


Enable and Disable Times

NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

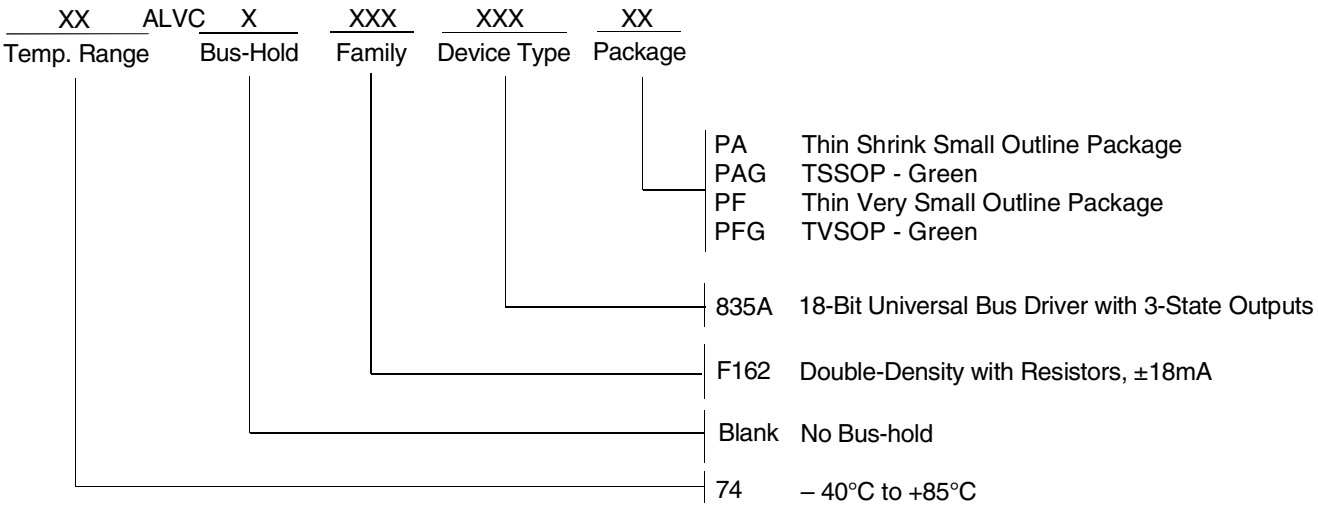


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



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