

NMC27C32B

32,768-Bit (4096 x 8) CMOS EPROM

General Description

The NMC27C32B is a 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C32B is designed to operate with a single +5V power supply with $\pm 10\%$ tolerance.

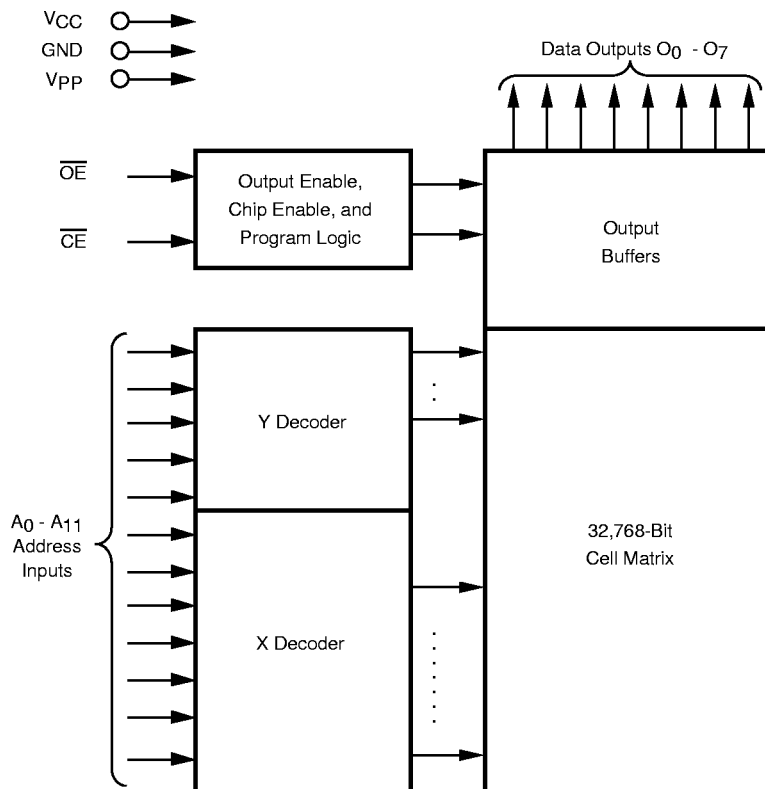
The NMC27C32B is packaged in a 24-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with Fairchild's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

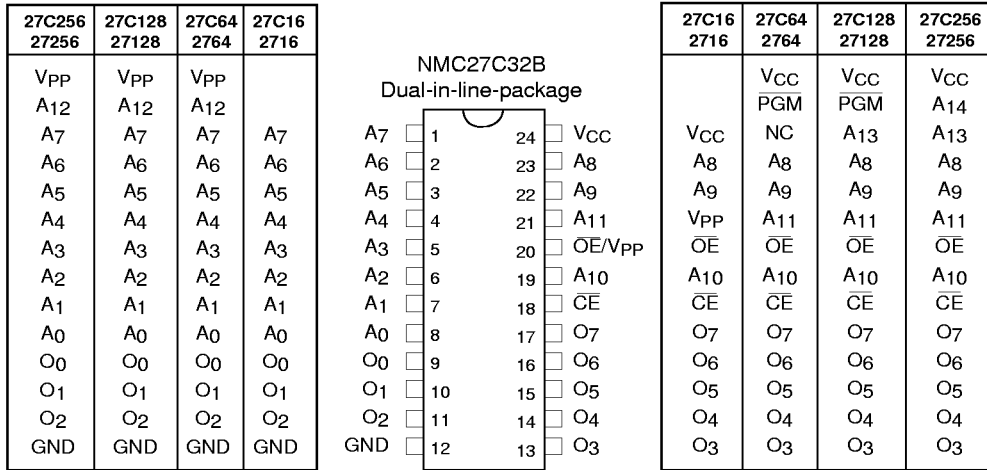
- Low CMOS power consumption
 - Active Power: 55 mW Max
 - Standby Power: 0.55 mW Max
- Industrial temperature range, -40°C to +85°C
- Fast and reliable programming
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming
- High current CMOS level output drivers
- Compatible with NMOS 2732

Block Diagram



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Connection Diagram



Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32B pin.

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Order Number NMC27C32BQ See Package Number J24AQ

Pin Names

A0–A11	Addresses
CE	Chip Enable
OE	Output Enable
V _{PP}	Programming Voltage
O0 –O7	Outputs
V _{CC}	Power Supply
GND	Ground

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQ150	150
NMC27C32BQ200	200

Industrial Temp Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQE200	200

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
V _{CC} Supply Voltage with Respect to Ground	+7.0V to -0.6V
All Input Voltages except A9 and OE/V _{PP} with Respect to Ground (Note 9)	+6.5V to -0.6V
All Output Voltages with Respect to Ground (Note 9)	V _{CC} +1.0V to GND-0.6V

OE/V _{PP} Supply and A9 Voltage with Respect to Ground	+14.0V to -0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 6)

Temperature Range	NMC27C32BQ150, 200	0°C to +70°C
	NMC27C32BQE 200	-40°C to +85°C
V _{CC} Power Supply		+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{LI}	Input Load Current	V _{IN} = V _{CC} or GND		0.01	1	μA
I _{PP}	OE/V _{PP} Load Current	OE/V _{PP} = V _{CC} or GND			10	μA
I _{LO}	Output Leakage Current	V _{OUT} = V _{CC} or GND, CE = V _{IH}		0.01	1	μA
I _{CC1}	V _{CC} Current (Active) TTL Inputs	CE = V _{IL} , f=5 MHz Inputs = V _{IH} or V _{IL} , I/O = 0 mA		5	20	mA
I _{CC2}	V _{CC} Current (Active) CMOS Inputs	CE = GND, f = 5 MHz Inputs = V _{CC} or GND, I/O = 0 mA		3	10	mA
I _{CCSB1}	V _{CC} Current (Standby) TTL Inputs	CE = V _{IH}		0.1	1	mA
I _{CCSB2}	V _{CC} Current (Standby) CMOS Inputs	CE = V _{CC}		0.5	100	μA
V _{IL}	Input Low Voltage		-0.2		0.8	V
V _{IH}	Input High Voltage		2.0		V _{CC} +1	V
V _{OL1}	Output Low Voltage	I _{OL} = 2.1 mA			0.45	V
V _{OH1}	Output High Voltage	I _{OH} = -400 μA	2.4			V
V _{OL2}	Output Low Voltage	I _{OL} = 10 μA			0.1	V
V _{OH2}	Output High Voltage	I _{OH} = -10 μA	V _{CC} - 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32B				Units
			Q150		Q200, QE200		
			Min	Max	Min	Max	
t _{ACC}	Address to Output Delay	CE = OE = V _{IL}		150		200	ns
t _{CE}	CE to Output Delay	OE = V _{IL}		150		200	ns
t _{OE}	OE to Output Delay	CE = V _{IL}		60		60	ns
t _{DF}	OE High to Output Float	CE = V _{IL}	0	50	0	60	ns
t _{CF}	CE High to Output Float	OE = V _{IL}	0	50	0	60	ns
t _{OH}	Output Hold from Addresses, CE or OE, Whichever Occurred First	CE = OE = V	0		0		ns

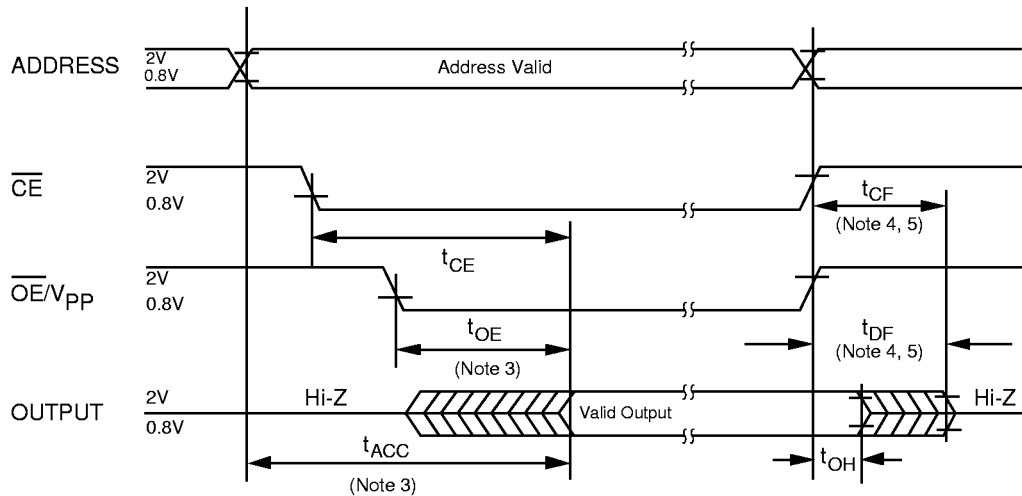
Capacitance (Note 2) $T_A = +25^\circ\text{C}$, $f = 1\text{ MHz}$

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except OE/V _{PP}	$V_{IN} = 0\text{V}$	6	12	pF
C_{IN2}	OE/V _{PP} Input Capacitance	$V_{IN} = 0\text{V}$	16	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100\text{ pF}$ (Note 8)
Input Rise and Fall Times	$\leq 5\text{ ns}$
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 7)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: OE may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of CE without impacting t_{ACC} .

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) - 0.10V;

Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using OE or CE.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0\text{V}$ to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6\text{ mA}$, $I_{OH} = -400\ \mu\text{A}$

C_L : 100 pF includes fixture capacitance.

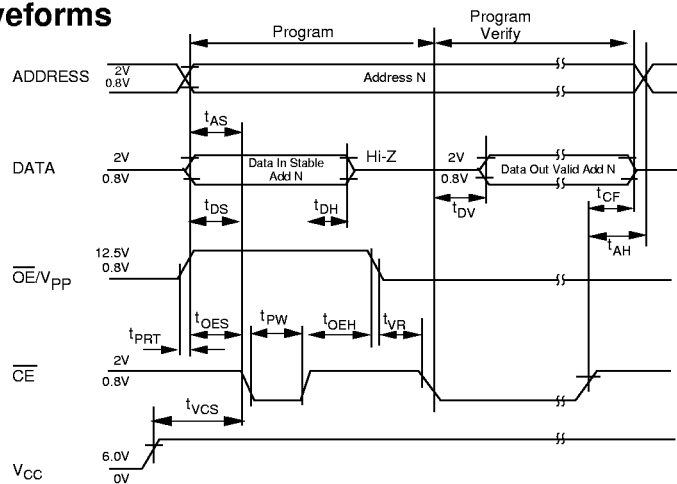
Note 9: Inputs and outputs can undershoot to -2.0V for 20 ns Max, except for OE/V_{PP} which cannot exceed -0.2V.

Note 10: Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages.

Programming Characteristics (Note 11) (Note 12) (Note 13) (Note 14)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	OE Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	OE Hold Time		1			μs
t_{DV}	Data Valid from CE	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	OE Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	$^{\circ}\text{C}$
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms



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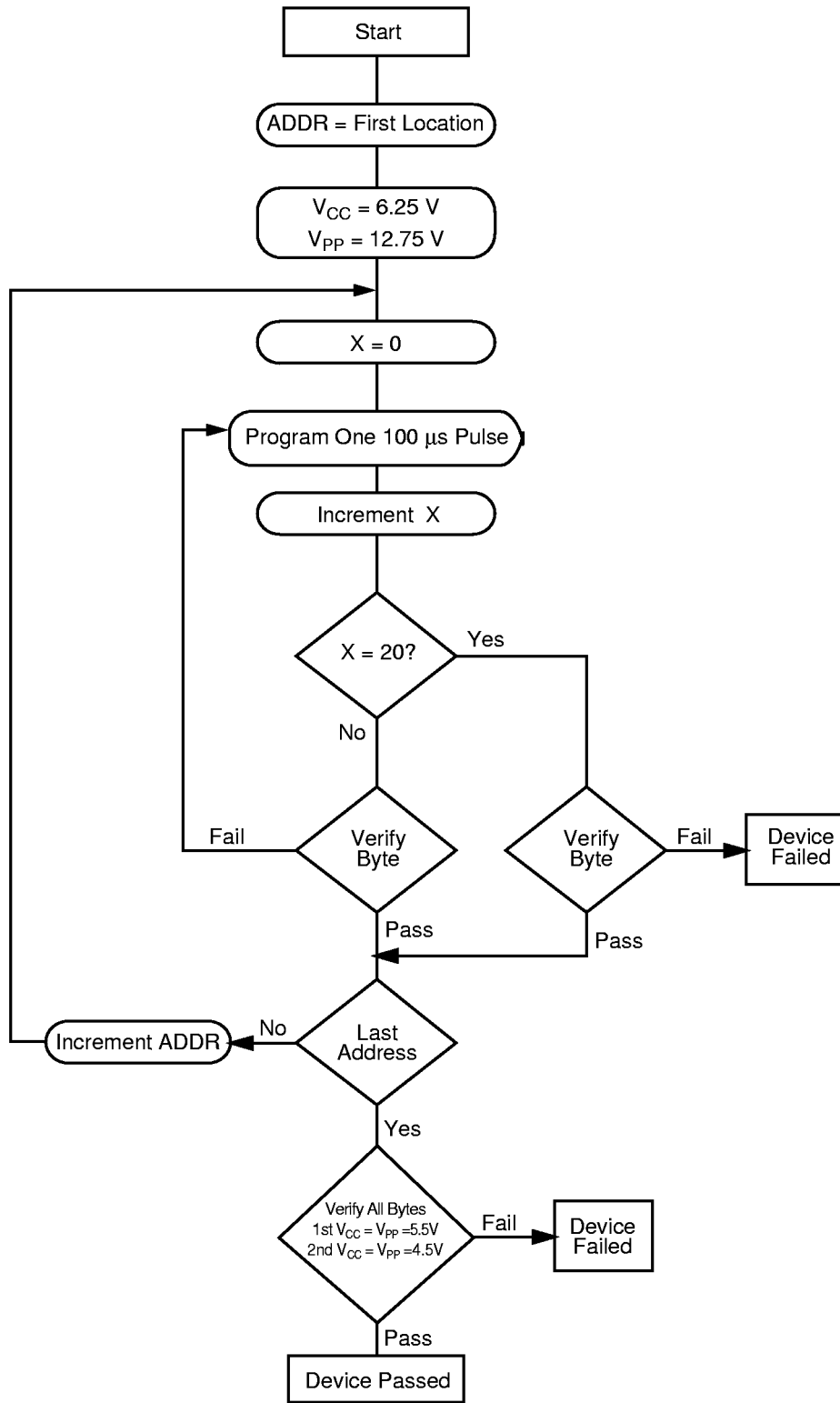
Note 11: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} . The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC} .

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Note 14)



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FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C32B are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for \overline{OE}/V_{PP} during programming. In the program mode the \overline{OE}/V_{PP} input is pulsed from a TTL low level to 12.75V.

Read Mode

The NMC27C32B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE) is the power control and should be used for device selection. Output Enable (\overline{OE}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of \overline{OE} , assuming that CE has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C32B has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C32B is placed in the standby mode by applying a CMOS high signal to the CE input. When in standby mode, the outputs are in a high impedance state, independent of the \overline{OE} input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

1. The lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE (pin 18) be decoded and used as the primary device selecting function, while \overline{OE} (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 20 \overline{OE}/V_{PP} will damage the NMC27C32B.

Initially, and after each erasure, all bits of the NMC27C32B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C32B is in the programming mode when \overline{OE}/V_{PP} is at 12.75V. It is required that at least a 0.1 μ F capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE input. A program pulse must be applied at each address location to be programmed. The NMC27C32B is programmed with the Fast Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 100 μ s pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 μ s pulse.

The NMC27C32B must not be programmed with a DC signal applied to the CE input.

Programming multiple NMC27C32Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32B may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE input programs the paralleled NMC27C32B.

TABLE 1. Mode Selection

Pins	CE (18)	\overline{OE}/V_{PP} (20)	V_{CC} (24)	Outputs (9–11, 13–17)
Mode				
Read	V_{IL}	V_{IL}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	Hi-Z
Program	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	Hi-Z

Program Inhibit

Programming multiple NMC27C32B in parallel with different data is also easily accomplished. Except for CE all like inputs (including OE) of the parallel NMC27C32B may be common. A TTL low level

program pulse applied to an NMC27C32B's CE input with \overline{OE}/V_{PP} at 12.75V will program that NMC27C32B. A TTL high level CE input inhibits the other NMC27C32B from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bit to determine whether they were correctly programmed. The verify is accomplished with OE/V_{pp} and CE at V_{IL}. Data should be verified t_{DV} after the falling edge of CE.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C32B has a manufacturer's identification code to aid in programming. The code, shown in Table 2, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C32B is, "8F01", where "8F" designates that it is made by Fairchild Semiconductor, and "01" designates a 32k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A11, CE, and OE are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å - 4000Å range. After programming, opaque labels should be placed over the NMC27C32B's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32B is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm².

The NMC27C32B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

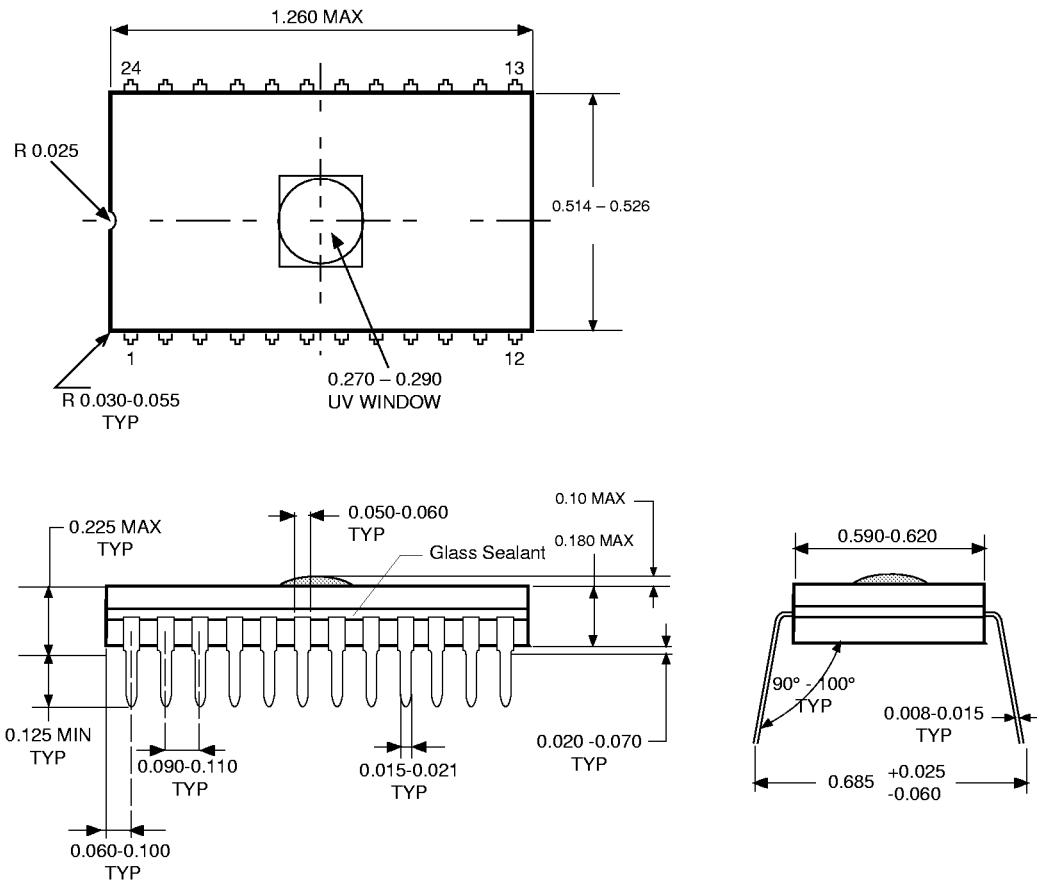
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE 2. Manufacturer's Identification Code

Pins	A0 (8)	O7 (17)	O6 (16)	O5 (15)	O4 (14)	O3 (13)	O2 (11)	O1 (10)	O0 (9)	Hex Data
Manufacturer Code	V _{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V _{IH}	0	0	0	0	0	0	0	1	01

Physical Dimensions inches (millimeters) unless otherwise noted



**UV Window Cavity Dual-In-Line Cerdip Package (JQ)
Order Number NMC27C32BQ
Package Number J24AQ**

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