Data Conversion HSMC

Reference Manual

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Contents

Additional Information

1. Overview

General Description

This manual provides technical information about the Data Conversion HSMC. This High Speed Mezzanine Card (HSMC) can be used for developing DSP applications with Altera Development boards that feature the High Speed Mezzanine Card (HSMC) connector. Figure 1–1. shows a topside view of the Data Conversion HSMC.

The Data Conversion HSMC was created to provide a set of Analog to Digital and Digital to Analog interfaces including an Audio Codec interface. The purpose of this reference manual is to describe each of the hardware interfaces on the Data Conversion HSMC.

For the latest information about High Speed Mezzanine Cards (HSMCs), go to **www.altera.com/products/devkits/kit-index.html**.

Figure 1–1. Data Conversion HSMC Topside View

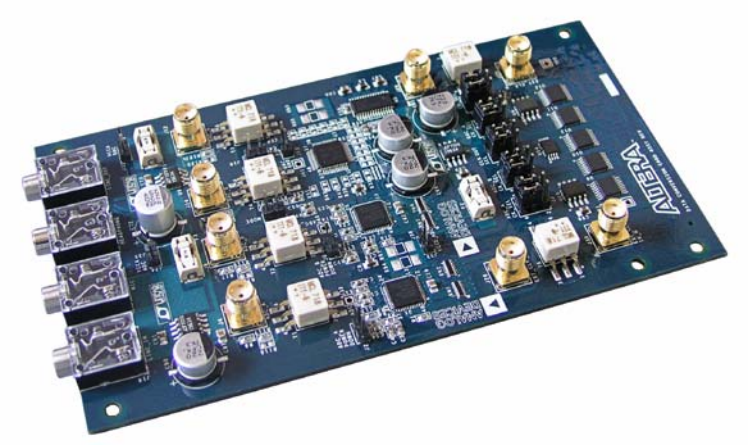


Figure 1–2 shows the Data Conversion HSMC in the DSP Development Kit, Cyclone III edition.

Figure 1–2. Data Conversion HSMC in the DSP Development Kit, Cyclone III Edition

For more information, refer *DSP Development Kit, Cyclone III Edition, Getting Started User Guide*.

Components and Block Diagram

Components

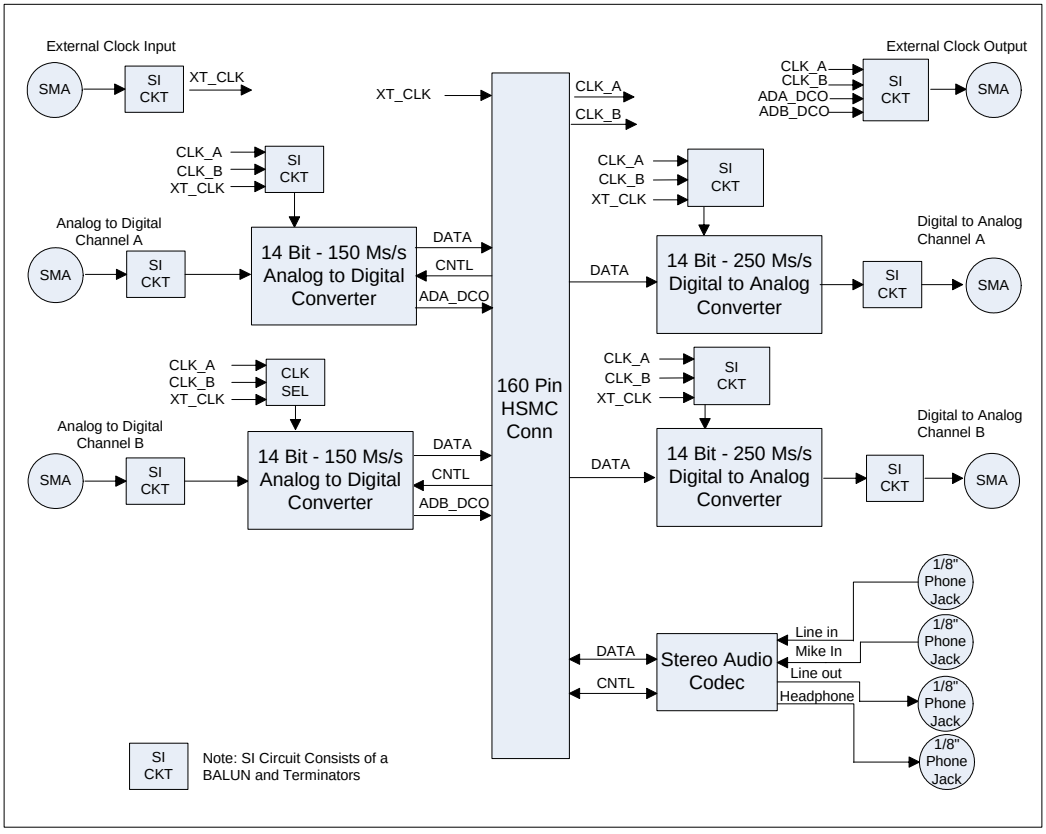
The Data Conversion HSMC contains the following components.

- Interfaces
  - HSMC Interface
  - Audio CODEC Interface
  - External Clock In Interface
  - External Clock Out Interface
  - ADC Channel A and B Input Interface
  - DAC Channel A and B Output Interface
- Power supply
- I2C Serial EEPROM

Block Diagram

Figure 1–3 shows a functional block diagram of the Data Conversion HSMC.

Figure 1–3. Data Conversion HSMC Block Diagram



2. Board Components and Interfaces

Board Overview

This chapter provides operational and connectivity details for the Data Conversion HSMC's major components and interfaces.

Board schematics, board layout database, and assembly files for the Data Conversion HSMC are included in the board_design_files subdirectory of the installed kit directory.

For information on powering-up the Data Conversion HSMC and installing the demo software and examples, refer to the user guide provided with your kit.

Figure 2–1 shows the top view of the Data Conversion HSMC.

Figure 2–1. Top View of the the Data Conversion HSMC

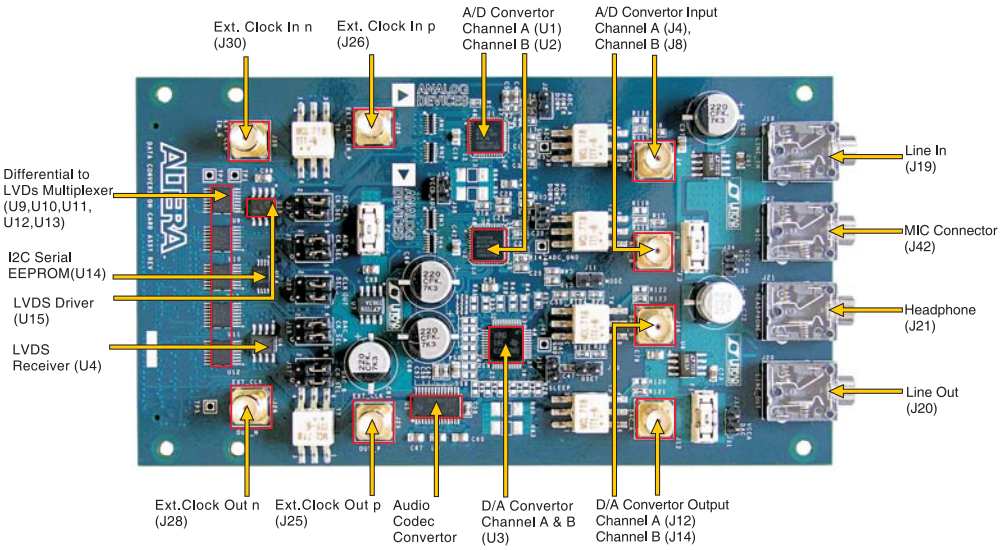


Figure 2–2 shows the back view of the Data Conversion HSMC.

Figure 2–2. Back View of the the Data Conversion HSMC

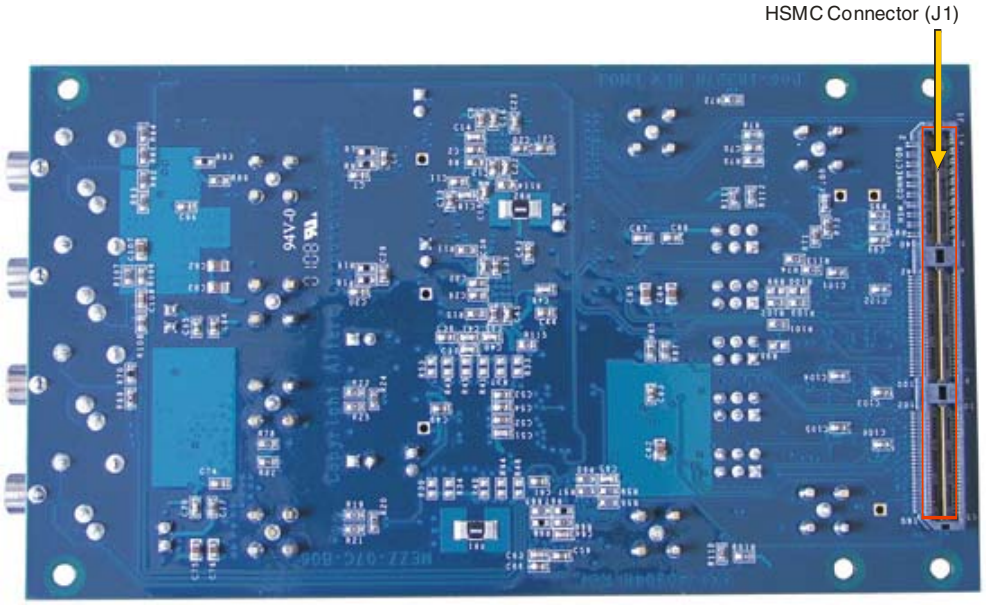


Table 2–1 lists the components and their corresponding board references.

Table 2–1. Data Conversion HSMC Feature Overview

Board Reference	Name	Description	Page
Configuration, Status and Setup Elements			
J3 (Channel A) J7 (Channel B)	A/D converter clock select jumper	Controls which of the three input clock signals (FPGA clock A, B, or the external SMA clock) is routed to the A/D converter	2–4
J2 (Channel A) J6 (Channel B)	Power down select jumper	Controls whether the ADC operates in power down or power up state	2–4
J15 (Channel A) J17 (Channel B)	D/A converter clock select jumper	Controls which of the three input clock signals (FPGA clock A, B, or the external SMA clock) is routed to the D/A converter	2–5
J11	Mode select jumper	Controls whether the DAC operates in dual bus mode or interleaved mode	2–5
J10	Gain setting select jumper	Controls whether the DAC channel's gain is set through one or two resistors	2–6

Table 2–1. Data Conversion HSMC Feature Overview

Board Reference	Name	Description	Page
J13	Sleep select jumper	Controls whether the DAC operates in power down or power up state	2–6
J23	External clock output select jumper	Selects which of the four input clocks (FPGA clock A, B or A/D converter Data Clock Output) is routed to the SMA clock out (J28)	2–6
Clock			
J26 (External Clock In-p) J30 (External Clock In-n)	External clock input SMA connectors	SMA connectors for a differential clock input	2–7
J25 (External Clock In-p) J28 (External Clock In-n)	External clock output SMA connectors	SMA connectors for a differential clock output	2–8
Components and Interfaces			
U1 (Channel A) U2 (Channel B)	A/D converter	Analog Devices AD9254. 14 bit, 150MS/s Analog to Digital converter	2–8
J4 (Channel A) J8 (Channel B)	A/D converter input SMA's	SMA's that drive the A/D converter inputs	2–13
U3 (Channel A and B)	D/A converter	Texas Instruments DAC5672. 14 bit, 175 MS/s Digital to Analog converter	2–13
J12 (Channel A) J14 (Channel B)	D/A converter output SMA's	SMA outputs for the D/A converters	2–17
U5	Audio CODEC	Texas Instruments TLV320AK23. Stereo Audio CODEC, 96KHz, with integrated headphone amplifier	2–17
J19	Line-in audio jack	3.5mm audio connector for line-in	2–18
J20	Line-out audio jack	3.5mm audio connector for line-out	2–18
J21	Headphone jack	3.5mm audio connector for headphones	2–18
J42	MIC jack	3.5mm audio connector for MIC	2–18
J1	HSMC	Expansion connector used to interface with Altera development boards	2–19
U14	I2C EEPROM	ISSI EEPROM IS24C02B, 2kbit	2–20

Configuration, Status and Setup Elements

This section describes configuration, status, and setup elements.

A/D Converter Clock Select Jumper (J3, J7)

Table 2–2 lists the J3 (channel A) and J7 (channel B) jumper settings used to select the A/D converter clock.

Table 2–2. A/D Converter Clock Select Jumper (J3,J7) Settings

Clock Source	Board Reference	Schematic Signal Name (1) (2) (3)	A/D Converter Clock Select (J3 or J7) Jumper Setting
FPGA Clock	HSMC Connector	FPGA_CLK_A_P FPGA_CLK_A_N	Pins 3 and 5, Pins 4 and 6
FPGA Clock	HSMC Connector	FPGA_CLK_B_P FPGA_CLK_B_N	Pins 1 and 3, Pins 4 and 6
External Clock	External Clock Input SMA	XT_IN_P XT_IN_N	Pins 3 and 5, Pins 2 and 4
No Clock	-	NO_CLK_P NO_CLK_N	Pins 1 and 3, Pins 2 and 4

Notes:
(1) See the appendices for FPGA pin-numbers for specific development boards.
(2) On the schematic MUX (U9) output signal names are ADA_CLK_SEL_P, ADA_CLK_SEL_N
(3) On the schematic MUX (U10) output signal names are ADB_CLK_SEL_P, ADB_CLK_SEL_N

Power Down Select Jumper (J2, J6)

The power down configuration of A/D converter is selectable through J2 (channel A) or J6 (channel B). Table 2–3 lists the jumper settings for power down options. A/D converters should be powered down when not used to reduce spurious noise output.

Table 2–3. Power Down Select Jumper Settings for AD9254 A/D Converter (U1, U2)

A/D Converter	Jumper Settings (1)	Description
U1 (Channel A)	J2 Jumper OFF	ADC channel A in normal (operational) state
U1 (Channel A)	J2 Jumper ON	ADC channel A in power down
U2 (Channel B)	J6 Jumper OFF	ADC channel B in normal (operational) state
U2 (Channel B)	J6 Jumper ON	ADC channel B in power down

Notes:
(1) If jumper pins are left open, ADC will be in normal state.

D/A Converter Clock Select Jumper (J15, J17)

Table 2–4 lists the J15 (channel A) and J17 (channel B) jumper settings used to select the D/A converter clock.

Table 2–4. D/A Converter Clock Select Jumper (J15, J17) Settings

Clock Source	Board Reference	Schematic Signal Name (1) (2)	D/A Converter Clock Select (J15 or J17) Jumper Setting
FPGA Clock	HSMC Connector	FPGA_CLK_A_P FPGA_CLK_A_N	Pins 3 and 5, Pins 4 and 6
FPGA Clock	HSMC Connector	FPGA_CLK_B_P FPGA_CLK_B_N	Pins 1 and 3, Pins 4 and 6
External Clock	External Clock Input SMA	XT_IN_P XT_IN_N	Pins 3 and 5, Pins 2 and 4
No Clock	-	NO_CLK_P NO_CLK_N	Pins 1 and 3, Pins 2 and 4

Notes:
(1) On the schematic MUX (U11) output signal names are DAC_CLK_1_P, DAC_CLK_1_N
(2) On the schematic MUX (U12) output signal names are DAC_CLK_2_P, DAC_CLK_2_N

Mode Select Jumper (J11)

The mode select jumper is used to put D/A converter in either dual bus or interleaved mode. It is selectable through J11 (channel A & channel B) Table 2–5 lists the jumper settings for mode select options.

Table 2–5. Mode Select Jumper (J11) Settings for DAC5672 D/A Converter

Jumper Settings (J11)	Description
Jumper ON	Interleaved mode
Jumper OFF	Dual bus mode

Gain Select Jumper (J10)

The Gain setting select jumper is used to set gain of D/A converter's channels. It is selectable through J10 (channel A & channel B) Table 2–6 lists the jumper settings for gain settings options.

Table 2–6. Gain Select Jumper (J10) Settings for DAC5672 D/A Converter

Jumper Settings (J10)	Description
Jumper ON	Sets gain of channel A through Rset on BiasJ_A pin and of channel B through Rset on BiasJ_B pin
Jumper OFF	Gain of channel A and B is set through Rset on BIASJ_a pin only and Rset on BIASJ_B pin is ignored

Sleep Select Jumper (J13)

The sleep select jumper is used to put D/A converter in power down mode. It is selectable through J13 (channel A & channel B). Table 2–7 lists the jumper settings for sleep select options. The D/A when not in use should be put in sleep mode.

Table 2–7. Sleep Select Jumper (J13) Settings for DAC5672 D/A Converter

Jumper Settings (J13)	Description
Jumper ON	Puts DAC in power down mode
Jumper OFF	DAC in normal state

External Clock Output Select Jumper (J23)

Table 2–8 lists External Clock Output Select Jumper (J23) Settings.

Table 2–8. External Clock Output Select Jumper (J23) Settings

Clock Source	Board Reference	Schematic Signal Name (1)	External Clock Output Select Jumper (J23) Settings
FPGA Clock	HSMC Connector	FPGA_CLK_A_P FPGA_CLK_A_N	Pins 3 and 5, Pins 4 and 6
FPGA Clock	HSMC Connector	FPGA_CLK_B_P FPGA_CLK_B_N	Pins 1 and 3, Pins 4 and 6
A/D A DCO	A/D Channel A	ADA_DCO_P ADA_DCO_N	Pins 3 and 5, Pins 2 and 4

Table 2–8. External Clock Output Select Jumper (J23) Settings			
Clock Source	**Board Reference**	**Schematic Signal Name (1)**	**External Clock Output Select Jumper (J23) Settings**
A/D B DCO	A/D Channel B	ADB_DCO_P ADB_DCO_N	Pins 1 and 3, Pins 2 and 4
Notes: (1) On the schematic MUX (U13) output signal names are RX_CLK_P, RX_CLK_N			

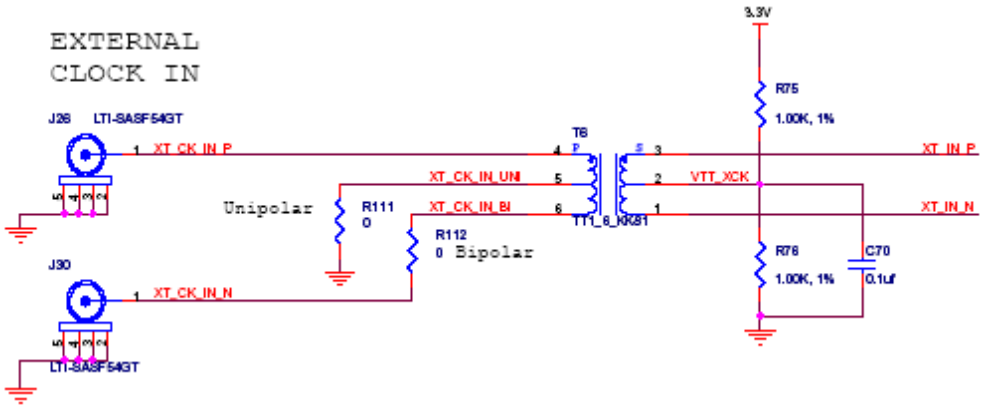
Clocks

This section describes External Clock Input and Output SMA connectors.

External Clock Input SMA Connectors (J26, J30)

The CLK SMA connector (J26, J30) provides an external clock input. It can be selected to be the input to U1, U2 and U3. See Figure 2–3. An external clock input provides designers, while using a particular design, the flexibility to use the same external clock source for the entire system under test. If you choose to use a single ended clock, R112 should be removed and R111 should be installed.

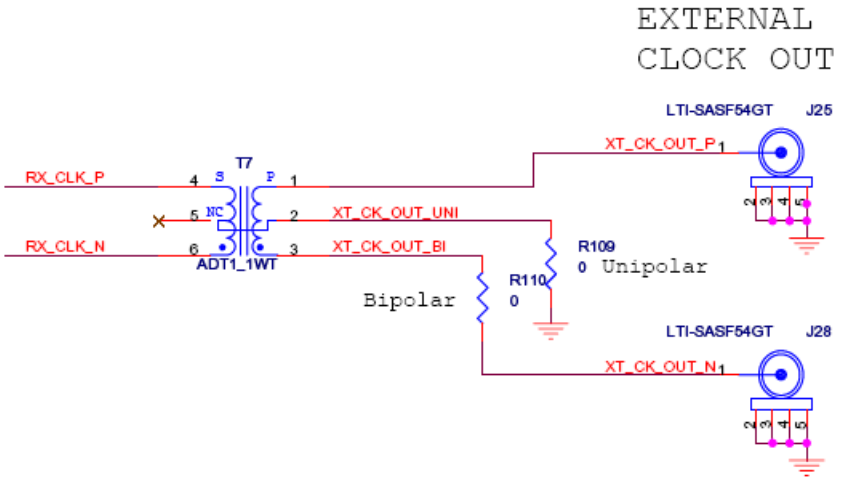
Figure 2–3. External Clock Input Schematic



External Clock Output SMA Connectors (J25, J28)

The CLK SMA connector (J25, J28) provides an external clock output. Different clocks can be selected by using differential LVDS multiplexer (U13) and clock select jumper (J23). See Figure 2–4. The external clock source provides designers, while using a particular design, the flexibility to alter the input frequency to verify FMAX tolerances. If you choose to use a single ended clock, R110 should be removed and R109 should be installed.

Figure 2–4. External Clock Output Schematic



Component Interfaces

This section describes the user interfaces, which consist of A/D converter, D/A converter, Audio Codec Converter, HSMC Connector, and I2C Serial EEPROM.

A/D Converter (U1, U2)

The Data Conversion HSMC contains two AD9254 14-bit 150 MSPS A/D converters. This device is designed for high speed and high-performance applications.

The inputs to these A/D converters are transformer-coupled in order to create a balanced input. The signal-to-noise ratio for the system is up to 72 dB for input signals from 1 MHz to the Nyquist frequency of the

converter. The maximum differential input voltage to the converter is 2 VPP. Usable voltage input to the SMA connector is approximately 512 mV when driven from a 50 Ohm source.

Table 2–9 lists the A/D converter references.

Table 2–9. A/D Converter Component Reference

Item	Description
Board reference	U1, U2
Part Number	AD9254
Device description	14 bit, 150 MSPS Analog to Digital converter
Manufacturer	Analog Device
Manufacturer web site	www.analog.com

Table 2–10 lists the pinouts of ADC Channel A.

Table 2–10. ADC Channel A (U1) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
ADA_D0	79	D0	45	Data Output Bit 0
ADA_D1	77	D1	46	Data Output Bit1
ADA_D2	73	D2	1	Data Output Bit 2
ADA_D3	71	D3	2	Data Output Bit 3
ADA_D4	67	D4	3	Data Output Bit 4
ADA_D5	65	D5	4	Data Output Bit 5
ADA_D6	61	D6	5	Data Output Bit 6
ADA_D7	59	D7	6	Data Output Bit 7
ADA_D8	55	D8	9	Data Output Bit 8
ADA_D9	53	D9	10	Data Output Bit 9
ADA_D10	49	D10	11	Data Output Bit 10
ADA_D11	47	D11	12	Data Output Bit 11
ADA_D12	43	D12	13	Data Output Bit 12
ADA_D13	41	D13	14	Data Output Bit 13
ADA_OR	83	OR	15	Out-of-Range Indicator
AD_SDIO	91	SDIO/DCS	18	Serial Port Interface (SPI) Data Input/Output (Serial Port Mode)
AD_SCLK	92	SCLK/DFS	19	Serial Port Interface Clock (Serial Port Mode)

Table 2–10. ADC Channel A (U1) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
ADA_SPI_CS	89	CSB	20	Serial Port Interface Chip Select (Active Low)
ADA_OE	85	OEB	43	Output Enable (Active Low)
ADA_DCO	156	DCO	44	Data Clock Output
-	-	ADA_CLK_P	38 (1)	Clock Input
-	-	ADA_CLK_N	39 (2)	Clock Input
-	-	ADA_PWDN	36 (3)	Power-Down Function Select

Notes:
(1) This pin is connected to Multiplexer pin U9.15.
(2) This pin is connected to Multiplexer pin U9.14.
(3) This pin is connected to Jumper pin J2.2.

Table 2–11 shows the pinout details of ADC Channel B.

Table 2–11. ADC Channel B (U2) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
ADB_D0	80	D0	45	Data Output Bit 0
ADB_D1	78	D1	46	Data Output Bit1
ADB_D2	74	D2	1	Data Output Bit 2
ADB_D3	72	D3	2	Data Output Bit 3
ADB_D4	68	D4	3	Data Output Bit 4
ADB_D5	66	D5	4	Data Output Bit 5
ADB_D6	62	D6	5	Data Output Bit 6
ADB_D7	60	D7	6	Data Output Bit 7
ADB_D8	56	D8	9	Data Output Bit 8
ADB_D9	54	D9	10	Data Output Bit 9
ADB_D10	50	D10	11	Data Output Bit 10
ADB_D11	48	D11	12	Data Output Bit 11
ADB_D12	44	D12	13	Data Output Bit 12
ADB_D13	42	D13	14	Data Output Bit 13
ADB_OR	84	OR	15	Out-of-Range Indicator
AD_SDIO	91	SDIO/DCS	18	Serial Port Interface (SPI) Data Input/Output (Serial Port Mode)
AD_SCLK	92	SCLK/DFS	19	Serial Port Interface Clock (Serial Port Mode)

Table 2–11. ADC Channel B (U2) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
ADB_SPI_CS	90	CSB	20	Serial Port Interface Chip Select (Active Low)
ADB_OE	86	OEB	43	Output Enable (Active Low)
ADB_DCO	158	DCO	44	Data Clock Output
-	-	ADB_CLK_P	38 (1)	Clock Input
-	-	ADB_CLK_N	39 (2)	Clock Input
-	-	ADB_PWDN	36 (3)	Power-Down Function Select

Notes:
(1) This pin is connected to Multiplexer pin U10.15.
(2) This pin is connected to Multiplexer pin U10.14.
(3) This pin is connected to Jumper pin J6.2.

A/D Converter Clocks

Figure 2–5 shows the components involved in selecting the clock signal to be sent to the AD9254 A/D converter (U1 for channel A, U2 for channel B). J3 (channel A) or J7 (channel B) selects the A/D clock from the FPGA clock A, the FPGA clock B or the External SMA clock (J26 and J30). The selected A/D clock passes through a differential to LVDS clock multiplexer (U9 for channel A, U10 for channel B), which provides the clock signal to the AD9254.

Figure 2–5. A/D Converter Clocking Options

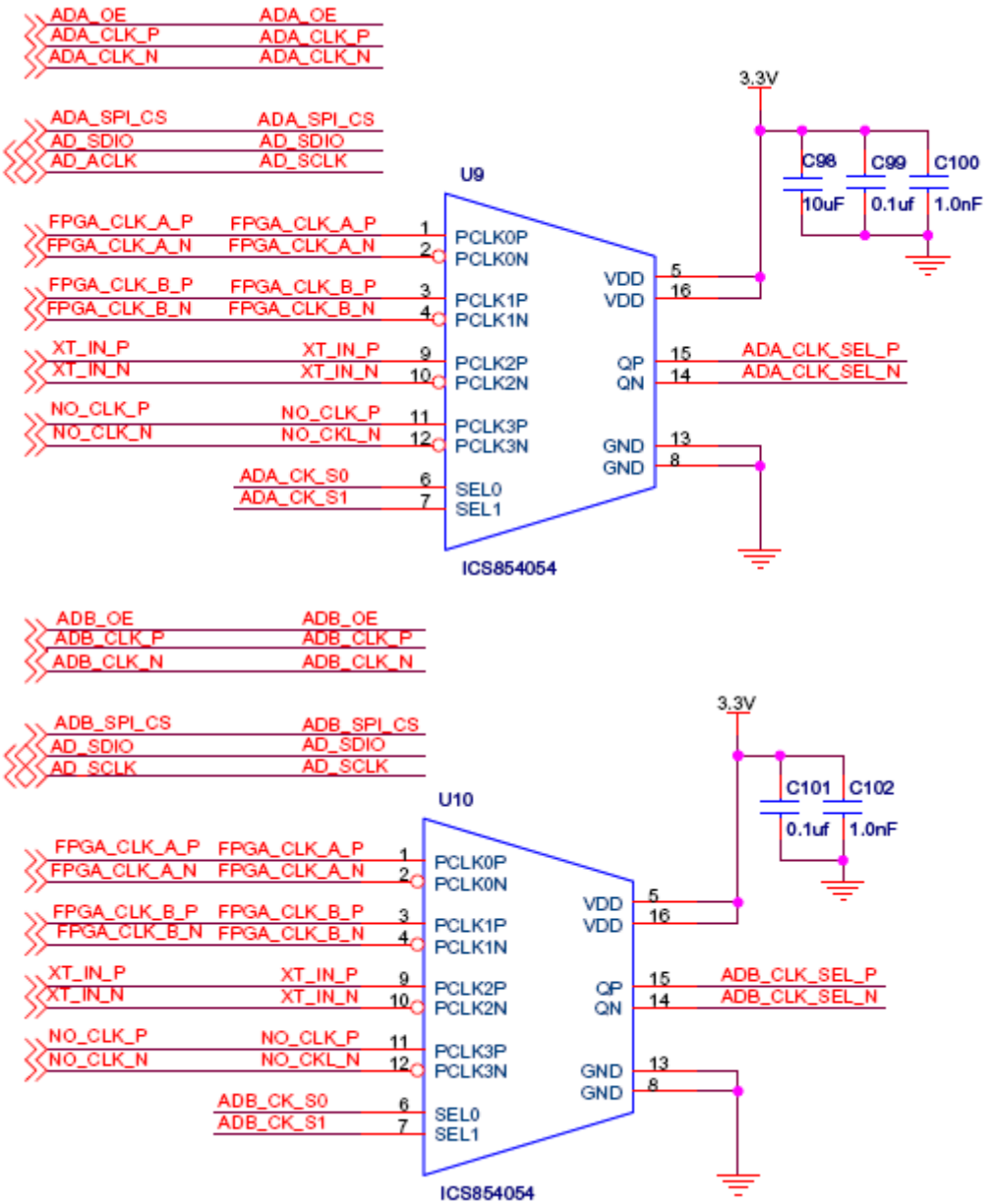


Table 2–12 lists the differential to LVDS clock multiplexer pinouts.

Table 2–12. Differential to LVDS Clock Multiplexer (U9, U10) Pinouts

Schematic Signal	HSMC Connector Pin Number	Device Signal	Device Pin No.	Description
FPGA_CLK_A_P	95	PCLK0P	1	Non-inverting Differential clock input
FPGA_CLK_A_N	97	PCLK0N	2	Inverting Differential clock input
FPGA_CLK_B_P	155	PCLK1P	3	Non-inverting Differential clock input
FPGA_CLK_B_N	157	PCLK1N	4	Inverting Differential clock input
XT_IN_P	96	PCLK2P	9	Non-inverting Differential clock input
XT_IN_N	98	PCLK2N	10	Inverting Differential clock input
AD(A,B)_CLK_SEL_P	-	QP	15	Non-inverting Differential Clock Output
AD(A,B)_CLK_SEL_N	-	QN	14	Inverting Differential Clock Output

A/D Converter Input SMA Connector (J4, J8)

J4 (channel A) and J8 (channel B) are standard through-hole SMA connectors used to interface the AD9254 A/D converter input with SMA cables.

D/A Converter (U3)

The D/A converter (U3 for channel A and B) on the Data Conversion HSMC provides 14-bit resolution and produces samples at rates up to 275 MSPS. It is a high-speed TI DAC5672 D/A converter and is set up to drive a differential-to-single output through a transformer. The output is transformer coupled and can be found on the SMA connector (J12 for channel A, J14 for channel B). The output of the TI DAC5672 D/A converter is set to the maximum output current of 20 mA. The signal-to-noise ratio for the system is up to 60 dB for output signals from 1 MHz to the Nyquist frequency of the converter.

Table 2–13 lists the D/A converter references.

Table 2–13. D/A Converter Component Reference

Item	Description
Board reference	U3
Part Number	DAC5672
Device description	14 bit, 275 MSPS Digital to Analog converter

Table 2–13. D/A Converter Component Reference	
Item	**Description**
Manufacturer	Texas Instruments
Manufacturer web site	www.ti.com

Table 2–14 lists the pinouts of DAC Channel A and Channel B.

Table 2–14. DAC Channel A and Channel B (U3) Pinouts				
HSMC Signal	**HSMC Pin**	**Device Signal**	**Device Pin No.**	**Description**
DA0	139	DA0	14	Data port A0
DA1	137	DA1	13	Data port A1
DA2	133	DA2	12	Data port A2
DA3	131	DA3	11	Data port A3
DA4	127	DA4	10	Data port A4
DA5	125	DA5	9	Data port A5
DA6	121	DA6	8	Data port A6
DA7	119	DA7	7	Data port A7
DA8	115	DA8	6	Data port A8
DA9	113	DA9	5	Data port A9
DA10	109	DA10	4	Data port A10
DA11	107	DA11	3	Data port A11
DA12	103	DA12	2	Data port A12
DA13	101	DA13	1	Data port A13
DB0	140	DB0	36	Data port B0
DB1	138	DB1	35	Data port B1
DB2	134	DB2	34	Data port B2
DB3	132	DB3	33	Data port B3
DB4	128	DB4	32	Data port B4
DB5	126	DB5	31	Data port B5
DB6	122	DB6	30	Data port B6
DB7	120	DB7	29	Data port B7
DB8	116	DB8	28	Data port B8
DB9	114	DB9	27	Data port B9
DB10	110	DB10	26	Data port B10
DB11	108	DB11	25	Data port B11

Table 2–14. DAC Channel A and Channel B (U3) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
DB12	104	DB12	24	Data port B12
DB13	102	DB13	23	Data port B13
-	-	CLKA	18 (1)	Clock input for DACA, CLKIQ in interleaved mode
-	-	CLKB	19 (2)	Clock input for DACB, RESETIQ in interleaved mode
-	-	GSET	42 (3)	Gain-setting mode: H – 1 resistor, L – 2 resistors. Internal pull-up.
-	-	MODE	48 (4)	Mode Select: H – Dual Bus, L – Interleaved. Internal pull-up.
-	-	SLEEP	37 (5)	Sleep function control input: H – DAC in power-down mode, L – DAC in operating mode. Internal pull-down.

Notes:
(1) This pin is connected to Differential Receiver pin U4.7.
(2) This pin is connected to Differential Receiver pin U4.6.
(3) This pin is connected to Jumper pin J10.1.
(4) This pin is connected to Jumper pin J11.1.
(5) This pin is connected to Jumper Pin J13.2.

D/A Converter Clocks

Figure 2–6 shows the components involved in selecting the clock signal to be sent to the DAC5672 (U3 for channel A and B). J15 (channel A) or J17 (channel B) selects the D/A clock from the FPGA clock A, the FPGA clock B, or the SMA clock (J26 and J30). The selected D/A clock passes through a differential to LVDS clock multiplexer (U11 for channel A, U12 for channel B), which provides the clock signal to 2 bit high speed differential receiver FIN1028 which in turn outputs clock to the DAC5672. (see "D/A Converter Clock Select Jumper (J15, J17)" on page 2–5.)

Figure 2–6. D/A Converter Clocking Options

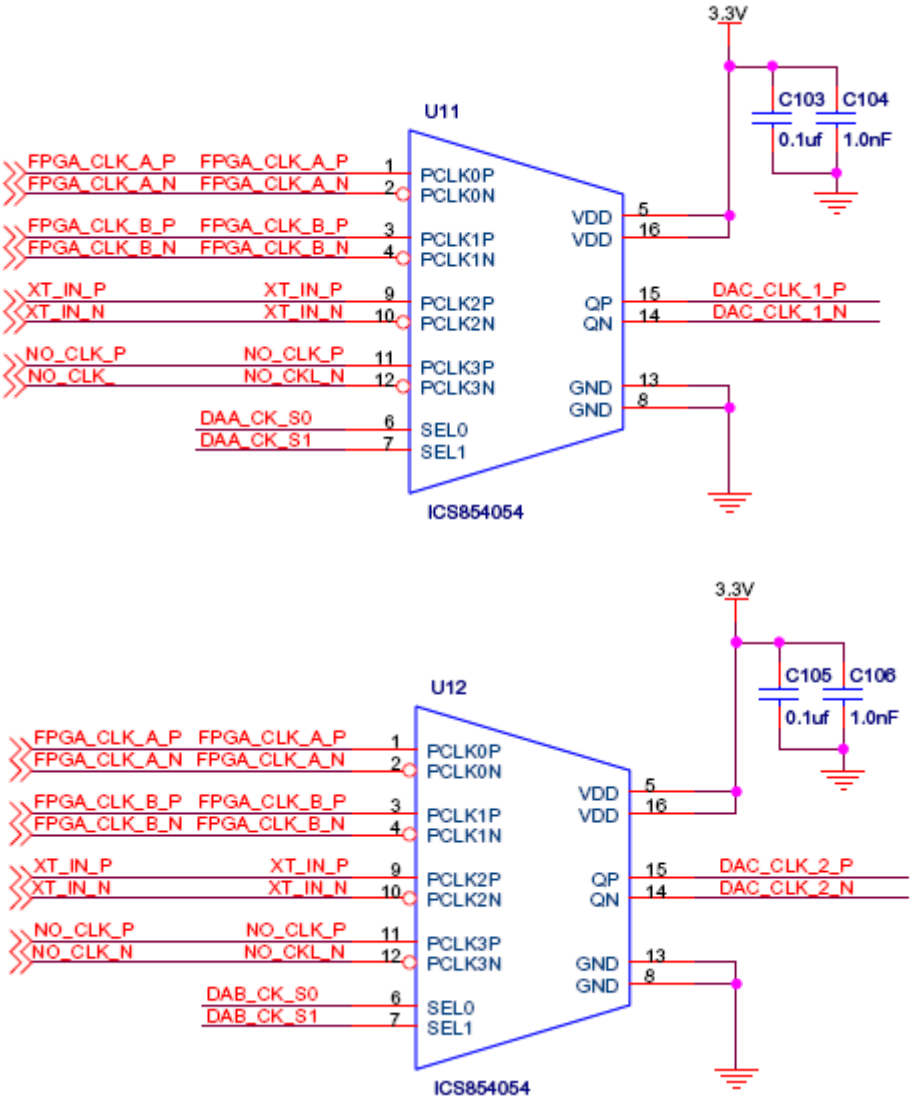


Table 2–15 lists the differential to LVDS clock multiplexer pinouts.

Table 2–15. Differential to LVDS Clock Multiplexer (U11, U12) Pinouts

Schematic Signal	HSMC Connector Pin Number	Device Signal	Device Pin No.	Description
FPGA_CLK_A_P	95	PCLK0P	1	Non-inverting Differential clock input
FPGA_CLK_A_N	97	PCLK0N	2	Inverting Differential clock input
FPGA_CLK_B_P	155	PCLK1P	3	Non-inverting Differential clock input
FPGA_CLK_B_N	157	PCLK1N	4	Inverting Differential clock input
XT_IN_P	96	PCLK2P	9	Non-inverting Differential clock input
XT_IN_N	98	PCLK2N	10	Inverting Differential clock input
DA(A,B)_CLK_SEL_P	-	QP	15	Non-inverting Differential Clock Output
DA(A,B)_CLK_SEL_N	-	QN	14	Inverting Differential Clock Output

D/A Converter Output SMA Connector (J12, J14)

J12 (channel A) and J14 (channel B) are standard through-hole SMA connectors used to interface the DAC5672 D/A converter output with SMA cables.

Audio CODEC Converter (U5)

The Data Conversion HSMC contains three stereo jack and one mic jack connectors which provide one stereo output, one stereo input, one amplified stereo headphone output, and one microphone input. The stereo jacks are driven by a stereo audio CODEC running at 8-96 kHz. Table 2–16 lists the audio CODEC references.

Table 2–16. Audio CODEC Converter Component Reference

Item	Description
Board reference	U5
Part Number	TLV320AIC23
Device description	Stereo Audio Codec, 8 to 96 KHz, with Integrated Headphone Amplifier
Manufacturer	Texas Instruments
Manufacturer web site	www.ti.com

Table 2–17 lists the TI TLV320AIC23 audio CODEC pin-outs.

Table 2–17. Audio CODEC Converter (U5) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
AIC_XCLK	150	XTI/MCLK	25	Crystal or external-clock input. Used for derivation of all internal clocks on the AIC23B
AIC_LRCOUT	146	LRCOUT	7	I2S ADC-word clock signal. In audio master mode, the AIC23B generates this framing signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP.
AIC_LRCIN	145	LRCIN	5	I2S DAC-word clock signal. In audio master mode, the AIC23B generates this framing signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP.
AIC_DIN	143	DIN	4	I2S format serial data input to the sigma-delta stereo DAC
AIC_DOUT	144	DOUT	6	I2S format serial data output from the sigma-delta stereo ADC
AD_SCLK	92	SCLK	24	Control-port serial-data clock. For SPI and 2-wire control modes this is the serial-clock input.
AD_SDIO	91	SDIN	23	I2S format serial data input to the sigma-delta stereo DAC
AIC_SPI_CS	151	CS_n	21	Serial Control Interface Chip Select (Active Low)
AIC_BCLK	149	BCLK	3	I2S serial-bit clock. In audio master mode, the AIC23B generates this signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP

Audio Jacks (J19, J20, J21, J42)

The Data Conversion HSMC contains the following audio connectors:

- J19—an audio connector for line-in
- J20—an audio connector for line-out
- J21—an audio connector for amplified line-out
- J42—an audio connector for mic

HSMC Connector (J1)

The Data Conversion HSMC connects to Altera FPGA Starter and Development Boards via a single High Speed Mezzanine Card (HSMC) connector (J6).

Table 2–18 below lists HSMC connector board reference and manufacturing information.

Table 2–18. HSMC Connector Component Reference

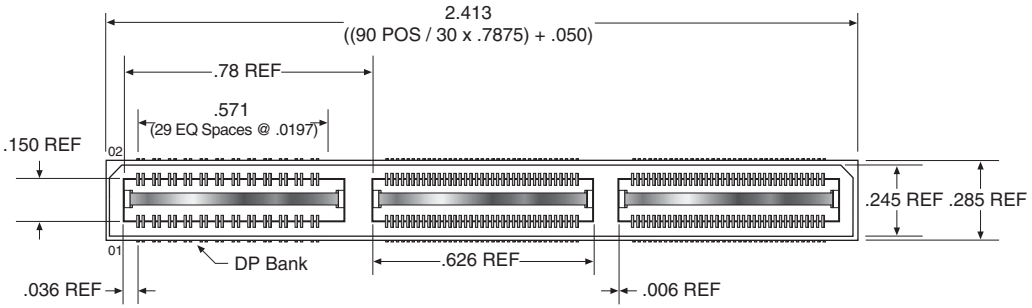
Item	Description
Board reference	J1
Part Number	ASP-122952-01
Device description	High Speed Mezzanine Card Connector
Manufacturer	Samtec
Manufacturer web site	http://www.samtec.com/signal_integrity/altera.asp

The HSMC connector is a modified version of standard high-speed Samtec connectors. To provide better integrity between host boards and daughter cards when using high-speed transceivers, the standard high-speed Samtec connector is modified by removing every third pin in bank 1.

CMOS utilization of the HSMC pins is assumed and no options for supporting other differential signaling are provided with the board. The eight clock-data-recovery high-speed transceiver channels are not connected on this HSMC.

The HSMC connector layout is shown in Figure 2–7 below.

Figure 2–7. Samtec Header Connector



I2C Serial EEPROM (U14)

There is a 2k-bits I2C Serial EEPROM on the Data Conversion HSMC. Table 2–19 below lists I2C Serial EEPROM board reference and manufacturing information.

Table 2–19. I2C Serial EEPROM Component Reference

Item	Description
Board reference	U14
Part Number	IS24C02B
Device description	2k-bits I2C Serial EEPROM
Manufacturer	ISSI
Manufacturer web site	www.issi.com

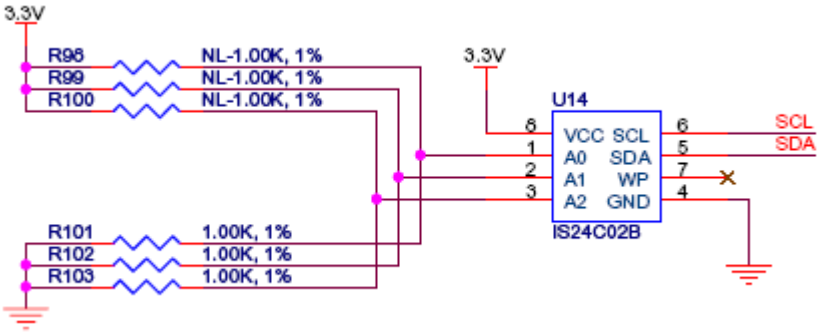
Table 2–20 shows the pinout of I2C Serial EEPROM with HSMC Connector.

Table 2–20. I2C Serial EEPROM (U14) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
SCL	34	SCL	6	Serial Clock Input
SDA	33	SDA	5	Serial Address/Data I/O

Figure 2–8 shows the I2C Serial EEPROM schematic.

Figure 2–8. I2C Serial EEPROM Schematic



Power Supply

Analog to Digital Power Supplies (U6, U7, U8)

The power supply block distributes clean power from the 12 V and 3.3 V input supply (from the host board through the HSMC Connector) to the Data Conversion HSMC through on-board regulators. To provide various voltage options, the board uses several Linear Technologies' regulators.

Table 2–21 below lists Power Supplies board reference and manufacturing information.

Table 2–21. Power Supplies Component Reference

Item	Description
Board reference	U6, U7, U8
Part Number	LT1963
Device description	LT1963A - 1.5A, Low Noise, Fast Transient Response LDO Regulators
Manufacturer	Linear Technology
Manufacturer web site	www.linear.com

Appendix A. Pinouts for the Cyclone III (3C120) Development Board

Introduction

The section below describes the HSMC Port A interface pinouts for the Cyclone III EP3C120F780 Development board. See Table A–1.

Table A–1. HSMC Port A Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
33	SDA	HSMA_SDA	AC1
34	SCL	HSMA_SCL	AC3
41	ADA_D13	HSMA_D0	AB6
42	ADB_D13	HSMA_D1	AF2
43	ADA_D12	HSMA_D2	AE3
44	ADB_D12	HSMA_D3	AC5
47	ADA_D11	HSMA_TX_D_P0	R7
48	ADB_D11	HSMA_RX_D_P0	AB2
49	ADA_D10	HSMA_TX_D_N0	R6
50	ADB_D10	HSMA_RX_D_N0	AB1
53	ADA_D9	HSMA_TX_D_P1	V4
54	ADB_D9	HSMA_RX_D_P1	Y4
55	ADA_D8	HSMA_TX_D_N1	V3
56	ADB_D8	HSMA_RX_D_N1	Y3
59	ADA_D7	HSMA_TX_D_P2	T4
60	ADB_D7	HSMA_RX_D_P2	U3
61	ADA_D6	HSMA_TX_D_N2	T3
62	ADB_D6	HSMA_RX_D_N2	U4
65	ADA_D5	HSMA_TX_D_P3	R3
66	ADB_D5	HSMA_RX_D_P3	W2
67	ADA_D4	HSMA_TX_D_N3	R4
68	ADB_D4	HSMA_RX_D_N3	W1
71	ADA_D3	HSMA_TX_D_P4	M8
72	ADB_D3	HSMA_RX_D_P4	V2

Table A–1. HSMC Port A Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
73	ADA_D2	HSMA_TX_D_N4	M7
74	ADB_D2	HSMA_RX_D_N4	V1
77	ADA_D1	HSMA_TX_D_P5	P2
78	ADB_D1	HSMA_RX_D_P5	U2
79	ADA_D0	HSMA_TX_D_N5	P1
80	ADB_D0	HSMA_RX_D_N5	U1
83	ADA_OR	HSMA_TX_P6	AE6
84	ADB_OR	HSMA_RX_P6	AF4
85	ADA_OE	HSMA_TX_N6	AE5
86	ADB_OE	HSMA_RX_N6	AF3
89	ADA_SPI_CS	HSMA_TX_P7	AD4
90	ADB_SPI_CS	HSMA_RX_P7	AG1
91	AD_SDIO	HSMA_TX_N7	AD3
92	AD_SCLK	HSMA_RX_N7	AH1
95	FPGA_CLK_A_P	HSMA_CLK_OUT_P1	V10
96	XT_IN_P	HSMA_CLK_IN_P1	Y4
97	FPGA_CLK_A_N	HSMA_CLK_OUT_N1	W9
98	XT_IN_N	HSMA_CLK_IN_N1	W3
101	DA13	HSMA_TX_P8	AC6
102	DB13	HSMA_RX_P8	AF2
103	DA12	HSMA_TX_N8	AC5
104	DB12	HSMA_RX_N8	AF1
107	DA11	HSMA_TX_P9	AB5
108	DB11	HSMA_RX_P9	AB6
109	DA10	HSMA_TX_N9	AE2
110	DB10	HSMA_RX_N9	AE1
113	DA9	HSMA_TX_P10	AB8
114	DB9	HSMA_RX_P10	AE4
115	DA8	HSMA_TX_N10	AC7

Table A–1. HSMC Port A Interface Pinout			
Data Conversion HSMC Schematic		**Development Board Schematic**	
Connector (J1) Pin No.	**Signal Name**	**Signal Name**	**FPGA Pin No.**
116	DB8	HSMA_RX_N10	AE3
119	DA7	HSMA_TX_P11	Y6
120	DB7	HSMA_RX_P11	AC2
121	DA6	HSMA_TX_N11	Y5
122	DB6	HSMA_RX_N11	AD1
125	DA5	HSMA_TX_P12	AA7
126	DB5	HSMA_RX_P12	AB2
127	DA4	HSMA_TX_N12	AA6
128	DB4	HSMA_RX_N12	AC1
131	DA3	HSMA_TX_P13	Y8
132	DB3	HSMA_RX_P13	AA1
133	DA2	HSMA_TX_N13	Y7
134	DB2	HSMA_RX_N13	AB1
137	DA1	HSMA_TX_P14	AC4
138	DB1	HSMA_RX_P14	Y10
139	DA0	HSMA_TX_N14	Y9
140	DB0	HSMA_RX_N14	AB3
143	AIC_DIN	HSMA_TX_P15	W12
144	AIC_DOUT	HSMA_RX_P15	AB4
145	AIC_LRCIN	HSMA_TX_N15	Y11
146	AIC_LRCOUT	HSMA_RX_N15	AA3
149	AIC_BCLK	HSMA_TX_P16	AA12
150	AIC_XCLK	HSMA_RX_P16	AA4
151	AIC_SPI_CS	HSMA_TX_N16	AB11
155	FPGA_CLK_B_P	HSMA_CLK_OUT_P2	W8
156	ADA_DCO	HSMA_CLK_IN_P2	T2
157	FPGA_CLK_B_N	HSMA_CLK_OUT_N2	W7
158	ADB_DCO	HSMA_CLK_IN_N2	T1

The section below describes HSMC Port B interface pinouts for the Cyclone III EP3C120F780 Development board. See Table A–2.

Table A–2. HSMC Port B Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
33	SDA	HSMB_SDA	H26
34	SCL	HSMB_SCL	H25
41	ADA_D13	HSMB_D0	G24
42	ADB_D13	HSMB_D1	H23
43	ADA_D12	HSMB_D2	G25
44	ADB_D12	HSMB_D3	H24
47	ADA_D11	HSMB_TX_D_P0	J25
48	ADB_D11	HSMB_RX_D_P0	F27
49	ADA_D10	HSMB_TX_D_N0	J26
50	ADB_D10	HSMB_RX_D_N0	F28
53	ADA_D9	HSMB_TX_D_P1	L23
54	ADB_D9	HSMB_RX_D_P1	G27
55	ADA_D8	HSMB_TX_D_N1	L24
56	ADB_D8	HSMB_RX_D_N1	G28
59	ADA_D7	HSMB_TX_D_P2	M25
60	ADB_D7	HSMB_RX_D_P2	K25
61	ADA_D6	HSMB_TX_D_N2	M26
62	ADB_D6	HSMB_RX_D_N2	K26
65	ADA_D5	HSMB_TX_D_P3	N25
66	ADB_D5	HSMB_RX_D_P3	K27
67	ADA_D4	HSMB_TX_D_N3	N26
68	ADB_D4	HSMB_RX_D_N3	K28
71	ADA_D3	HSMB_TX_D_P4	R27
72	ADB_D3	HSMB_RX_D_P4	L27
73	ADA_D2	HSMB_TX_D_N4	R28
74	ADB_D2	HSMB_RX_D_N4	L28
77	ADA_D1	HSMB_TX_D_P5	R25
78	ADB_D1	HSMB_RX_D_P5	M27

Table A–2. HSMC Port B Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	**Signal Name**	**Signal Name**	**FPGA Pin No.**
79	ADA_D0	HSMB_TX_D_N5	R26
80	ADB_D0	HSMB_RX_D_N5	M28
83	ADA_OR	HSMB_TX_D_P6	U25
84	ADB_OR	HSMB_RX_D_P6	P25
85	ADA_OE	HSMB_TX_D_N6	U26
86	ADB_OE	HSMB_RX_D_N6	P26
89	ADA_SPI_CS	HSMB_TX_D_P7	V27
90	ADB_SPI_CS	HSMB_RX_D_P7	P27
91	AD_SDIO	HSMB_TX_D_N7	V28
92	AD_SCLK	HSMB_RX_D_N7	P28
95	FPGA_CLK_A_P	HSMB_CLK_OUT_P1	AC26
96	XT_IN_P	HSMB_CLK_IN_P1	J27
97	FPGA_CLK_A_N	HSMB_CLK_OUT_N1	AD26
98	XT_IN_N	HSMB_CLK_IN_N1	J28
101	DA13	HSMB_TX_D_P8	V25
102	DB13	HSMB_RX_D_P8	P21
103	DA12	HSMB_TX_D_N8	V26
104	DB12	HSMB_RX_D_N8	R21
107	DA11	HSMB_TX_D_P9	W25
108	DB11	HSMB_RX_D_P9	R22
109	DA10	HSMB_TX_D_N9	W26
110	DB10	HSMB_RX_D_N9	R23
113	DA9	HSMB_TX_D_P10	Y25
114	DB9	HSMB_RX_D_P10	T25
115	DA8	HSMB_TX_D_N10	Y26
116	DB8	HSMB_RX_D_N10	T26
119	DA7	HSMB_TX_D_P11	AA25
120	DB7	HSMB_RX_D_P11	U27
121	DA6	HSMB_TX_D_N11	AA26
122	DB6	HSMB_RX_D_N11	U28
125	DA5	HSMB_TX_D_P12	AB25

Table A–2. HSMC Port B Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
126	DB5	HSMB_RX_D_P12	U22
127	DA4	HSMB_TX_D_N12	AB26
128	DB4	HSMB_RX_D_N12	V22
131	DA3	HSMB_TX_D_P13	Y23
132	DB3	HSMB_RX_D_P13	W28
133	DA2	HSMB_TX_D_N13	Y24
134	DB2	HSMB_RX_D_N13	W27
137	DA1	HSMB_TX_D_P14	AE27
138	DB1	HSMB_RX_D_P14	V23
139	DA0	HSMB_TX_D_N14	AE28
140	DB0	HSMB_RX_D_N14	V24
143	AIC_DIN	HSMB_TX_D_P15	W22
144	AIC_DOUT	HSMB_RX_D_P15	AB27
145	AIC_LRCIN	HSMB_TX_D_N15	Y22
146	AIC_LRCOUT	HSMB_RX_D_N15	AB28
149	AIC_BCLK	HSMB_TX_D_P16	V21
150	AIC_XCLK	HSMB_RX_D_P16	AC27
151	AIC_SPI_CS	HSMB_TX_D_N16	W21
155	FPGA_CLK_B_P	HSMB_CLK_OUT_P2	AD27
156	ADA_DCO	HSMB_CLK_IN_P2	Y27
157	FPGA_CLK_B_N	HSMB_CLK_OUT_N2	AD28
158	ADB_DCO	HSMB_CLK_IN_N2	Y28

Appendix B. Pinouts for the Stratix III (3SL150) Development Board

Introduction

The section below describes the HSMC Port A interface pinouts for the Stratix III (3SL150) Development board. See Table B–1

Table B–1. HSMC Port A Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
33	SDA	HSMA_SDA	P8
34	SCL	HSMA_SCL	AA32
41	ADA_D13	HSMA_D0	AK9
42	ADB_D13	HSMA_D1	AJ9
43	ADA_D12	HSMA_D2	AL7
44	ADB_D12	HSMA_D3	AL9
47	ADA_D11	HSMA_TX_P0	AC11
48	ADB_D11	HSMA_RX_P0	AJ4
49	ADA_D10	HSMA_TX_N0	AB10
50	ADB_D10	HSMA_RX_N0	AJ3
53	ADA_D9	HSMA_TX_P1	AC9
54	ADB_D9	HSMA_RX_P1	AG4
55	ADA_D8	HSMA_TX_N1	AC8
56	ADB_D8	HSMA_RX_N1	AG3
59	ADA_D7	HSMA_TX_P2	AH5
60	ADB_D7	HSMA_RX_P2	AM2
61	ADA_D6	HSMA_TX_N2	AH4
62	ADB_D6	HSMA_RX_N2	AM1
65	ADA_D5	HSMA_TX_P3	AE8
66	ADB_D5	HSMA_RX_P3	AL2
67	ADA_D4	HSMA_TX_N3	AE7

Table B–1. HSMC Port A Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
68	ADB_D4	HSMA_RX_N3	AL1
71	ADA_D3	HSMA_TX_P4	AF6
72	ADB_D3	HSMA_RX_P4	AJ2
73	ADA_D2	HSMA_TX_N4	AF5
74	ADB_D2	HSMA_RX_N4	AK1
77	ADA_D1	HSMA_TX_P5	AD7
78	ADB_D1	HSMA_RX_P5	AH2
79	ADA_D0	HSMA_TX_N5	AD6
80	ADB_D0	HSMA_RX_N5	AJ1
83	ADA_OR	HSMA_TX_P6	AE6
84	ADB_OR	HSMA_RX_P6	AF4
85	ADA_OE	HSMA_TX_N6	AE5
86	ADB_OE	HSMA_RX_N6	AF3
89	ADA_SPI_CS	HSMA_TX_P7	AD4
90	ADB_SPI_CS	HSMA_RX_P7	AG1
91	AD_SDIO	HSMA_TX_N7	AD3
92	AD_SCLK	HSMA_RX_N7	AH1
95	FPGA_CLK_A_P	HSMA_CLK_OUT_P1	V10
96	XT_IN_P	HSMA_CLK_IN_P1	Y4
97	FPGA_CLK_A_N	HSMA_CLK_OUT_N1	W9
98	XT_IN_N	HSMA_CLK_IN_N1	W3
101	DA13	HSMA_TX_P8	AC6
102	DB13	HSMA_RX_P8	AF2
103	DA12	HSMA_TX_N8	AC5
104	DB12	HSMA_RX_N8	AF1
107	DA11	HSMA_TX_P9	AB5
108	DB11	HSMA_RX_P9	AB6
109	DA10	HSMA_TX_N9	AE2

Table B–1. HSMC Port A Interface Pinout			
Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
110	DB10	HSMA_RX_N9	AE1
113	DA9	HSMA_TX_P10	AB8
114	DB9	HSMA_RX_P10	AE4
115	DA8	HSMA_TX_N10	AC7
116	DB8	HSMA_RX_N10	AE3
119	DA7	HSMA_TX_P11	Y6
120	DB7	HSMA_RX_P11	AC2
121	DA6	HSMA_TX_N11	Y5
122	DB6	HSMA_RX_N11	AD1
125	DA5	HSMA_TX_P12	AA7
126	DB5	HSMA_RX_P12	AB2
127	DA4	HSMA_TX_N12	AA6
128	DB4	HSMA_RX_N12	AC1
131	DA3	HSMA_TX_P13	Y8
132	DB3	HSMA_RX_P13	AA1
133	DA2	HSMA_TX_N13	Y7
134	DB2	HSMA_RX_N13	AB1
137	DA1	HSMA_TX_P14	AC4
138	DB1	HSMA_RX_P14	Y10
139	DA0	HSMA_TX_N14	Y9
140	DB0	HSMA_RX_N14	AB3
143	AIC_DIN	HSMA_TX_P15	W12
144	AIC_DOUT	HSMA_RX_P15	AB4
145	AIC_LRCIN	HSMA_TX_N15	Y11
146	AIC_LRCOUT	HSMA_RX_N15	AA3
149	AIC_BCLK	HSMA_TX_P16	AA12
150	AIC_XCLK	HSMA_RX_P16	AA4
151	AIC_SPI_CS	HSMA_TX_N16	AB11

Table B–1. HSMC Port A Interface Pinout			
Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
155	FPGA_CLK_B_P	HSMA_CLK_OUT_P2	W8
156	ADA_DCO	HSMA_CLK_IN_P2	T2
157	FPGA_CLK_B_N	HSMA_CLK_OUT_N2	W7
158	ADB_DCO	HSMA_CLK_IN_N2	T1

The section below describes the HSMC Port B interface pinouts for the Stratix III (3SL150) Development board. See Table B–2

Table B–2. HSMC Port B Interface Pinout			
Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
33	SDA	HSMB_SDA	U11
34	SCL	HSMB_SCL	AD31
41	ADA_D13	HSMB_D0	AB24
42	ADB_D13	HSMB_D1	AB25
43	ADA_D12	HSMB_D2	AF32
44	ADB_D12	HSMB_D3	AF31
47	ADA_D11	HSMB_TX_P0	P11
48	ADB_D11	HSMB_RX_P0	R4
49	ADA_D10	HSMB_TX_N0	P10
50	ADB_D10	HSMB_RX_N0	R3
53	ADA_D9	HSMB_TX_P1	T9
54	ADB_D9	HSMB_RX_P1	P4
55	ADA_D8	HSMB_TX_N1	T8
56	ADB_D8	HSMB_RX_N1	P3
59	ADA_D7	HSMB_TX_P2	T7
60	ADB_D7	HSMB_RX_P2	P2

Table B–2. HSMC Port B Interface Pinout			
Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
61	ADA_D6	HSMB_TX_N2	U6
62	ADB_D6	HSMB_RX_N2	R1
65	ADA_D5	HSMB_TX_P3	T5
66	ADB_D5	HSMB_RX_P3	N2
67	ADA_D4	HSMB_TX_N3	T4
68	ADB_D4	HSMB_RX_N3	P1
71	ADA_D3	HSMB_TX_P4	R10
72	ADB_D3	HSMB_RX_P4	M1
73	ADA_D2	HSMB_TX_N4	R9
74	ADB_D2	HSMB_RX_N4	N1
77	ADA_D1	HSMB_TX_P5	R7
78	ADB_D1	HSMB_RX_P5	L2
79	ADA_D0	HSMB_TX_N5	R6
80	ADB_D0	HSMB_RX_N5	L1
83	ADA_OR	HSMB_TX_P6	N9
84	ADB_OR	HSMB_RX_P6	K4
85	ADA_OE	HSMB_TX_N6	N8
86	ADB_OE	HSMB_RX_N6	K3
89	ADA_SPI_CS	HSMB_TX_P7	M7
90	ADB_SPI_CS	HSMB_RX_P7	J4
91	AD_SDIO	HSMB_TX_N7	M6
92	AD_SCLK	HSMB_RX_N7	J3
95	FPGA_CLK_A_P	HSMB_CLK_OUT_P1	P6
96	XT_IN_P	HSMB_CLK_IN_P1	N4
97	FPGA_CLK_A_N	HSMB_CLK_OUT_N1	P5
98	XT_IN_N	HSMB_CLK_IN_N1	N3
101	DA13	HSMB_TX_P8	L7
102	DB13	HSMB_RX_P8	H2

Table B–2. HSMC Port B Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
103	DA12	HSMB_TX_N8	L6
104	DB12	HSMB_RX_N8	J1
107	DA11	HSMB_TX_N9	L4
108	DB11	HSMB_TX_P9	L5
109	DA10	HSMB_RX_P9	G2
110	DB10	HSMB_RX_N9	H1
113	DA9	HSMB_TX_P10	K6
114	DB9	HSMB_RX_P10	F1
115	DA8	HSMB_TX_N10	K5
116	DB8	HSMB_RX_N10	G1
119	DA7	HSMB_TX_P11	J7
120	DB7	HSMB_RX_P11	H4
121	DA6	HSMB_TX_N11	J6
122	DB6	HSMB_RX_N11	H3
125	DA5	HSMB_TX_P12	H6
126	DB5	HSMB_RX_P12	E2
127	DA4	HSMB_TX_N12	H5
128	DB4	HSMB_RX_N12	E1
131	DA3	HSMB_TX_P13	K8
132	DB3	HSMB_RX_P13	C1
133	DA2	HSMB_TX_N13	K7
134	DB2	HSMB_RX_N13	D1
137	DA1	HSMB_RX_P14	D3
138	DB1	HSMB_TX_P14	L8
139	DA0	HSMB_TX_N14	L9
140	DB0	HSMB_RX_N14	D2
143	AIC_DIN	HSMB_TX_P15	M10
144	AIC_DOUT	HSMB_RX_P15	G5

Table B–2. HSMC Port B Interface Pinout			
Data Conversion HSMC Schematic		**Development Board Schematic**	
Connector (J1) Pin No.	**Signal Name**	**Signal Name**	**FPGA Pin No.**
145	AIC_LRCIN	HSMB_TX_N15	M9
146	AIC_LRCOUT	HSMB_RX_N15	G4
149	AIC_BCLK	HSMB_TX_P16	N11
150	AIC_XCLK	HSMB_RX_P16	F4
151	AIC_SPI_CS	HSMB_TX_N16	N10
155	FPGA_CLK_B_P	HSMB_CLK_OUT_P2	R12
156	ADA_DCO	HSMB_CLK_IN_P2	U4
157	FPGA_CLK_B_N	HSMB_CLK_OUT_N2	T11
158	ADB_DCO	HSMB_CLK_IN_N2	U3

Appendix C. Pinouts for the Cyclone III (3C25) Starter Board

Introduction

The section describes the HSMC port interface pinout for the Cyclone III (3C25) Starter board. See Table C–1

Table C–1. HSMC Port Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
33	SDA	HSMC_SDA	E1
34	SCL	HSMC_SCL	F3
41	ADA_D13	HSMC_D0	H6
42	ADB_D13	HSMC_D1	D3
43	ADA_D12	HSMC_D2	M5
44	ADB_D12	HSMC_D3	L6
47	ADA_D11	HSMC_D4	M5
48	ADB_D11	HSMC_D5	M3
49	ADA_D10	HSMC_D6	N7
50	ADB_D10	HSMC_D7	T2
53	ADA_D9	HSMC_D8	N8
54	ADB_D9	HSMC_D9	H15
55	ADA_D8	HSMC_D10	J13
56	ADB_D8	HSMC_D11	H16
59	ADA_D7	HSMC_D12	N10
60	ADB_D7	HSMC_D13	N16
61	ADA_D6	HSMC_D14	N11
62	ADB_D6	HSMC_D15	N15
65	ADA_D5	HSMC_D16	K17
66	ADB_D5	HSMC_D17	R16
67	ADA_D4	HSMC_D18	P11

Table C–1. HSMC Port Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
68	ADB_D4	HSMC_D19	T16
71	ADA_D3	HSMC_TX_p4	B2
72	ADB_D3	HSMC_RX_p4	C2
73	ADA_D2	HSMC_TX_n4	B1
74	ADB_D2	HSMC_RX_n4	C1
77	ADA_D1	HSMC_TX_p5	G2
78	ADB_D1	HSMC_RX_p5	H2
79	ADA_D0	HSMC_TX_n5	G1
80	ADB_D0	HSMC_RX_n5	H1
83	ADA_OR	HSMC_TX_p6	K2
84	ADB_OR	HSMC_RX_p6	K5
85	ADA_OE	HSMC_TX_n6	K1
86	ADB_OE	HSMC_RX_n6	L5
89	ADA_SPI_CS	HSMC_TX_p7	L2
90	ADB_SPI_CS	HSMC_RX_p7	L4
91	AD_SDIO	HSMC_TX_n7	L1
92	AD_SCLK	HSMC_RX_n7	L3
95	FPGA_CLK_A_P	HSMC_CLKOUT_p1	D14
96	XT_IN_P	HSMC_CLKIN_p1	F17
97	FPGA_CLK_A_N	HSMC_CLKOUT_n1	C14
98	XT_IN_N	HSMC_CLKIN_n1	F18
101	DA13	HSMC_TX_p8	M2
102	DB13	HSMC_RX_p8	P2
103	DA12	HSMC_TX_n8	M1
104	DB12	HSMC_RX_n8	P1
107	DA11	HSMC_TX_p9	R2
108	DB11	HSMC_RX_p9	T3
109	DA10	HSMC_TX_n9	R1

Table C–1. HSMC Port Interface Pinout			
Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	Signal Name	Signal Name	FPGA Pin No.
110	DB10	HSMC_RX_n9	R3
113	DA9	HSMC_TX_p10	E17
114	DB9	HSMC_RX_p10	G17
115	DA8	HSMC_TX_n10	E18
116	DB8	HSMC_RX_n10	G18
119	DA7	HSMC_TX_p11	H17
120	DB7	HSMC_RX_p11	K18
121	DA6	HSMC_TX_n11	H18
122	DB6	HSMC_RX_n11	L18
125	DA5	HSMC_TX_p12	L17
126	DB5	HSMC_RX_p12	L16
127	DA4	HSMC_TX_n12	M18
128	DB4	HSMC_RX_n12	M17
131	DA3	HSMC_TX_p13	L14
132	DB3	HSMC_RX_p13	L13
133	DA2	HSMC_TX_n13	L15
134	DB2	HSMC_RX_n13	M14
137	DA1	HSMC_TX_p14	P17
138	DB1	HSMC_RX_p14	R17
139	DA0	HSMC_TX_n14	P18
140	DB0	HSMC_RX_n14	R18
143	AIC_DIN	HSMC_TX_p15	R5
144	AIC_DOUT	HSMC_RX_p15	M6
145	AIC_LRCIN	HSMC_TX_n15	R4
146	AIC_LRCOUT	HSMC_RX_n15	N6
149	AIC_BCLK	HSMC_TX_p16	T17
150	AIC_XCLK	HSMC_RX_p16	M13
151	AIC_SPI_CS	HSMC_TX_n16	T18

Table C–1. HSMC Port Interface Pinout

Data Conversion HSMC Schematic		Development Board Schematic	
Connector (J1) Pin No.	**Signal Name**	**Signal Name**	**FPGA Pin No.**
155	FPGA_CLK_B_P	HSMC_CLKOUT_p2	U18
156	ADA_DCO	HSMC_CLKIN_p2	N17
157	FPGA_CLK_B_N	HSMC_CLKOUT_n2	V18
158	ADB_DCO	HSMC_CLKIN_n2	N18

Additional Information

Revision History

The table below displays the revision history for the chapters of the manual.

Chapter	Date	Version	Changes Made
All	March 2008	1.0.0	• First publication.

How to Contact Altera

For the most up-to-date information about Altera® products, refer to the following table.

Information Type	Contact *Note (1)*
Technical support	www.altera.com/mysupport/
Technical training	www.altera.com/training/
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Product literature services	literature@altera.com
FTP site	ftp.altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*

Visual Cue	Meaning
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>*.**pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
WARNING	A warning calls attention to a condition or possible situation that can cause injury to the user.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.