ATF-541M4

Low Noise Enhancement Mode Pseudomorphic HEMT in a Miniature Leadless Package

Data Sheet

Description

Avago Technologies' ATF-541M4 is a high linearity, low noise, single supply E-PHEMT housed in a miniature leadless package.

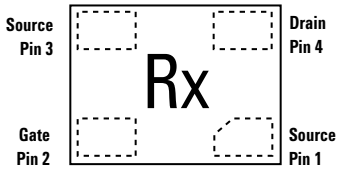
The ATF-541M4's small size and low profile makes it ideal for the design of hybrid module and other space-constraint devices.

The device can be used in applications such as TMA and front end LNA for Cellular/PCS and WCDMA base stations, LNA and driver amplifiers for Wireless Data and 802.11b WLAN.

In addition, the device's superior RF performance at higher frequency makes it an ideal candidate for high frequency applications such as WLL, 802.11a WLAN, 5–6 GHz UNII and HIPERLAN applications.

MiniPak 1.4 mm x 1.2 mm Package

Pin Connections and Package Marking



Note:
Top View. Package marking provides orientation, product identification and date code.

"R" = Device Type Code
"x" = Date code character. A different character is assigned for each month and year.

Features

- High linearity performance
- Single Supply Enhancement Mode Technology[1]
- Very low noise figure
- Excellent uniformity in product specifications
- 800 micron gate width
- Miniature leadless package
  1.4 mm x 1.2 mm x 0.7 mm
- Tape-and-Reel packaging option available

Specifications

2 GHz; 3 V, 60 mA (Typ.)

- 35.8 dBm output 3rd order intercept
- 21.4 dBm output power at 1 dB gain compression
- 0.5 dB noise figure
- 17.5 dB associated gain

Applications

- Low Noise Amplifier and Driver Amplifier for Cellular/PCS and WCDMA Base Stations
- LNA and Driver Amplifier for WLAN, WLL/RLL and MMDS applications
- General purpose discrete E-PHEMT for ultra low noise applications in the 450 MHz to 10 GHz frequency range

Note:

1. Enhancement mode technology requires positive Vgs, thereby eliminating the need for the negative gate voltage associated with conventional depletion mode devices.

ATF-541M4 Absolute Maximum Ratings [1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain-Source Voltage [2]	V	5
V_{GS}	Gate-Source Voltage [2]	V	-5 to +1
V_{GD}	Gate Drain Voltage [2]	V	5
I_{DS}	Drain Current [2]	mA	120
I_{GS}	Gate Current [5]	mA	2
P_{diss}	Total Power Dissipation [3]	mW	360
$P_{in\ max.}$	RF Input Power [5]	dBm	20
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{jc}	Thermal Resistance [4]	°C/W	212

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. Source lead temperature is 25°C. Derate 4.7 mW/°C for $T_L > 74$°C.
4. Thermal resistance measured using 150°C Liquid Crystal Measurement method.
5. The device can handle +20 dBm RF Input Power provided I_{GS} is limited to 2 mA. I_{GS} at P_{1dB} drive level is bias circuit dependent. See applications section for additional information.

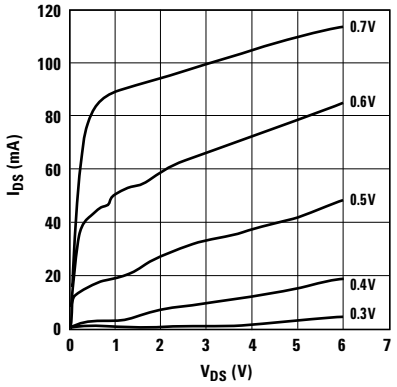


Figure 1. Typical I-V Curves. (V_{GS} = 0.1 V per step)

Product Consistency Distribution Charts [6, 7]

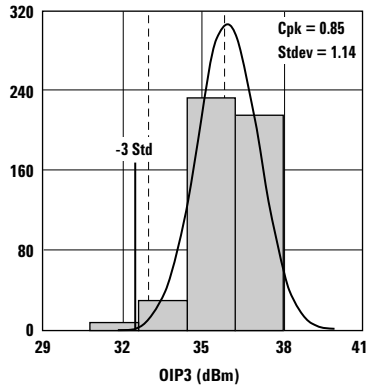


Figure 2. OIP3 @ 2 GHz, 3 V, 60 mA. LSL = 33.0, Nominal = 35.82

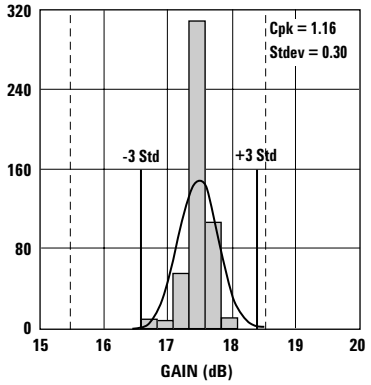


Figure 3. Gain @ 2 GHz, 3 V, 60 mA. LSL = 15.5, Nominal = 17.5, USL = 18.5

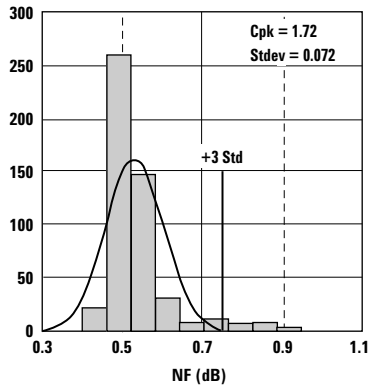


Figure 4. NF @ 2 GHz, 3 V, 60 mA. Nominal = 0.5, USL = 0.9

Notes:

6. Distribution data sample size is 500 samples taken from 6 different wafers. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
7. Measurements made on production test board. This circuit represents a trade-off between an optimal noise match and a realizeable match based on production test equipment. Circuit losses have been de-embedded from actual measurements.

ATF-541M4 Electrical Specifications

T_A = 25°C, RF parameters measured in a test circuit for a typical device

Symbol	Parameter and Test Condition			Units	Min.	Typ.	Max.
Vgs	Operational Gate Voltage		Vds = 3V, Ids = 60 mA	V	0.4	0.58	0.75
Vth	Threshold Voltage		Vds = 3V, Ids = 4 mA	V	0.18	0.36	0.52
Idss	Saturated Drain Current		Vds = 3V, Vgs = 0V	µA	—	0.28	5
Gm	Transconductance		Vds = 3V, gm = ΔIdss/ΔVgs; ΔVgs = 0.75 – 0.7 = 0.05V	mmho	230	398	560
Igss	Gate Leakage Current		Vgd = Vgs = -3V	µA	—	—	200
NF	Noise Figure [1]	f = 2 GHz	Vds = 3V, Ids = 60 mA	dB	—	0.5	0.9
			Vds = 4V, Ids = 60 mA	dB	—	0.5	—
Gain	Gain[1]	f = 2 GHz	Vds = 3V, Ids = 60 mA	dB	15.5	17.5	18.5
			Vds = 4V, Ids = 60 mA	dB	—	18.1	—
OIP3	Output 3rd Order Intercept Point[1]	f = 2 GHz	Vds = 3V, Ids = 60 mA	dBm	33	35.8	—
			Vds = 4V, Ids = 60 mA	dBm	—	35.9	—
P1dB	1dB Compressed Output Power[1]	f = 2 GHz	Vds = 3V, Ids = 60 mA	dBm	—	21.4	—
			Vds = 4V, Ids = 60 mA	dBm	—	22.1	—

Notes:

1. Measurements obtained using production test board described in Figure 5.

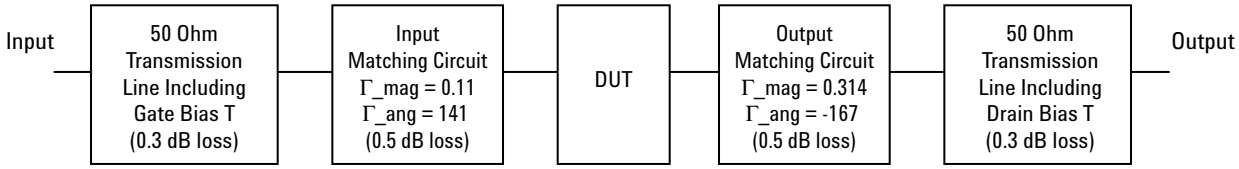


Figure 5. Block diagram of 2 GHz production test board used for Noise Figure, Gain, P1dB, OIP3, and OIP3 measurements. This circuit represents a trade-off between an optimal noise match, maximum OIP3 match and associated impedance matching circuit losses. Circuit losses have been de-embedded from actual measurements.

Symbol	Parameter and Test Condition			Units	Min.	Typ.	Max.
Fmin	Minimum Noise Figure [2]	f = 900 GHz	Vds = 3V, Ids = 60 mA	dB	—	0.16	—
		f = 2 GHz	Vds = 3V, Ids = 60 mA	dB	—	0.46	—
		f = 3.9 GHz	Vds = 3V, Ids = 60 mA	dB	—	0.8	—
		f = 5.8 GHz	Vds = 3V, Ids = 60 mA	dB	—	1.17	—
Ga	Associated Gain[2]	f = 900 GHz	Vds = 3V, Ids = 60 mA	dB	—	22.4	—
		f = 2 GHz	Vds = 3V, Ids = 60 mA	dB	—	18.7	—
		f = 3.9 GHz	Vds = 3V, Ids = 60 mA	dB	—	14.5	—
		f = 5.8 GHz	Vds = 3V, Ids = 60 mA	dB	—	11.9	—
OIP3	Output 3rd Order Intercept Point[3]	f = 900 GHz	Vds = 3V, Ids = 60 mA	dBm	—	35	—
			Vds = 4V, Ids = 60 mA	dBm	—	35.1	—
		f = 3.9 GHz	Vds = 3V, Ids = 60 mA	dB	—	36.6	—
		f = 5.8 GHz	Vds = 3V, Ids = 60 mA	dB	—	37.6	—
P1dB	1dB Compressed Output Power[3]	f = 900 GHz	Vds = 3V, Ids = 60 mA	dBm	—	19.5	—
			Vds = 4V, Ids = 60 mA	dBm	—	20.8	—
		f = 3.9 GHz	Vds = 3V, Ids = 60 mA	dB	—	20.4	—
		f = 5.8 GHz	Vds = 3V, Ids = 60 mA	dB	—	19.4	—

Notes:

2. Fmin and associated gain at minimum noise figure (Ga) values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true Fmin and Ga is calculated. Refer to the noise parameter application section for more information.
3. P_{1dB} and OIP3 measurements made in an InterContinental Microwave (ICM) test fixture with double stub tuners and bias tees. The input was tuned for minimum noise figure and the output was tuned for maximum OIP3.

ATF-541M4 Typical Performance Curves

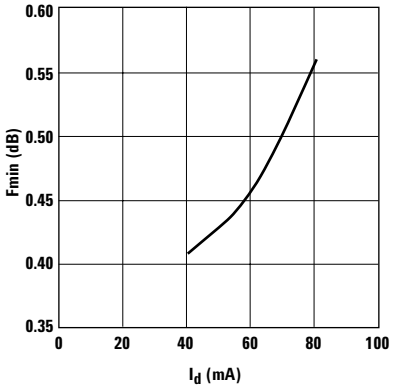


Figure 6. Fmin vs. I_{ds} at 2 GHz, V_{ds} = 3V[1]

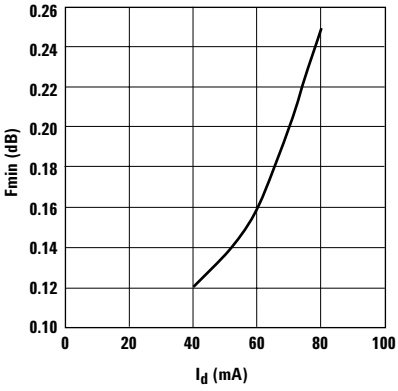


Figure 7. Fmin vs. I_{ds} at 900 MHz, V_{ds} = 3V[1]

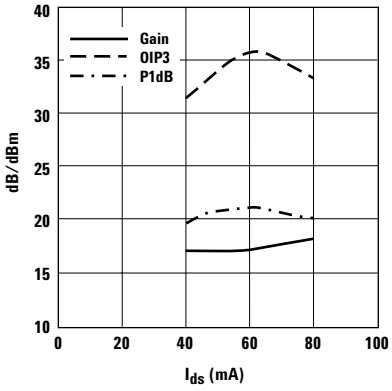


Figure 8. Gain, OIP3 & P1dB vs. I_{ds} Tuned for Max OIP3 and Min NF at 2 GHz, V_{ds} = 3V[2].

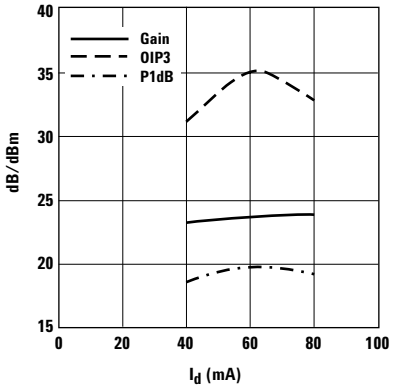


Figure 9. Gain, OIP3 & P1dB vs. I_{ds} Tuned for Max OIP3 and Min NF at 900 MHz, V_{ds} = 3V[3].

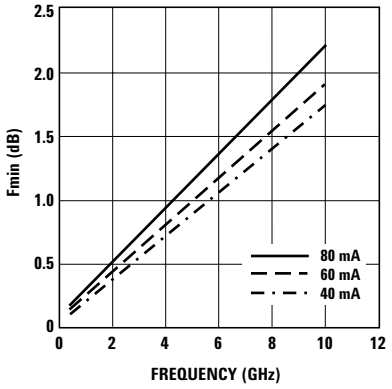


Figure 10. Fmin vs. Frequency vs. I_{ds}, V_{ds} = 3V[1].

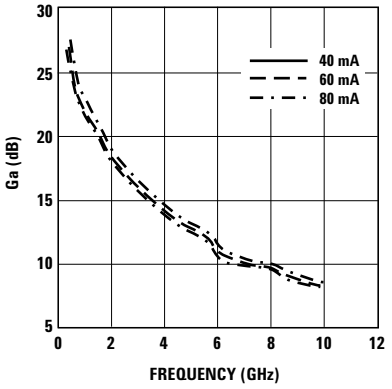


Figure 11. Ga vs. Frequency vs. I_{ds}, V_{ds} = 3V[1].

Notes:

1. Fmin and associated gain at minimum noise figure (Ga) values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true Fmin and Ga is calculated. Refer to the noise parameter application section for more information.
2. Measurements obtained using production test board described in Figure 5.
3. Input tuned for minimum NF and the output tuned for maximum OIP3 using an InterContinental Microwave (ICM) test fixture, double stub tuners and bias tees.

ATF-541M4 Typical Performance Curves, continued

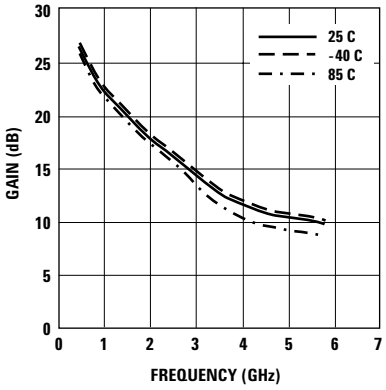


Figure 12. Gain vs. Freq. and Temperature Tuned for Max OIP3 and Min NF at V_{ds} = 3V, I_{ds} = 60 mA[1].

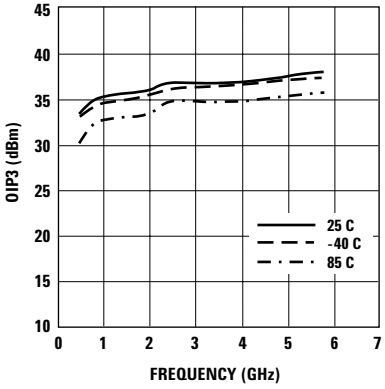


Figure 13. OIP3 vs. Freq. and Temperature Tuned for Max OIP3 and Min NF at V_{ds} = 3V, I_{ds} = 60 mA[1].

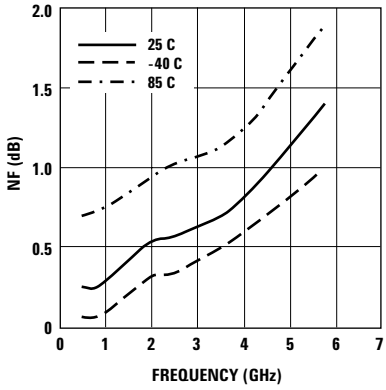


Figure 14. NF vs. Freq. and Temperature Tuned for Max OIP3 and Min NF at V_{ds} = 3V, I_{ds} = 60 mA[1].

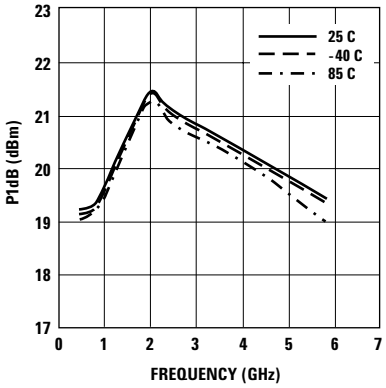


Figure 15. P1dB vs. Freq. and Temperature Tuned for Max OIP3 and Min NF at V_{ds} = 3V, I_{ds} = 60 mA[1].

ATF-541M4 Output Reflection Coefficient Parameters Tuned for Maximum Output IP3[1]; V_{DS} = 3V, I_{DS} = 60 mA

Freq (GHz)	Gamma[2] Out_Mag. (Mag)	Gamma[2] Out_Mag. (Degrees)	OIP3 (dBm)	P1dB (dBm)
0.9	0.006	23	35.04	19.47
2.0	0.314	-167	35.82	21.36
3.9	0.321	134	36.60	20.37
5.8	0.027	89	37.62	19.38

Notes:

1. Input tuned for minimum NF and the output tuned for maximum OIP3 using an InterContinental Microwave (ICM) test fixture, double stub tuners and bias tees.
2. Gamma out is the reflection coefficient of the matching circuit presented to the output of the device.

ATF-541M4 Typical Scattering Parameters, V_{DS} = 3V, I_{DS} = 40 mA

Freq.	S_{11}			S_{21}		S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.99	-16.4	27.62	24.03	169.5	0.01	80.2	0.58	-10.6	33.81
0.5	0.88	-71.2	25.51	18.85	135.7	0.03	54.4	0.46	-45.3	27.98
0.9	0.79	-107.2	22.76	13.74	115.0	0.04	41.2	0.34	-66.5	25.36
1.0	0.77	-114.0	22.07	12.69	110.9	0.04	39.0	0.32	-71.0	25.01
1.5	0.73	-137.2	19.26	9.18	96.1	0.05	32.8	0.23	-87.8	22.64
1.9	0.71	-150.1	17.48	7.48	87.7	0.05	30.4	0.19	-97.9	21.75
2.0	0.70	-155.1	16.94	7.03	86.4	0.05	30.6	0.16	-101.6	21.48
2.5	0.69	-168.4	15.19	5.75	78.3	0.06	29.7	0.13	-113.1	19.82
3.0	0.69	-178.1	13.68	4.83	71.1	0.06	29.5	0.11	-128.4	19.06
4.0	0.69	166.9	11.30	3.67	58.3	0.07	29.3	0.11	-152.9	15.14
5.0	0.70	155.0	9.44	2.96	46.6	0.07	27.9	0.11	-174.7	12.85
6.0	0.71	139.7	8.02	2.52	34.5	0.09	25.1	0.12	173.9	11.68
7.0	0.72	129.2	6.67	2.16	23.9	0.10	22.3	0.13	157.8	10.34
8.0	0.73	119.3	5.54	1.89	13.6	0.11	19.0	0.14	145.8	9.24
9.0	0.74	110.0	4.51	1.68	3.6	0.12	15.1	0.16	135.6	8.31
10.0	0.76	100.3	3.61	1.52	-6.5	0.13	10.5	0.19	124.6	7.74
11.0	0.77	90.5	2.80	1.38	-16.9	0.14	4.8	0.22	113.5	7.01
12.0	0.79	82.1	2.01	1.26	-27.5	0.15	-1.7	0.27	102.7	6.58
13.0	0.81	72.4	1.21	1.15	-37.6	0.16	-8.5	0.32	92.5	6.19
14.0	0.83	62.2	0.37	1.04	-48.8	0.16	-15.9	0.37	83.1	5.73
15.0	0.85	52.3	-0.51	0.94	-59.4	0.17	-24.1	0.44	74.2	5.46
16.0	0.86	42.7	-1.70	0.82	-69.3	0.17	-31.6	0.50	66.0	4.53
17.0	0.89	33.1	-2.59	0.74	-78.2	0.17	-39.0	0.57	60.5	4.93
18.0	0.90	24.5	-3.81	0.65	-86.9	0.17	-45.9	0.62	55.9	4.44

Typical Noise Parameters, V_{DS} = 3V, I_{DS} = 40 mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.10	0.45	8.3	0.06	26.17
0.9	0.12	0.41	11.3	0.06	22.19
1.0	0.17	0.29	23.8	0.05	21.81
1.9	0.40	0.23	89.2	0.05	18.72
2.0	0.41	0.22	89.9	0.05	18.24
2.4	0.51	0.24	112.1	0.05	17.16
3.0	0.55	0.29	140.2	0.05	15.91
3.9	0.64	0.34	165.4	0.04	14.26
5.0	0.95	0.35	-173.4	0.04	12.74
5.8	1.07	0.34	-160.3	0.05	11.72
6.0	1.10	0.40	-151.2	0.08	10.32
7.0	1.30	0.42	-139.3	0.10	9.77
8.0	1.45	0.48	-129.2	0.13	9.46
9.0	1.57	0.55	-118.0	0.21	8.64
10.0	1.69	0.59	-101.7	0.34	8.15

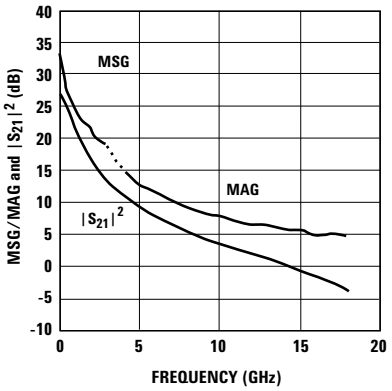


Figure 16. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 3V, 40 mA.

Notes:

1. The Fmin values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true Fmin is calculated. Refer to the noise parameter application section for more information.
2. Refer to the applications section for additional information on the test fixture used for the measurement of the s and noise parameters.

ATF-541M4 Typical Scattering Parameters, V_{DS} = 3V, I_{DS} = 60 mA

Freq.	S_{11}		S_{21}			S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.99	-17.6	28.36	26.18	168.9	0.01	85.1	0.54	-11.3	34.18
0.5	0.87	-74.7	26.04	20.03	133.9	0.03	54.2	0.41	-48.1	28.25
0.9	0.78	-110.7	23.13	14.34	113.5	0.04	41.8	0.30	-70.1	25.54
1.0	0.76	-117.6	22.42	13.22	109.4	0.04	40.2	0.28	-74.9	25.19
1.5	0.72	-140.1	19.54	9.49	95.1	0.05	34.6	0.20	-92.5	22.78
1.9	0.70	-152.6	17.73	7.70	86.9	0.05	32.8	0.17	-103.3	21.88
2.0	0.70	-157.5	17.19	7.24	85.7	0.05	33.5	0.14	-108.9	21.61
2.5	0.69	-170.4	15.45	5.92	77.9	0.05	34.1	0.12	-122.4	20.73
3.0	0.69	-179.9	13.91	4.96	70.8	0.06	33.4	0.10	-138.7	19.17
4.0	0.69	165.7	11.53	3.77	58.3	0.07	32.8	0.10	-164.1	15.26
5.0	0.70	153.8	9.66	3.04	46.8	0.08	32.0	0.09	174.9	13.21
6.0	0.71	138.8	8.25	2.58	34.8	0.09	28.2	0.11	162.9	11.80
7.0	0.71	128.6	6.89	2.21	24.4	0.10	25.1	0.12	149.1	10.30
8.0	0.73	118.6	5.76	1.94	14.3	0.11	21.1	0.14	138.7	9.42
9.0	0.74	109.2	4.72	1.72	4.4	0.12	16.6	0.17	129.5	8.46
10.0	0.76	99.9	3.80	1.55	-5.7	0.13	11.2	0.19	119.3	7.86
11.0	0.77	89.7	3.03	1.42	-16.0	0.14	5.5	0.23	108.8	7.21
12.0	0.79	81.5	2.23	1.29	-26.3	0.15	-1.1	0.27	98.6	6.73
13.0	0.80	71.8	1.45	1.18	-36.3	0.16	-8.7	0.32	89.2	6.11
14.0	0.83	61.7	0.58	1.07	-47.4	0.17	-15.6	0.38	80.3	5.98
15.0	0.85	52.2	-0.31	0.96	-58.1	0.17	-23.4	0.44	71.7	5.54
16.0	0.86	42.1	-1.41	0.85	-67.9	0.17	-31.6	0.49	64.3	4.75
17.0	0.90	33.2	-2.34	0.76	-76.8	0.17	-38.7	0.57	58.8	5.73
18.0	0.90	24.3	-3.53	0.67	-84.8	0.17	-45.8	0.62	54.7	4.51

Typical Noise Parameters, V_{DS} = 3V, I_{DS} = 60 mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.12	0.37	13.2	0.05	27.06
0.9	0.16	0.34	10.9	0.06	22.88
1.0	0.19	0.21	30.8	0.04	22.44
1.9	0.45	0.22	102.9	0.05	19.17
2.0	0.46	0.21	104.2	0.05	18.69
2.4	0.57	0.23	125.2	0.05	17.57
3.0	0.62	0.30	149.0	0.04	16.26
3.9	0.80	0.35	173.1	0.04	14.54
5.0	1.02	0.43	-168.3	0.05	12.97
5.8	1.17	0.46	-155.8	0.06	11.85
6.0	1.22	0.51	-146.4	0.09	10.98
7.0	1.41	0.52	-137.0	0.11	10.03
8.0	1.49	0.54	-129.5	0.15	9.66
9.0	1.69	0.56	-115.1	0.25	8.82
10.0	1.87	0.61	-99.8	0.40	8.32

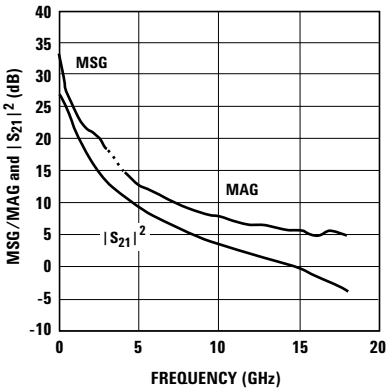


Figure 17. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 3V, 60 mA.

Notes:

1. The Fmin values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true Fmin is calculated. Refer to the noise parameter application section for more information.
2. Refer to the applications section for additional information on the test fixture used for the measurement of the s and noise parameters.

ATF-541M4 Typical Scattering Parameters, V_{DS} = 3V, I_{DS} = 80 mA

Freq.	S_{11}			S_{21}		S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.97	-17.9	28.61	26.94	168.8	0.01	79.8	0.50	-11.6	34.30
0.5	0.85	-76.2	26.21	20.44	133.6	0.03	54.7	0.39	-49.1	28.33
0.9	0.77	-112.1	23.27	14.57	113.2	0.04	43.1	0.28	-71.5	25.61
1.0	0.75	-119.2	22.55	13.42	109.1	0.04	41.5	0.26	-76.4	25.26
1.5	0.71	-142.2	19.65	9.60	95.0	0.04	36.3	0.19	-94.6	23.80
1.9	0.70	-154.9	17.83	7.79	86.9	0.05	34.8	0.16	-105.8	21.93
2.0	0.69	-159.5	17.30	7.33	85.8	0.05	35.8	0.13	-112.9	21.66
2.5	0.69	-171.1	15.53	5.98	78.0	0.05	36.0	0.11	-127.2	20.78
3.0	0.69	179.5	14.00	5.01	71.0	0.06	35.8	0.10	-144.2	19.22
4.0	0.69	165.2	11.62	3.81	58.5	0.06	35.0	0.10	-170.0	14.97
5.0	0.70	153.3	9.75	3.07	47.2	0.07	33.7	0.10	168.7	13.05
6.0	0.70	138.3	8.33	2.61	35.3	0.09	29.6	0.11	156.1	11.67
7.0	0.72	127.8	6.97	2.23	25.0	0.10	26.6	0.12	143.5	10.52
8.0	0.73	118.0	5.84	1.96	14.8	0.11	22.3	0.14	133.6	9.47
9.0	0.74	109.1	4.82	1.74	5.2	0.12	17.8	0.17	125.1	8.52
10.0	0.76	99.3	3.89	1.56	-4.9	0.13	12.1	0.19	115.7	7.88
11.0	0.76	89.7	3.11	1.43	-15.1	0.14	6.1	0.23	105.6	7.03
12.0	0.79	80.9	2.29	1.30	-25.2	0.15	-0.4	0.27	95.7	6.75
13.0	0.80	71.9	1.56	1.20	-35.3	0.16	-7.8	0.32	86.7	6.21
14.0	0.83	61.8	0.73	1.09	-46.6	0.17	-15.0	0.37	78.3	6.12
15.0	0.85	52.1	-0.18	0.98	-56.2	0.17	-23.3	0.44	70.0	5.66
16.0	0.86	41.6	-1.22	0.87	-67.1	0.17	-31.0	0.49	63.1	4.89
17.0	0.89	32.9	-2.18	0.78	-75.9	0.17	-39.1	0.57	57.7	5.21
18.0	0.89	24.3	-3.36	0.68	-83.6	0.17	-45.5	0.62	53.6	4.07

Typical Noise Parameters, V_{DS} = 3V, I_{DS} = 80 mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.21	0.23	24.4	0.05	27.83
0.9	0.25	0.20	17.8	0.06	23.58
1.0	0.28	0.11	60.8	0.04	23.43
1.9	0.53	0.21	121.1	0.05	19.57
2.0	0.56	0.20	124.5	0.05	19.13
2.4	0.64	0.26	142.6	0.05	18.05
3.0	0.72	0.32	159.7	0.05	16.60
3.9	0.81	0.38	179.2	0.05	14.81
5.0	1.03	0.41	-153.7	0.05	13.21
5.8	1.33	0.42	-152.5	0.07	12.20
6.0	1.40	0.46	-143.4	0.10	11.35
7.0	1.59	0.47	-139.1	0.13	10.24
8.0	1.79	0.53	-127.3	0.19	9.84
9.0	2.01	0.59	-113.4	0.31	9.00
10.0	2.20	0.63	-97.9	0.5	8.46

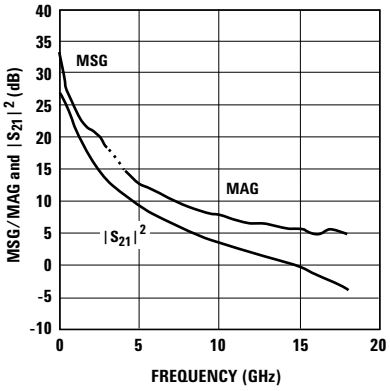


Figure 18. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 3V, 80 mA.

Notes:

1. The Fmin values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true Fmin is calculated. Refer to the noise parameter application section for more information.
2. Refer to the applications section for additional information on the test fixture used for the measurement of the s and noise parameters.

ATF-541M4 Typical Scattering Parameters, V_{DS} = 4V, I_{DS} = 60 mA

Freq.	S_{11}			S_{21}		S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.99	-17.5	28.39	26.27	168.9	0.01	81.0	0.56	-10.7	34.19
0.5	0.87	-74.8	26.07	20.12	133.9	0.03	54.5	0.44	-44.7	28.27
0.9	0.78	-110.7	23.18	14.42	113.6	0.04	41.6	0.32	-64.3	25.57
1.0	0.76	-117.5	22.47	13.29	109.4	0.04	39.4	0.29	-68.3	25.21
1.5	0.72	-141.4	19.60	9.55	95.1	0.04	35.2	0.21	-82.7	23.78
1.9	0.70	-154.3	17.79	7.75	86.9	0.05	33.3	0.18	-91.2	21.90
2.0	0.69	-159.0	17.25	7.29	85.6	0.05	33.7	0.14	-93.8	21.64
2.5	0.69	-170.1	15.50	5.96	77.7	0.051	34.2	0.11	-103.7	20.68
3.0	0.69	-179.6	13.98	5.00	70.6	0.05	33.1	0.10	-117.7	17.98
4.0	0.69	165.9	11.60	3.80	57.9	0.06	33.2	0.09	-141.7	15.13
5.0	0.70	153.9	9.72	3.06	46.4	0.07	32.4	0.09	-166.9	13.17
6.0	0.70	138.8	8.31	2.60	34.4	0.08	29.5	0.10	-175.8	11.68
7.0	0.72	128.6	6.96	2.23	23.9	0.09	26.4	0.12	163.3	10.53
8.0	0.73	118.8	5.82	1.95	13.5	0.10	22.7	0.13	149.1	9.44
9.0	0.75	109.5	4.80	1.74	3.6	0.11	18.2	0.14	138.2	8.76
10.0	0.76	99.9	3.89	1.56	-6.6	0.13	13.4	0.17	126.7	8.01
11.0	0.77	90.1	3.07	1.42	-17.1	0.14	7.2	0.20	114.9	7.30
12.0	0.79	81.5	2.27	1.30	-27.6	0.15	0.6	0.24	103.7	6.91
13.0	0.81	71.6	1.47	1.19	-37.8	0.16	-6.5	0.29	93.3	6.54
14.0	0.83	62.2	0.68	1.08	-48.9	0.17	-13.9	0.35	84.3	6.22
15.0	0.85	51.9	-0.28	0.97	-59.6	0.17	-21.7	0.42	75.0	5.73
16.0	0.87	42.1	-1.39	0.85	-69.7	0.17	-29.9	0.48	67.0	5.20
17.0	0.90	32.7	-2.28	0.77	-78.7	0.18	-37.8	0.55	61.1	6.31
18.0	0.90	24.2	-3.52	0.67	-87.4	0.17	-44.8	0.61	56.4	5.96

Typical Noise Parameters, V_{DS} = 4V, I_{DS} = 60 mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.13	0.36	14.2	0.05	27.18
0.9	0.16	0.35	13.3	0.06	22.95
1.0	0.20	0.22	33.7	0.05	22.51
1.9	0.45	0.22	101.6	0.05	19.14
2.0	0.47	0.20	102.7	0.06	18.66
2.4	0.57	0.24	126.0	0.05	17.61
3.0	0.63	0.29	148.9	0.05	16.26
3.9	0.73	0.35	172.3	0.04	14.58
5.0	1.05	0.37	-168.4	0.05	13.04
5.8	1.21	0.38	-155.9	0.06	12.01
6.0	1.23	0.41	-151.0	0.08	11.05
7.0	1.43	0.45	-139.9	0.11	10.11
8.0	1.61	0.51	-129.9	0.15	9.76
9.0	1.80	0.57	-114.8	0.26	8.95
10.0	2.01	0.61	-99.2	0.41	8.44

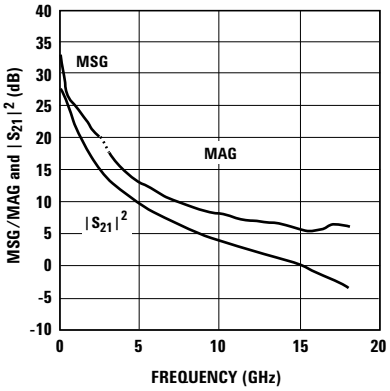


Figure 19. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 4V, 60 mA.

Notes:

1. The Fmin values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true Fmin is calculated. Refer to the noise parameter application section for more information.
2. Refer to the applications section for additional information on the test fixture used for the measurement of the s and noise parameters.

S and Noise Parameter Measurements

The position of the reference planes used for the measurement of both S and Noise Parameter measurements is shown in Figure 20. The reference plane can be described as being at the center of both the gate and drain pads.

S and noise parameters are measured with a 50 ohm microstrip test fixture made with a 0.010" thickness aluminum substrate. Both source leads are connected directly to ground via a 0.010" thickness metal rib which provides a very low inductance path to ground for both source leads. The inductance associated with the addition of printed circuit board plated through holes and source bypass capacitors must be added to the computer circuit simulation to properly model the effect of grounding the source leads in a typical amplifier design.

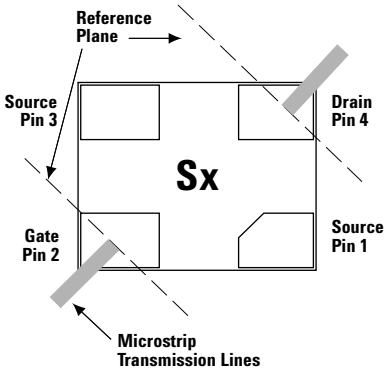


Figure 20.

Noise Parameter Applications Information

The Fmin values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements, a true Fmin is calculated. Fmin represents the true minimum noise figure of the device when the device is presented with an impedance matching network that transforms the source impedance, typically 50Ω, to an impedance represented by the reflection coefficient Γ_o. The designer must design a matching network that will present Γ_o to the device with minimal associated circuit losses. The noise figure of the completed amplifier is equal to the noise figure of the device plus the losses of the matching network preceding the device. The noise figure of the device is equal to Fmin only when the device is presented with Γ_o. If the reflection coefficient of the matching network is other than Γ_o, then the noise figure of the device will be greater than Fmin based on the following equation.

$$NF = F_{min} + \frac{4 R_n}{Zo} \frac{|\Gamma_s - \Gamma_o|^2}{(|1 + \Gamma_o|^2)(1 - |\Gamma_s|^2)}$$

Where Rn/Zo is the normalized noise resistance, Γ_o is the optimum reflection coefficient required to produce Fmin and Γ_s is the reflection coefficient of the source impedance actually presented to the device.

The losses of the matching networks are non-zero and they will also add to the noise figure of the device creating a higher amplifier noise figure. The losses of the matching networks are related to the Q of the components and associated printed circuit board loss. Γ_o is typically fairly low at higher frequencies and increases as frequency is lowered. Larger gate width devices will typically have a lower Γ_o as compared to narrower gate width devices. Typically for FETs , the higher Γ_o usually infers that an impedance much higher than 50Ω is required for the device to produce Fmin. At VHF frequencies and even lower L Band frequencies, the required impedance can be in the vicinity of several thousand ohms. Matching to such a high impedance requires very hi-Q components in order to minimize circuit losses. As an example at 900 MHz, when airwwound coils (Q>100)are used for matching networks, the loss can still be up to 0.25 dB which will add directly to the noise figure of the device. Using muiltilayer molded inductors with Qs in the 30 to 50 range results in additional loss over the airwound coil. Losses as high as 0.5 dB or greater add to the typical 0.15 dB Fmin of the device creating an amplifier noise figure of nearly 0.65 dB.

SMT Assembly

The package can be soldered using either lead-bearing or lead-free alloys (higher peak temperatures). Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g. IR or vapor phase reflow, wave soldering, etc) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the Minipak 1412 package, will reach solder reflow temperatures faster than those with a greater mass.

The recommended leaded solder time-temperature profile is shown in Figure 21. This profile is representative of an IR reflow type of surface mount assembly process. After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of board or damage to components due to thermal shock. The maximum temperature in the reflow zone (Tmax) should not exceed 235°C for leaded solder.

These parameters are typical for a surface mount assembly process for the ATF-541M4. As a general guideline, the circuit board and components should only be exposed to the minimum temperatures and times the necessary to achieve a uniform reflow of solder.

The recommended lead-free reflow profile is shown in Figure 22.

Electrostatic Sensitivity

FETs and RFICs are electrostatic discharge (ESD) sensitive devices. Avago devices are manufactured using a very robust and reliable PHEMT process, however, permanent damage may occur to these devices if they are subjected to high-energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without detection and may result in failure or degradation in performance and reliability.

Electronic devices may be subjected to ESD damage in any of the following areas:

- Storage & handling
- Inspection
- Assembly & testing
- In-circuit use

The ATF-541M4 is an ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, testing, and assembling these devices to avoid damage.

Any user-accessible points in wireless equipment (e.g. antenna or battery terminals) provide an opportunity for ESD damage.

For circuit applications in which the ATF-541M4 is used as an input or output stage with close coupling to an external antenna, the device should be protected from high voltage spikes due to human contact with the antenna. A good practice, illustrated in Figure 23, is to place a shunt inductor or RF choke at the antenna connection to protect the receiver and transmitter circuits. It is often advantageous to integrate the RF choke into the design of the diplexer or T/R switch control circuitry.

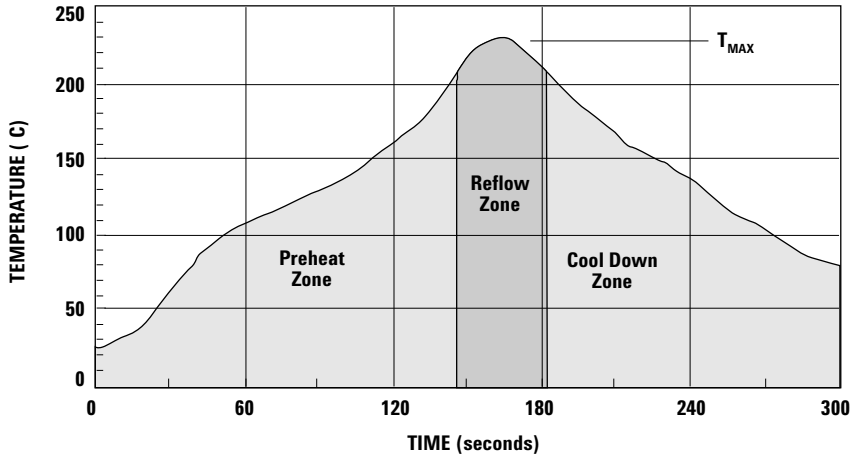


Figure 21. Leaded Solder Reflow Profile.

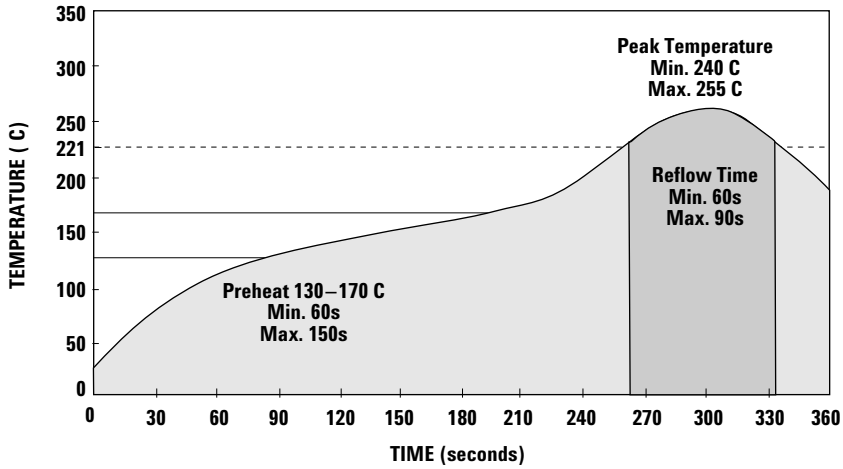


Figure 22. Lead-free Solder Reflow Profile.

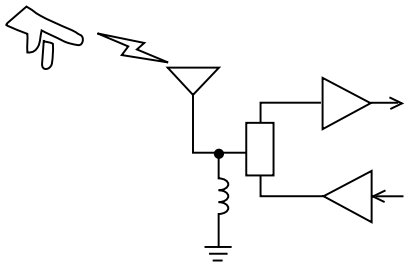


Figure 23. In-circuit ESD Protection.

ATF-541M4 Applications Information

Introduction

Avago Technologies's ATF-541M4 is a low noise enhancement mode PHEMT designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. As opposed to a typical depletion mode PHEMT where the gate must be made negative with respect to the source for proper operation, an enhancement mode PHEMT requires that the gate be made more positive than the source for normal operation. Therefore a negative power supply voltage is not required for an enhancement mode device. Biasing an enhancement mode PHEMT is much like biasing the typical bipolar junction transistor. Instead of a 0.7V base to emitter voltage, the ATF-541M4 enhancement mode PHEMT requires a nominal 0.58V potential between the gate and source for a nominal drain current of 60 mA.

Matching Networks

The techniques for impedance matching an enhancement mode device are very similar to those for matching a depletion mode device. The only difference is in the method of supplying gate bias. S and Noise Parameters for various bias conditions are listed in this data sheet. The circuit shown in Figure 1 shows a typical LNA circuit normally used for 900 and 1900 MHz applications. (Consult the Avago Technologies web site for application notes covering specific designs and applications). High pass impedance matching networks consisting of L1/C1 and L4/C4 provide the appropriate match for noise figure, gain, S11 and S22. The high pass structure also provides low frequency gain reduction which can be beneficial from the standpoint of improving out-of-band rejection.

Capacitors C2 and C5 provide a low impedance in-band RF bypass for the matching networks. Resistors R3 and R4 provide a very important low frequency termination for the device. The resistive termination improves low frequency stability. Capacitors C3 and C6 provide the RF bypass for resistors R3 and R4. Their value should be chosen carefully as C3 and C6 also provide a termination for low frequency mixing products. These mixing products are as a result of two or more in-band signals mixing and producing third order in-band distortion products. The low frequency or difference mixing products are terminated by C3 and C6. For best suppression of third order distortion products based on the CDMA 1.25 MHz signal spacing, C3 and C6 should be 0.1 uF in value. Smaller values of capacitance will not suppress the generation of the 1.25 MHz difference signal and as a result will show up as poorer two tone IP3 results.

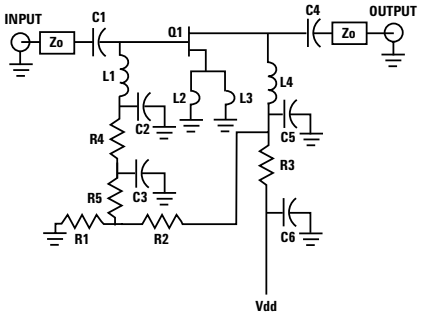


Figure 1. Typical ATF-541M4 LNA with Passive Biasing.

Bias Networks

One of the major advantages of the enhancement mode technology is that it allows the designer to be able to dc ground the source leads and then merely apply a positive voltage on the gate to set the desired amount of quiescent drain current Id.

Whereas a depletion mode PHEMT pulls maximum drain current when $V_{gs} = 0V$, an enhancement mode PHEMT pulls only a small amount of leakage current when $V_{gs} = 0V$. Only when V_{gs} is increased above V_{to}, the device threshold voltage, will drain current start to flow. At a V_{ds} of 3V and a nominal V_{gs} of 0.58V, the drain current I_d will be approximately 60 mA. The data sheet suggests a minimum and maximum V_{gs} over which the desired amount of drain current will be achieved. It is also important to note that if the gate terminal is left open circuited, the device will pull some amount of drain current due to leakage current creating a voltage differential between the gate and source terminals.

Passive Biasing

Passive biasing of the ATF-541M4 is accomplished by the use of a voltage divider consisting of R1 and R2 connected to the gate of the device. The voltage for the divider is derived from the drain voltage. This provides a form of voltage feedback (through the use of R3) to help keep drain current constant. Resistor R5 (approximately 10KΩ) is added to limit the gate current of enhancement mode devices such as the ATF-541M4. This is especially important when the device is driven to P1dB or Psat.

Resistor R3 is calculated based on desired V_{ds}, I_{ds} and available power supply voltage.

$$R3 = \frac{V_{DD} - V_{ds}}{I_{ds} + I_{BB}} \quad (1)$$

V_{DD} is the power supply voltage.
V_{ds} is the device drain to source voltage.
I_{ds} is the desired drain current.
I_{BB} is the current flowing through the R1/R2 resistor voltage divider network.

The value of resistors R1 and R2 are calculated with the following formulas

$$R1 = \frac{V_{gs}}{I_{BB}} \quad (2)$$

$$R2 = \frac{(V_{ds} - V_{gs})\,R1}{V_{gs}} \quad (3)$$

Example Circuit

$V_{DD} = 5\,V$
$V_{ds} = 3V$
$I_{ds} = 60\ mA$
$V_{gs} = 0.58\,V$

Choose I_{BB} to be at least 10X the maximum expected gate leakage current. I_{BB} was chosen to be 2 mA for this example. Using equations (1), (2), and (3) the resistors are calculated as follows

$R1 = 290\Omega$
$R2 = 1210\Omega$
$R3 = 32.3\Omega$

Active Bias

Active biasing provides a means of keeping the quiescent bias point constant over temperature and constant over lot to lot variations in device dc performance. The advantage of the active biasing of an enhancement mode PHEMT versus a depletion mode PHEMT is that a negative power source is not required. The techniques of active biasing an enhancement mode device are very similar to those used to bias a bipolar junction transistor.

An active bias scheme is shown in Figure 2.

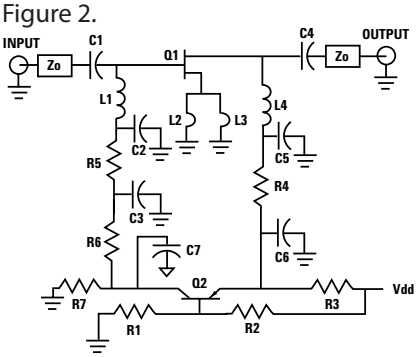


Figure 2. Typical ATF-541M4 LNA with Active Biasing.

R1 and R2 provide a constant voltage source at the base of a PNP transistor at Q2. The constant voltage at the base of Q2 is raised by 0.7 volts at the emitter. The constant emitter voltage plus the regulated V_{DD} supply are present across resistor R3. Constant voltage across R3 provides a constant current supply for the drain current. Resistors R1 and R2 are used to set the desired V_{ds}. The combined series value of these resistors also sets the amount of extra current consumed by the bias network. The equations that describe the circuit's operation are as follows.

$$V_E = V_{ds} + (I_{ds} \cdot R4) \quad (1)$$

$$R3 = \frac{V_{DD} - V_E}{I_{ds}} \quad (2)$$

$$V_B = V_E - V_{BE} \quad (3)$$

$$V_B = \frac{R1}{R1 + R2}\,V_{DD} \quad (4)$$

$$V_{DD} = I_{BB}\,(R1 + R2) \quad (5)$$

Rearranging equation (4) provides the following formula

$$R2 = \frac{R_1\,(V_{DD} - V_B)}{V_B} \quad (4A)$$

and rearranging equation (5) provides the follow formula

$$R1 = \frac{V_{DD}}{I_{BB}\left(1 + \frac{V_{DD} - V_B}{V_{B.}}\right)} \quad (5A)$$

Example Circuit

$V_{DD} = 5\,V$
$V_{ds} = 3V$
$I_{ds} = 60\ mA$
$R4 = 10\Omega$
$V_{BE} = 0.7\,V$

Equation (1) calculates the required voltage at the emitter of the PNP transistor based on desired V_{ds} and I_{ds} through resistor R4 to be 3.6V. Equation (2) calculates the value of resistor R3 which determines the drain current I_{ds}. In the example R3=23.3Ω. Equation (3) calculates the voltage required at the junction of resistors R1 and R2. This voltage plus the step-up of the base emitter junction determines the regulated V_{ds}. Equations (4) and (5) are solved simultaneously to determine the value of resistors R1 and R2. In the example R1=1450Ω and R2 =1050Ω. Resistor R7 is chosen to be 1 kΩ. This resistor keeps a small amount of current flowing through Q2 to help maintain bias stability. R6 is chosen to be 10 KΩ. This value of resistance is high enough to limit Q1 gate current in the presence of high RF drive levels as experienced when Q1 is driven to the P1dB gain compression point. C7 provides a low frequency bypass to keep noise from Q2 effecting the operation of Q1. C7 is typically 0.1 µF.

Maximum Suggested Gate Current

The maximum suggested gate current for the ATF-541M4 is 2 mA. Incorporating resistor R5 in the passive bias network or resistor R6 in the active bias network safely limits gate current to 500 µA at P1dB drive levels. In order to minimize component count in the passive biased amplifier circuit, the 3 resistor bias circuit consisting of R1, R2, and R5 can be simplified if desired. R5 can be removed if R1 is replaced with a 4.7KΩ resistor and if R2 is replaced with a 27KΩ resistor. This combination should limit gate current to a safe level.

PCB Layout

A suggested PCB pad print for the miniature, Minipak 1412 package used by the ATF-541M4 is shown in Figure 3.

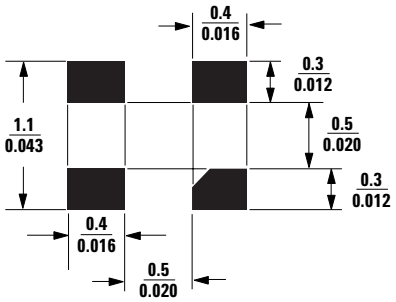


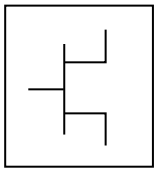
Figure 3. PCB Pad Print for Minipak 1412. Package (mm [inches]).

This pad print provides allowance for package placement by automated assembly equipment without adding excessive parasitics that could impair the high frequency performance of the ATF-541M4. The layout is shown with a footprint of the ATF-541M4 superimposed on the PCB pads for reference.

For Further Information

The information presented here is an introduction to the use of the ATF-541M4 enhancement mode PHEMT. More detailed application circuit information is available from Avago Technologies. Consult the web page or your local Avago Technologies sales representative.

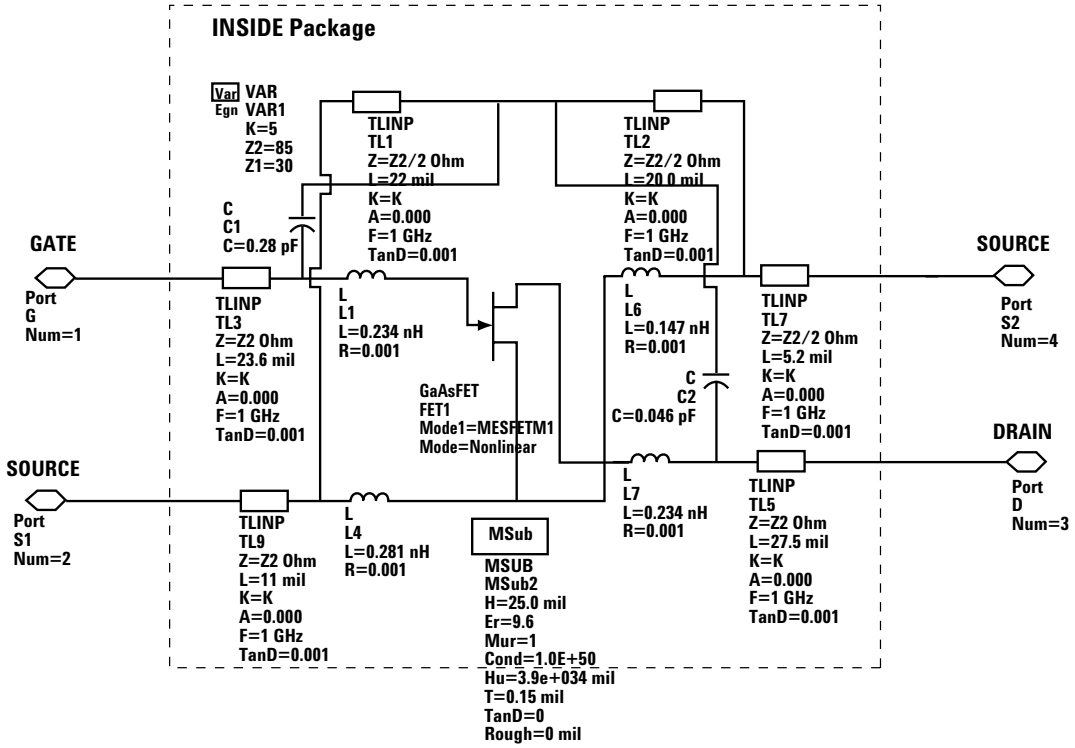
ATF-541M4 Die Model



Advanced_Curtice2_Model
MESFETM1

NFET=yes	Rf=	Crf=0.1 F	N=
PFET=no	Gscap=2	Gsfwd=	Fnc=1 MHz
Vto=0.3	Cgs=1.732 pF	Gsrev=	R=0.08
Beta=0.888	Cgd=0.255 pF	Gdfwd=	P=0.2
Lambda=72e-3	Gdcap=2	Gdrev=	C=0.1
Alpha=13	Fc=0.65	R1=	Taumdl=no
Tau=	Rgd=0.25 Ohm	R2=	wVgfwd=
Tnom=16.85	Rd=1.0125 Ohm	Vbi=0.95	wBvgs=
Idstc=	Rg=1.7 Ohm	Vbr=	wBvgd=
Ucrit=-0.72	Rs=0.3375 Ohm	Vjr=	wBvds=
Vgexp=1.91	Ld=	Is=	wIdsmax=
Gamds=1e-4	Lg=0.188 nH	Ir=	wPmax=
Vtotc=	Ls=	Imax=	AllParams=
Betatce=	Cds=0.273 pF	Xti=	
Rgs=0.25 Ohm	Rc=195 Ohm	Eg=	

ATF-541M4 Minipak Model

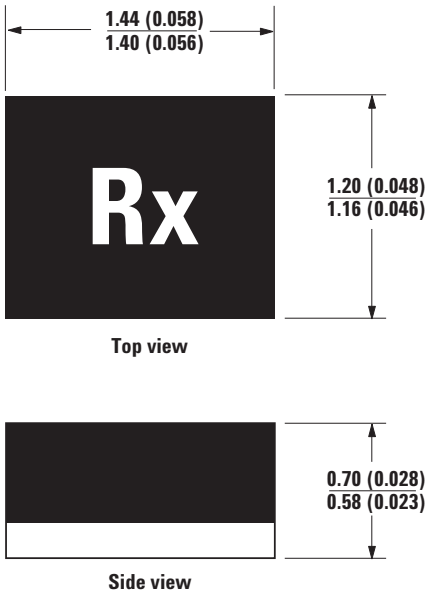


This model can be used as a design tool. It has been tested on ADS for various specifications. However, for more precise and accurate design, please refer to the measured data in this data sheet. For future improvements, Avago reserves the right to change these models without prior notice.

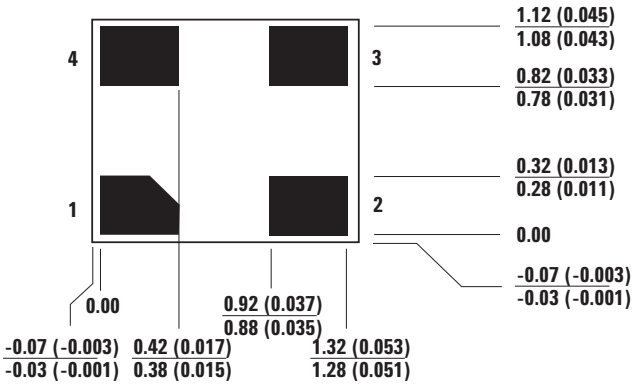
Ordering Information

Part Number	No. of Devices	Container
ATF-541M4-TR1	3000	7″ Reel
ATF-541M4-TR2	10000	13″ Reel
ATF-541M4-BLK	100	antistatic bag

MiniPak Package Outline Drawing

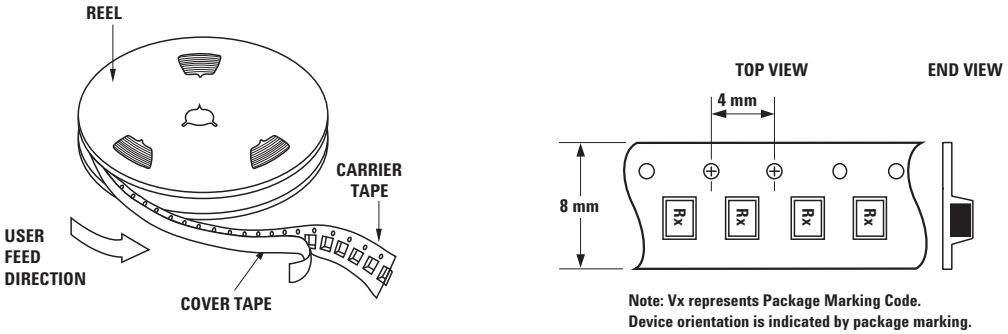


Solder Pad Dimensions



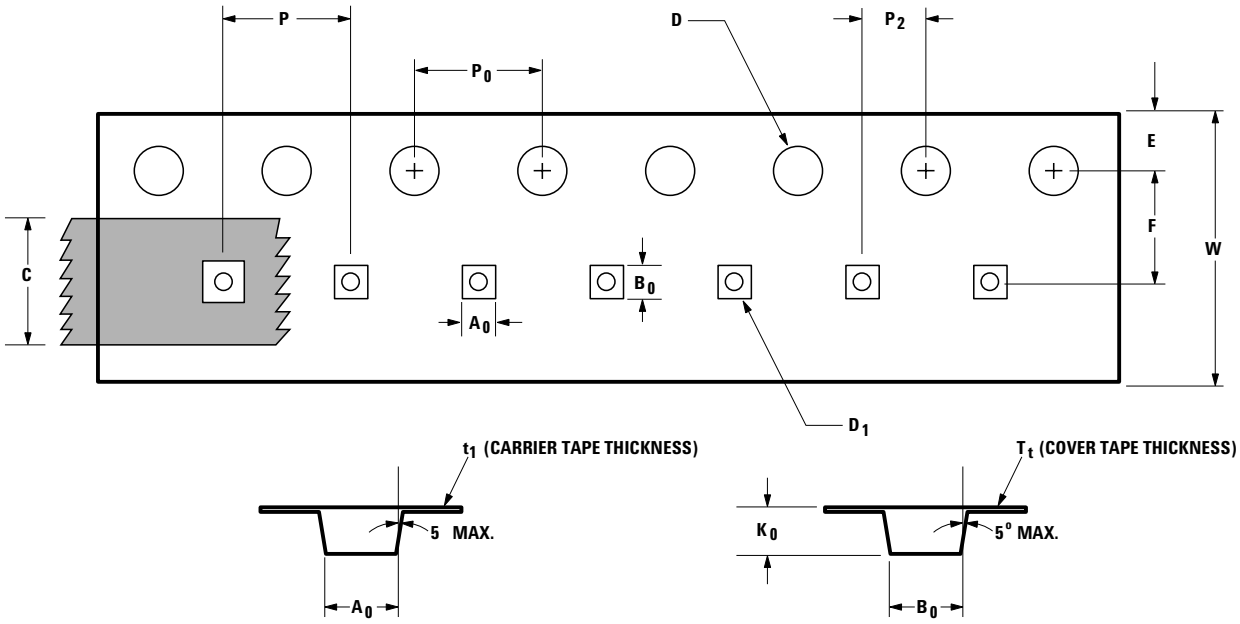
Dimensions are in millimeteres (inches)

Device Orientation for Outline 4T, MiniPak 1412



Note: Vx represents Package Marking Code.
Device orientation is indicated by package marking.

Tape Dimensions



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	1.40 0.05	0.055 0.002
	WIDTH	B_0	1.53 0.05	0.064 0.002
	DEPTH	K_0	0.80 0.05	0.031 0.002
	PITCH	P	4.00 0.10	0.157 0.004
	BOTTOM HOLE DIAMETER	D_1	0.80 0.05	0.031 0.002
PERFORATION	DIAMETER	D	1.50 0.10	0.060 0.004
	PITCH	P_0	4.00 0.10	0.157 0.004
	POSITION	E	1.75 0.10	0.069 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 - 0.10	0.315 + 0.012 - 0.004
	THICKNESS	t_1	0.254 0.02	0.010 0.0008
COVER TAPE	WIDTH	C	5.40 0.10	0.213 0.004
	TAPE THICKNESS	T_t	0.062 0.001	0.0024 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 0.05	0.138 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 0.05	0.079 0.002

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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