nuvoTon

ARM Cortex™-M0

32-BIT MICROCONTROLLER

NuMicro Mini51™ DE Series Datasheet

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1 GENERAL DESCRIPTION

The NuMicro Mini51™ series 32-bit microcontroller is embedded with ARM® Cortex™-M0 core for industrial control and applications which require high performance, high integration, and low cost. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NuMicro Mini51™ series can run up to 24 MHz and operate at 2.5V ~ 5.5V, -40℃ ~ 105℃, and thus can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro Mini51™ series offers 4K/8K/16K-bytes embedded program flash, size configurable data flash (shared with program flash), 2K-byte flash for the ISP, and 2K-byte SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NuMicro Mini51™ series in order to reduce component count, board space and system cost. These useful functions make the NuMicro Mini51™ series powerful for a wide range of applications.

Additionally, the NuMicro Mini51™ series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core running up to 24 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Built-in LDO for wide operating voltage ranged: 2.5 V to 5.5 V
- Memory
  - 4 KB/ 8 KB/ 16 KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash for loader (LDROM)
  - 2 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz external crystal input (HXT)
  - 32.768 kHz external crystal input (LXT) for Power-down wake-up and system operation clock
  - 22.1184 MHz internal oscillator (HIRC) (1% accuracy at 25°C, 5V)
    - Dynamically calibrating the HIRC OSC to 22.1184 MHz ±1% from -40°C to 105°C by external 32.768K crystal oscillator (LXT)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and Power-down wake-up
- I/O Port
  - Up to 30 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Input-only with high impendence
    - Push-pull output
    - Open-drain output
    - Quasi-bidirectional
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - Configurable default I/O mode of all pins after POR
- Timer

- Provides two channel 32-bit timers. One 8-bit pre-scale counter with 24-bit up counter for each timer
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Provides event counter function
- Supports wake-up from Idle or Power-down mode

- WDT (Watchdog Timer)
  - Multiple clock sources
  - Supports wake-up from Idle or Power-down mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Independent 16-bit PWM duty control units with maximum six outputs
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake protections
  - Supports duty, period, and fault break interrupts
  - Supports duty/period trigger ADC conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
- UART (Universal Asynchronous Receiver/Transmitters)
  - One UART device
  - Buffered receiver and transmitter, each with 16-byte FIFO
  - Optional flow control function (CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI devices
  - Supports Master/Slave mode

- Full-duplex synchronous serial data transfer
- Provides 3-wire function
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx latching data can be either at rising edge or at falling edge of serial clock
- Tx sending data can be either at rising edge or at falling edge of serial clock
- Supports Byte Suspend mode in 32-bit transmission
- 4-level depth FIFO buffer

- I^2C
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
  - Supports Power-down wake-up function
  - Support FIFO function
- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 300K SPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger, PWM trigger, or external pin trigger
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V

- Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 4.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro Mini51™ Series Selection Code

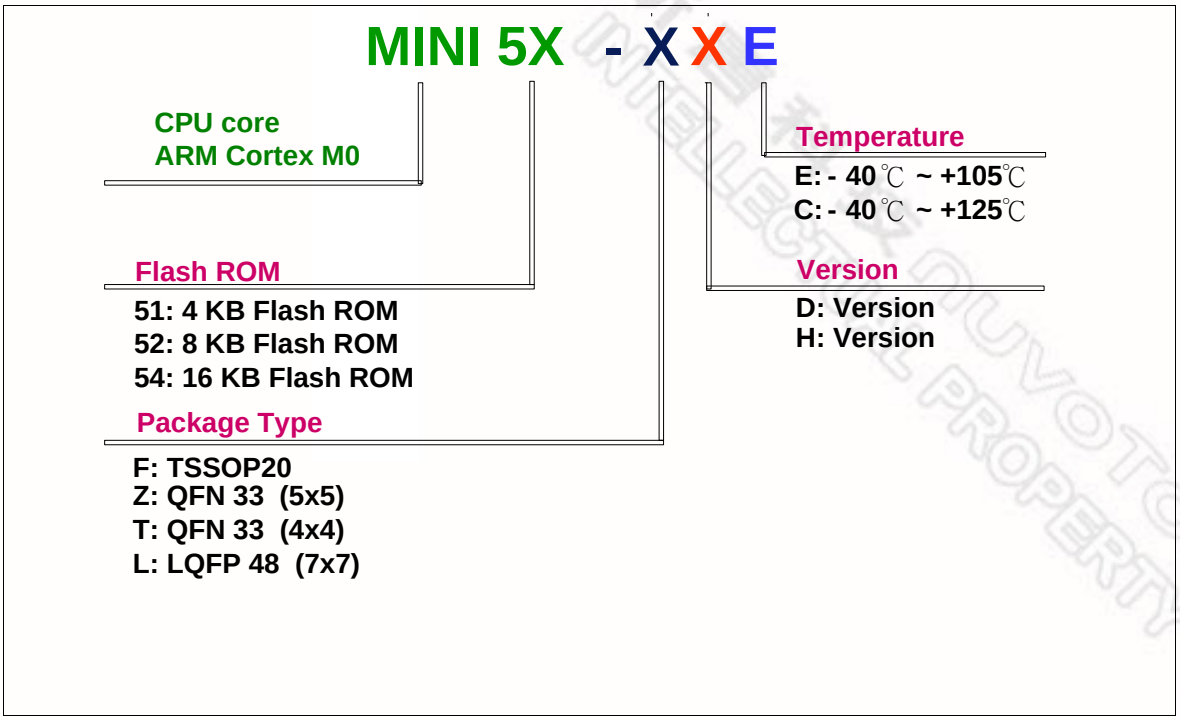


Figure 4.1-1 NuMicro Mini51™ Series Selection Code

4.2 NuMicro Mini51™ Series Product Selection Guide

Part No.	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP IAP	IRC 22.1184 MHz	Package
							UART	SPI	I²C						
MINI51FDE	4 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI51LDE	4 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI51ZDE	4 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI51TDE	4 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
MINI52FDE	8 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI52LDE	8 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI52ZDE	8 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI52TDE	8 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
MINI54FDE	16 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI54LDE	16 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI54ZDE	16 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI54TDE	16 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
*MINI54FHC	16 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	6	3x10-bit	v	v	TSSOP20

Table 4.2-1NuMicro Mini51™ Series Product Selection Guide

* Mini54FHC is a special part number, not pin to pin compatible to others Mini51series part number.

4.3 PIN CONFIGURATION

4.3.1 LQFP 48-pin

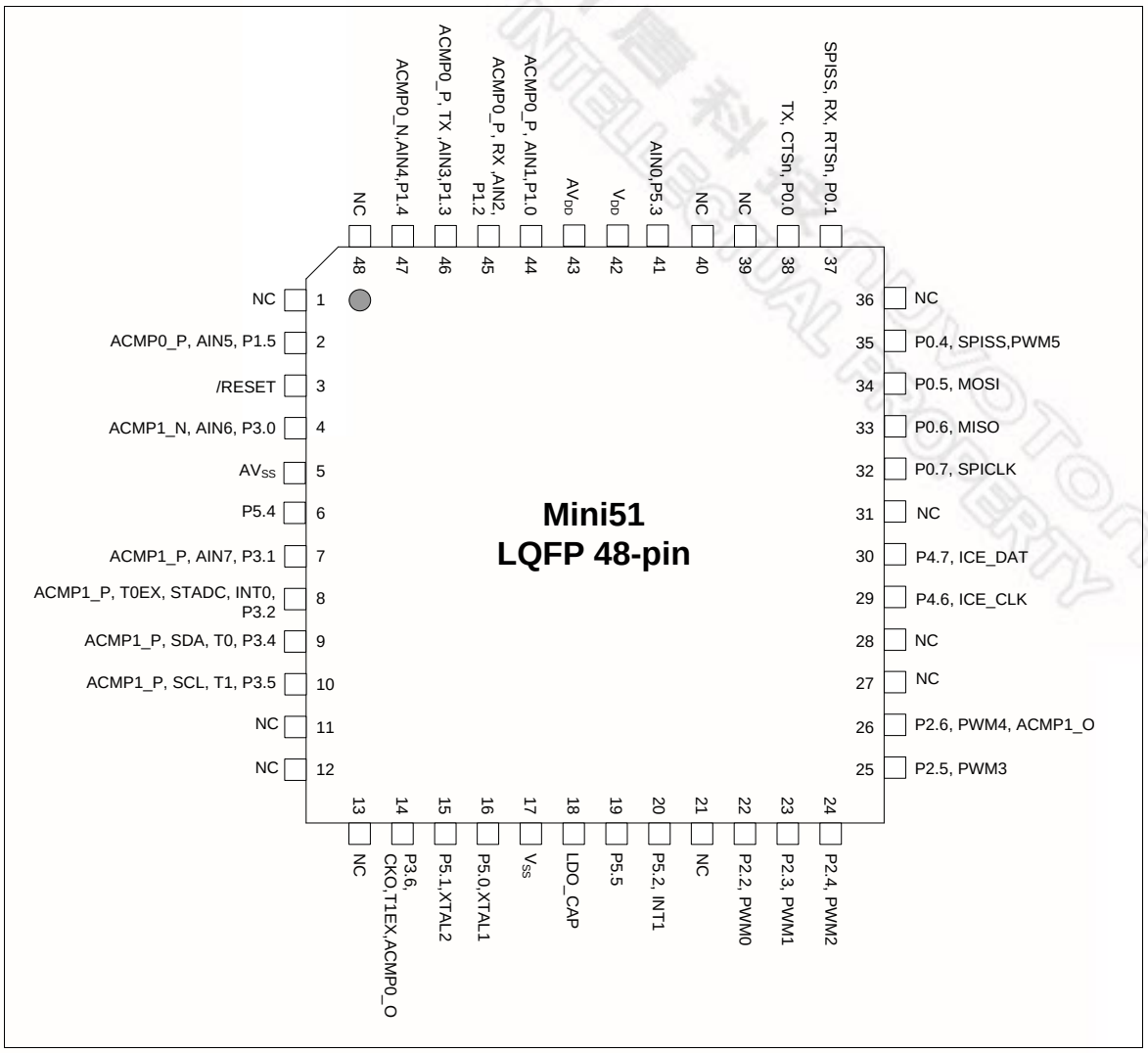


Figure 4.3-1 NuMicro Mini51™ Series LQFP 48-pin Diagram

4.3.2 QFN 33-pin

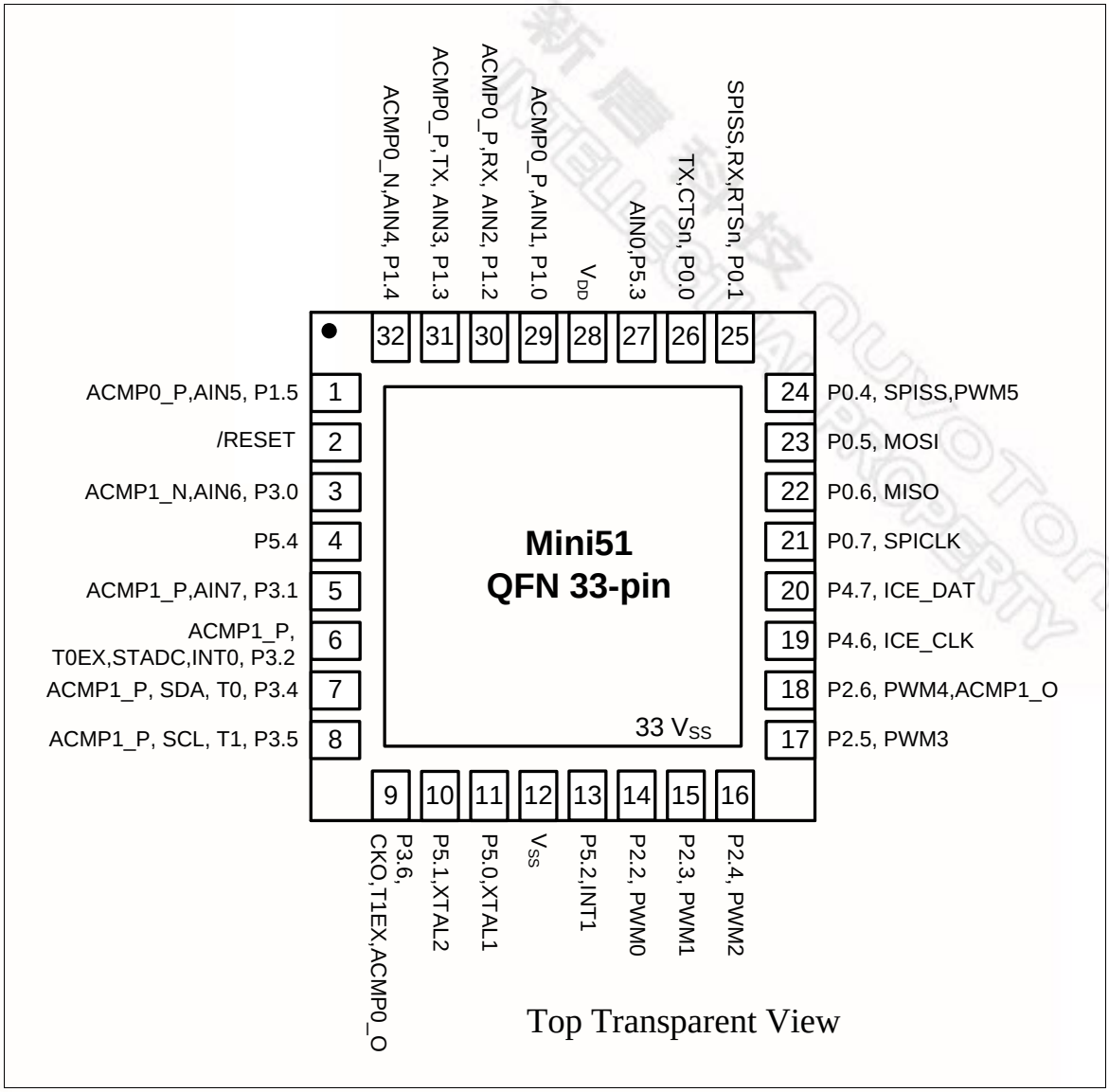


Figure 4.3-2 NuMicro Mini51™ Series QFN 33-pin Diagram

4.3.3 TSSOP 20-pin

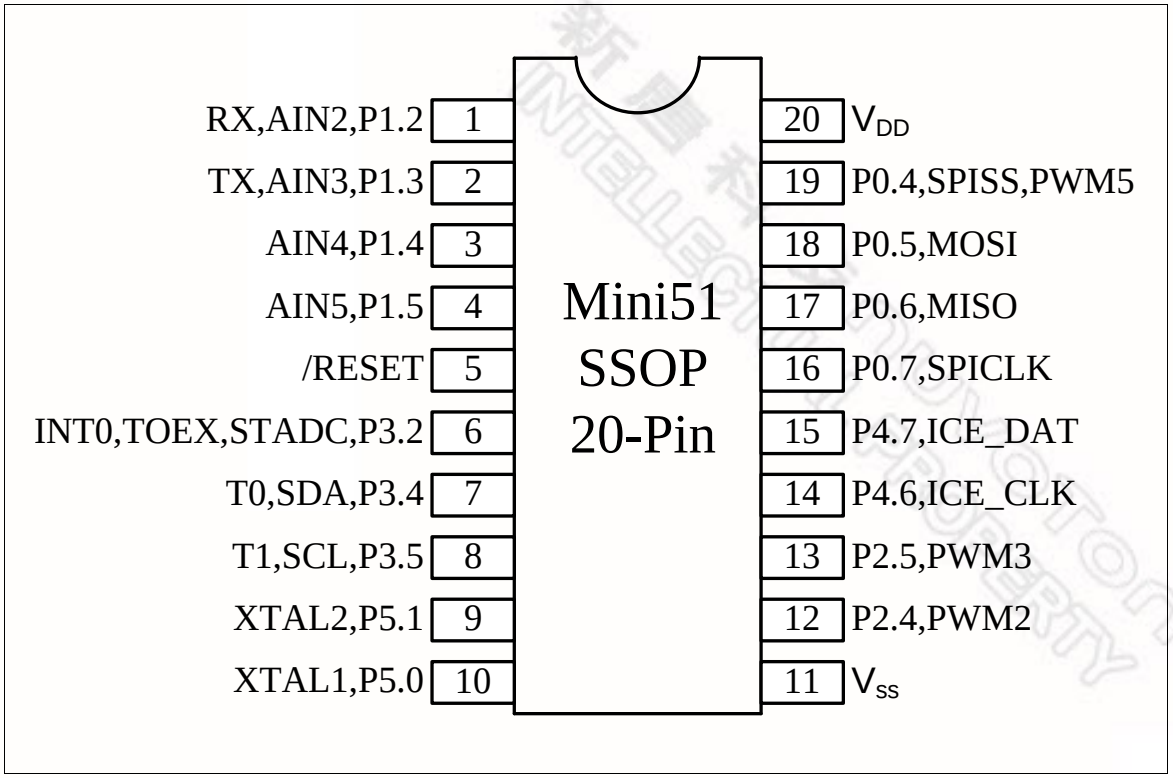


Figure 4.3-3 NuMicro Mini51™ Series TSSOP 20-pin Diagram

4.3.4 Mini54FHC (TSSOP20-pin)

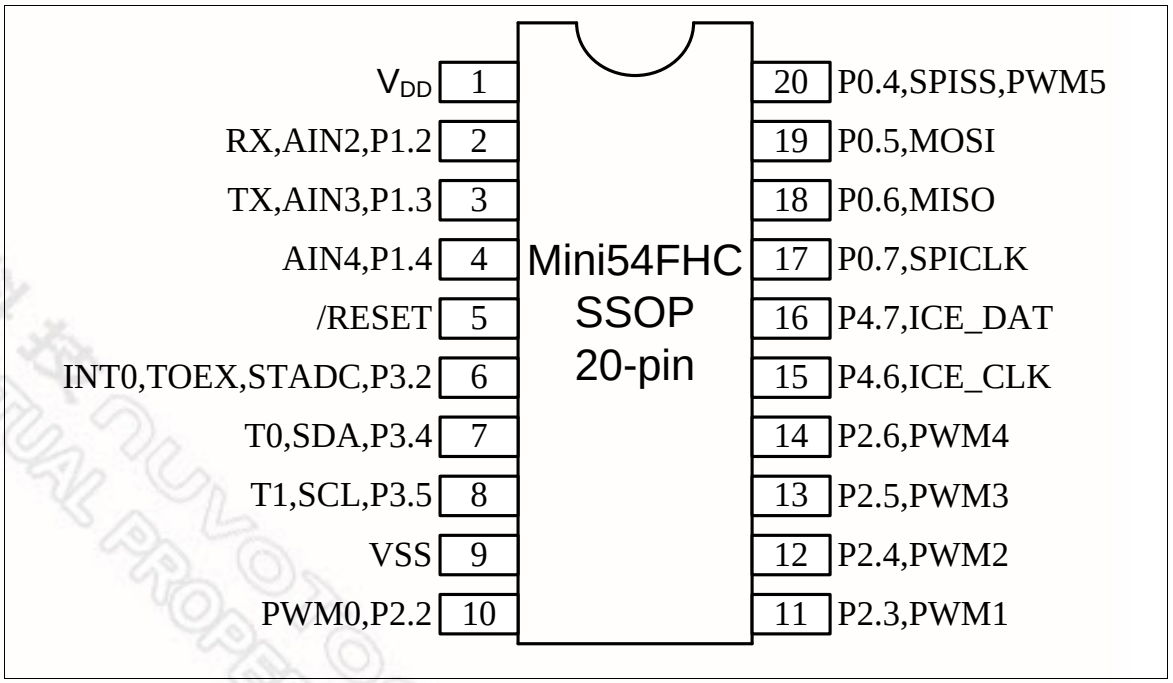


Figure 4.3-4 NuMicro Mini51™ Series TSSOP 20-pin Diagram

4.4 Pin Description

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
1	---	---	---	NC	**---**	Not connected
2	1	4	---	P1.5	**I/O**	General purpose digital I/O pin
				AIN5	**AI**	ADC analog input pin
				ACMP0_P	**AI**	Analog comparator positive input pin
3	2	5	5	/RESET	**I(ST)**	The Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. /RESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
4	3	---	---	P3.0	**I/O**	General purpose digital I/O pin
				AIN6	**AI**	ADC analog input pin
				ACMP1_N	**AI**	Analog comparator negative input pin
5	---	---	---	AV_{SS}	**AP**	Ground pin for analog circuit
6	4	---	---	P5.4	**I/O**	General purpose digital I/O pin
7	5	---	---	P3.1	**I/O**	General purpose digital I/O pin
				AIN7	**AI**	ADC analog input pin
				ACMP1_P	**AI**	Analog comparator positive input pin
8	6	6	6	P3.2	**I/O**	General purpose digital I/O pin
				INT0	**I**	External interrupt 0 input pin
				STADC	**I**	ADC external trigger input pin
				T0EX	**I**	Timer 0 external capture/reset trigger input pin
				ACMP1_P	**AI**	Analog comparator positive input pin
9	7	7	7	P3.4	**I/O**	General purpose digital I/O pin
				T0	**I/O**	Timer 0 external event counter input pin
				SDA	**I/O**	I^2C data I/O pin
				ACMP1_P	**AI**	Analog comparator positive input pin
10	8	8	8	P3.5	**I/O**	General purpose digital I/O pin
				T1	**I/O**	Timer 1 external event counter input pin
				SCL	**I/O**	I^2C clock I/O pin
				ACMP1_P	**AI**	Analog comparator positive input pin
11	---	---	---	NC	**---**	Not connected.
12	---	---	---	NC	**---**	Not connected.
13	---	--	--	NC	**---**	Not connected.

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
14	9	---	---	P3.6	I/O	General purpose digital I/O pin.
				ACMP0_O	O	Analog comparator output pin.
				CKO	O	Frequency divider output pin.
				T1EX	I	Timer 1 external capture/reset trigger input pin.
15	10	9	---	P5.1	I/O	General purpose digital I/O pin.
				XTAL2	O	The output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
16	11	10	---	P5.0	I/O	General purpose digital I/O pin.
				XTAL1	I	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
17	12	11	9	V_{SS}	P	Ground pin for digital circuit.
	33					
18	---	---	---	LDO_CAP	P	LDO output pin.
19	---	---	---	P5.5	I/O	General purpose digital I/O pin. User program must enable pull-up resistor in the QFN-33 package.
20	13	---	---	P5.2	I/O	General purpose digital I/O pin.
				INT1	I	External interrupt 1 input pin.
21	---	---	---	NC	---	Not connected.
22	14	---	10	P2.2	I/O	General purpose digital I/O pin.
				PWM0	O	PWM0 output of PWM unit.
23	15	---	11	P2.3	I/O	General purpose digital I/O pin.
				PWM1	O	PWM1 output of PWM unit.
24	16	12	12	P2.4	I/O	General purpose input/output digital pin.
				PWM2	O	PWM2 output of PWM unit.
25	17	13	13	P2.5	I/O	General purpose digital I/O pin.
				PWM3	O	PWM3 output of PWM unit.
26	18	---	14	P2.6	I/O	General purpose digital I/O pin.
				PWM4	O	PWM4 output of PWM unit.
				ACMP1_O	O	Analog comparator output pin.
27	---	---	---	NC	---	Not connected.
28	---	---	---	NC	---	Not connected.
29	19	14	15	P4.6	I/O	General purpose digital I/O pin.

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
				ICE_CLK	**I**	Serial wired debugger clock pin.
30	20	15	16	P4.7	**I/O**	General purpose digital I/O pin.
				ICE_DAT	**I/O**	Serial wired debugger data pin.
31	---	---	---	NC	**---**	Not connected.
32	21	16	17	P0.7	**I/O**	General purpose digital I/O pin.
				SPICLK	**I/O**	SPI serial clock pin.
33	22	17	18	P0.6	**I/O**	General purpose digital I/O pin.
				MISO	**I/O**	SPI MISO (master in/slave out) pin.
34	23	18	19	P0.5	**I/O**	General purpose digital I/O pin.
				MOSI	**O**	SPI MOSI (master out/slave in) pin.
35	24	19	20	P0.4	**I/O**	General purpose digital I/O pin.
				SPISS	**I/O**	SPI slave select pin.
				PWM5	**O**	PWM5 output of PWM unit.
36	---	---	---	NC	**---**	Not connected.
37	25	---	---	P0.1	**I/O**	General purpose digital I/O pin.
				RTSn	**O**	UART RTS pin.
				RX	**I**	UART data receiver input pin.
				SPISS	**I/O**	SPI slave select pin.
38	26	---	---	P0.0	**I/O**	General purpose digital I/O pin.
				CTSn	**I**	UART CTS pin.
				TX	**O**	UART transmitter output pin.
39	---	---	---	NC	**---**	Not connected.
40	---	---	---	NC	**---**	Not connected.
41	27	---	---	P5.3	**I/O**	General purpose digital I/O pin.
				AIN0	**AI**	ADC analog input pin.
42	28	20	1	V_{DD}	**P**	Power supply for digital circuit.
43				AV_{DD}	**P**	Power supply for analog circuit.
44	29	---	---	P1.0	**I/O**	General purpose digital I/O pin.
				AIN1	**AI**	ADC analog input pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
45	30	1	2	P1.2	**I/O**	General purpose digital I/O pin.
				AIN2	**AI**	ADC analog input pin.

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
				RX	**I**	UART data receiver input pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
46	31	2	3	P1.3	**I/O**	General purpose digital I/O pin.
				AIN3	**AI**	ADC analog input pin.
				TX	**O**	UART transmitter output pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
47	32	3	4	P1.4	**I/O**	General purpose digital I/O pin.
				AIN4	**I/O**	PWM5: PWM output/Capture input.
				ACMP0_N	**AI**	Analog comparator negative input pin.
48	---	--	--	NC	**---**	Not connected.

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

5 BLOCK DIAGRAM

5.1 NuMicro Mini51™ Block Diagram

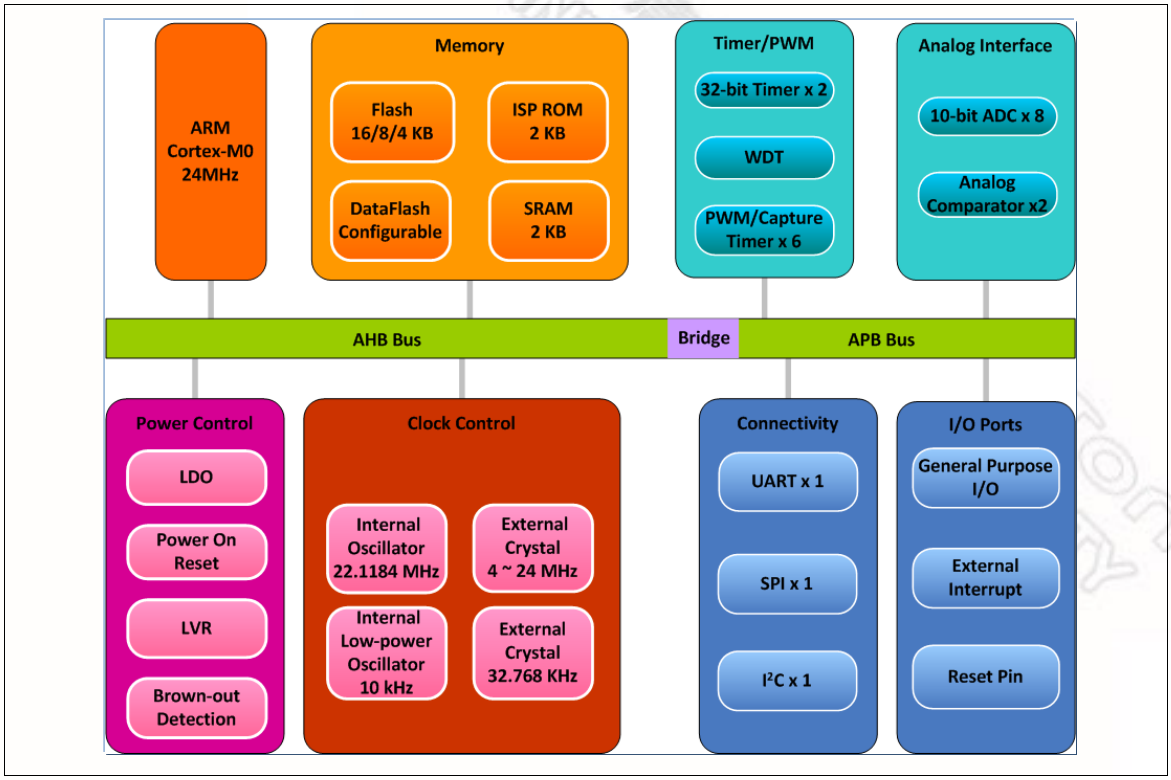


Figure 5.1-1 NuMicro Mini51™ Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Memory Organization

6.1.1 Overview

The NuMicro Mini51™ series provides 4G-byte addressing space. The addressing space assigned to each on-chip controllers is shown the following table. The detailed register definition, addressing space, and programming details will be described in the following sections for each on-chip peripheral. The NuMicro Mini51™ series only supports little-endian data format.

6.1.2 System Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Addressing Space	Token	Modules
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_3FFF	FLASH_BA	Flash Memory Space (16 KB)
0x2000_0000 – 0x2000_07FF	SRAM_BA	SRAM Memory Space (2 KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GP_BA	GPIO (P0~P5) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB Modules Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I^2C Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI_BA	SPI with Master/slave Function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM_BA	PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART_BA	UART Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
System Control Space (0xE000_E000 – 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Block Registers

Table 6.1-1 Address Space Assignments for On-Chip Modules

6.2 Nested Vectored Interrupt Controller (NVIC)

6.2.1 Overview

The Cortex™-M0 CPU provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features.

6.2.2 Features

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority change
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the Interrupt Service Routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.3 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro Mini51™ series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as 0 and the lowest priority is denoted as 3. The default priority of all the user-configurable interrupts is 0. Note that the priority 0 is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-1 Exception Model

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
1 ~ 15	-	-	-	System exceptions	-
16	0	**BOD_OUT**	Brown-out	Brown-out low voltage detected interrupt	Yes
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	2	**EINT0**	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	**EINT1**	GPIO	External signal interrupt from P5.2 pin	Yes
20	4	**GP0/1_INT**	GPIO	External signal interrupt from GPIO group P0~P1	Yes
21	5	**GP2/3/4_INT**	GPIO	External signal interrupt from GPIO group P2~P4 except P3.2	Yes
22	6	**PWM_INT**	PWM	PWM interrupt	No
23	7	**BRAKE_INT**	PWM	PWM interrupt	No
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt	Yes
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt	Yes
26 ~ 27	10 ~ 11	-	-	-	
28	12	**UART_INT**	UART	UART interrupt	Yes

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
29	13	-	-	-	
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	-	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HIRC_TRIM_INT**	HIRC	HIRC trim interrupt	No
34	18	**I2C_INT**	I^2C	I^2C interrupt	Yes
35 ~ 40	19 ~ 24	-	-	-	
41	25	**ACMP_INT**	ACMP	Analog Comparator 0 or Comparator 1 interrupt	Yes
42 ~ 43	26 ~ 27	-	-	-	
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	-	-	-	

Table 6.2-2 System Interrupt Map Vector Table

6.2.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number * 0x04	Exception Entry Pointer using that Exception Number

Table 6.2-3 Vector Table Format

6.2.5 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending; however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 System Manager

6.3.1 Overview

System management includes the following sections:

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.3.2 System Reset

The system reset can be included by one of the following listed events. For these reset events flags can be read by RSTSRC register.

- Power-On Reset (POR)
- Low level on the Reset Pin (/RESET)
- Watchdog Timer Time-out Reset (WDT)
- Brown-out Detector Reset (BOD)
- Cortex™-M0 MCU Reset
- CPU Reset

6.3.3 System Power Architecture

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.
- Digital power from V_{DD} and V_{SS} supplies power to the I/O pins and internal regulator which provides a fixed 1.8V power for digital operation.
- Build-in a capacitor for internal voltage regulator

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level as the digital power (V_{DD}). The following figure shows the power distribution of the Mini51™DE series.

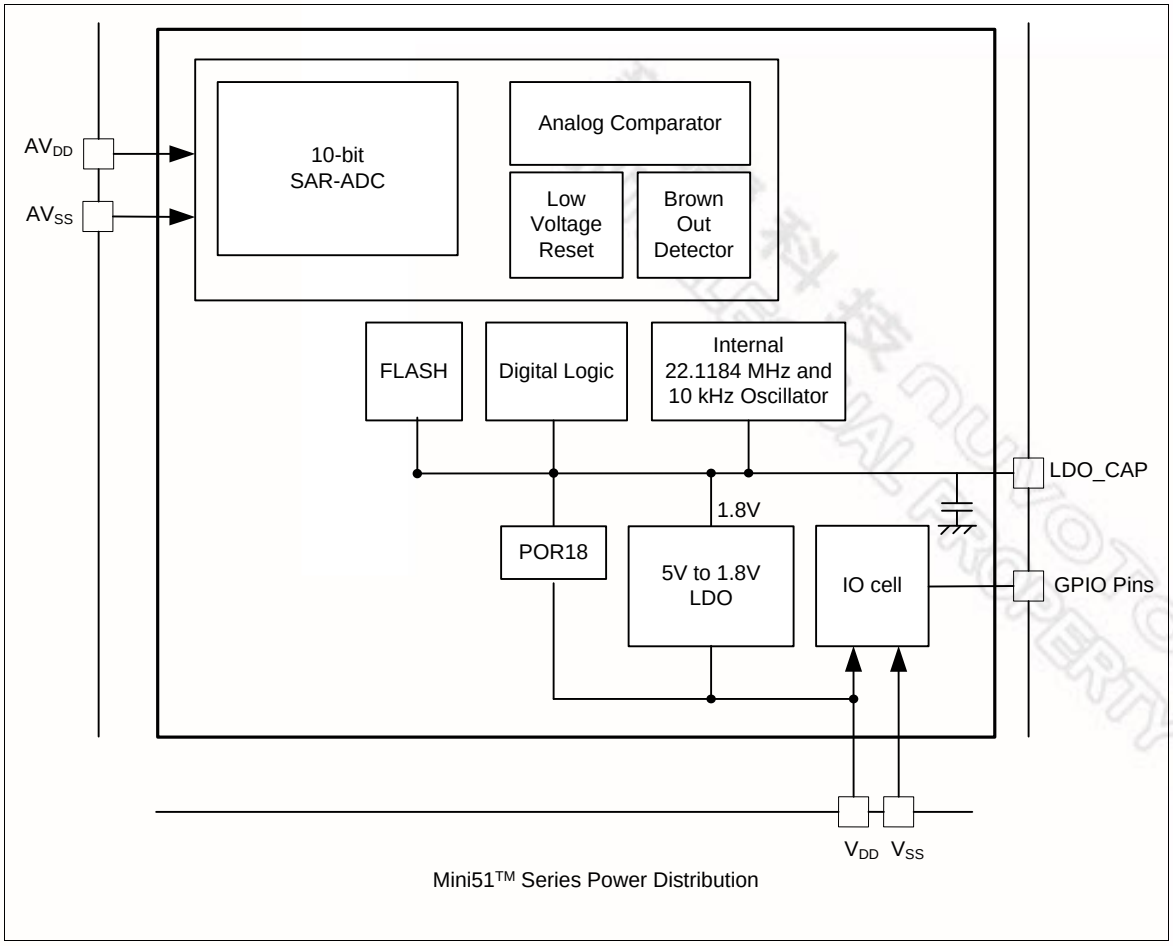


Figure 6.3-1 NuMicro Mini51™ Series Power Architecture Diagram

6.3.4 Whole System Memory Mapping

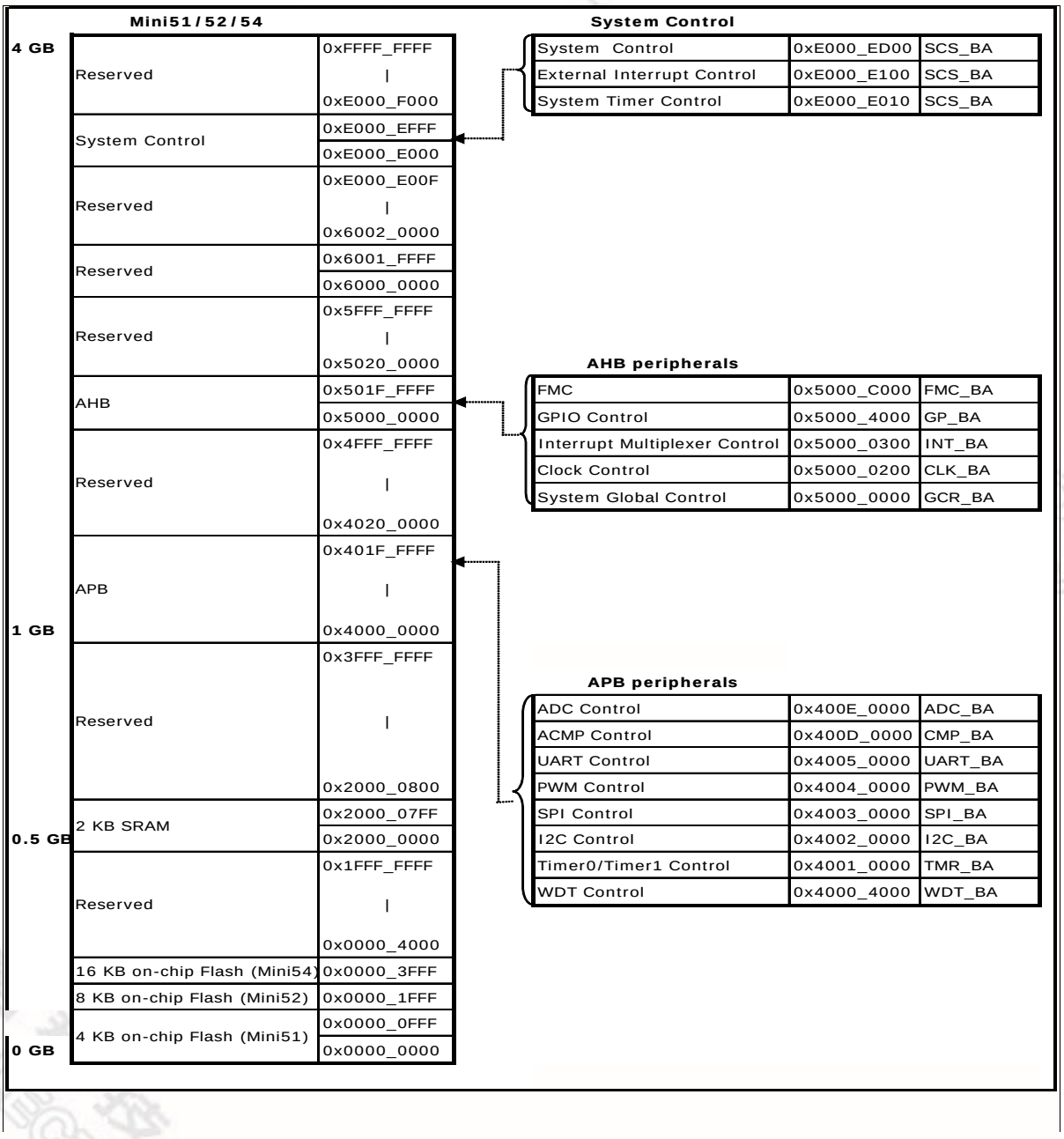


Table 6.3-1 Memory Mapping Table

6.4 Clock Controller

6.4.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex™-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 3 sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT) or 32.768 kHz (LXT) external low speed crystal oscillator
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

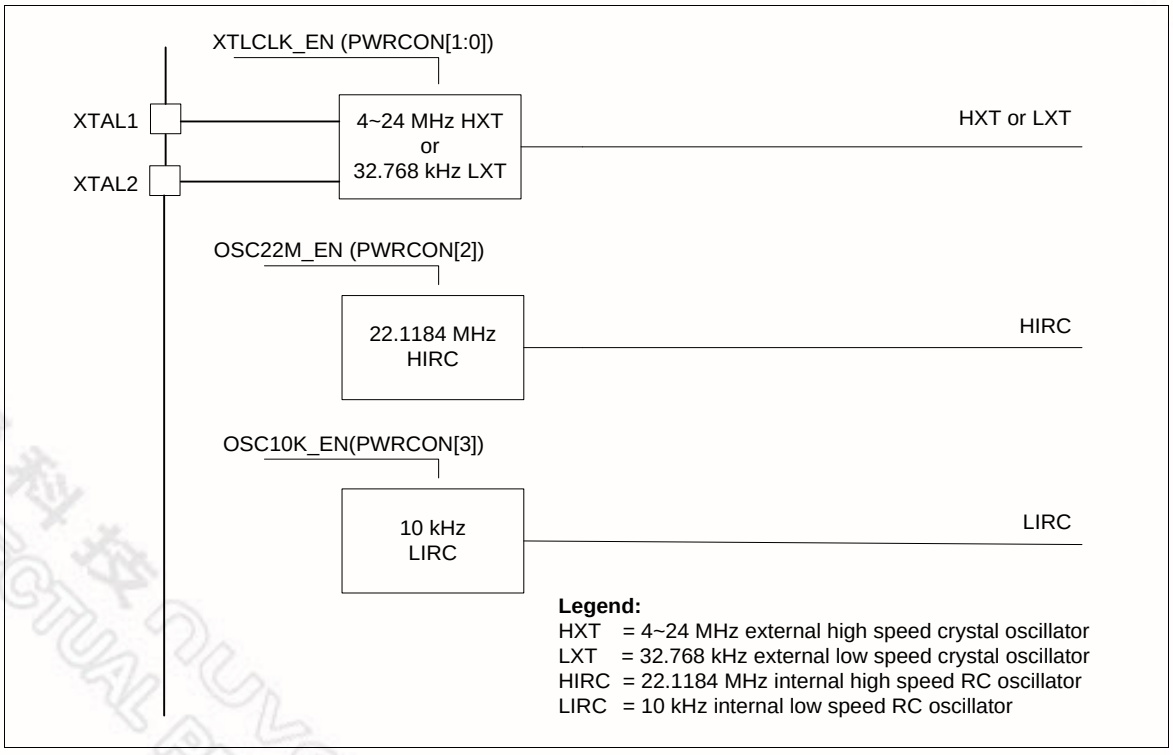


Figure 6.4-1 Clock Generator Block Diagram

6.4.2 System Clock and SysTick Clock

The system clock has three clock sources which are generated from clock generator block. The clock source switches depending on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown below.

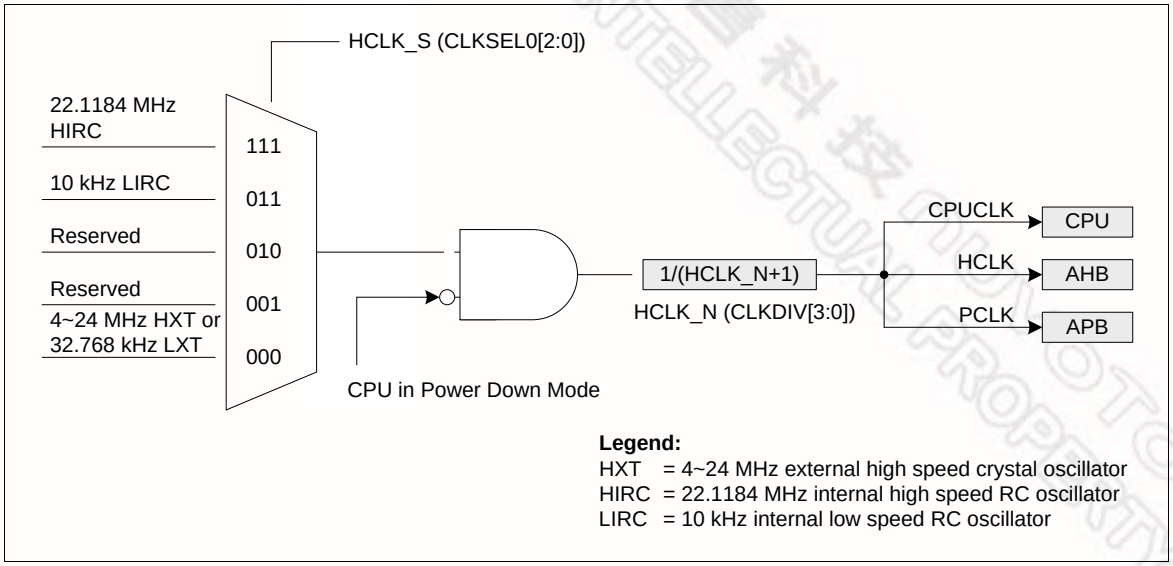


Figure 6.4-2 System Clock Block Diagram

The clock source of SysTick in Cortex™-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switches depending on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown below.

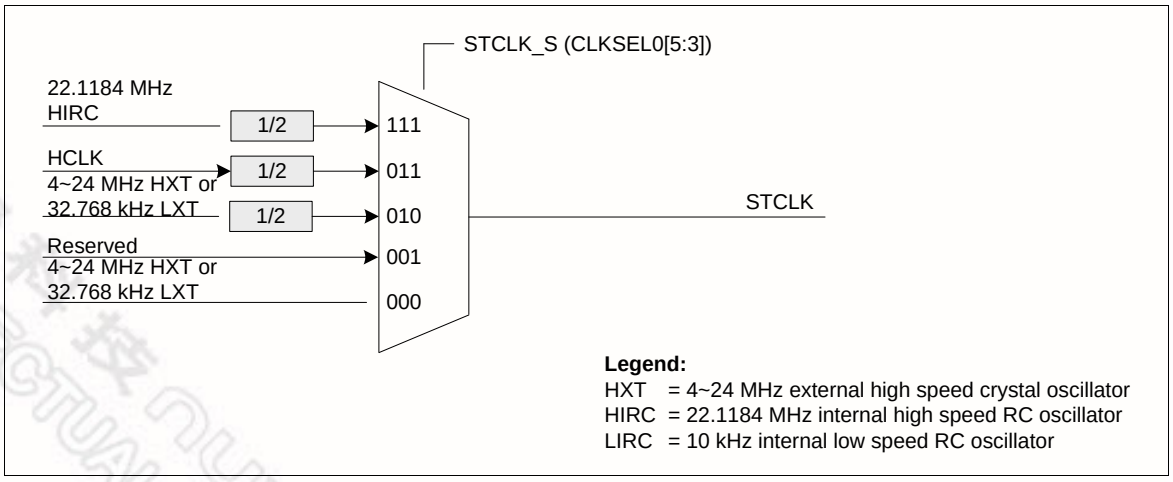


Figure 6.4-3 SysTick Clock Control Block Diagram

6.4.3 ISP Clock Source Selection

The clock source of ISP is from AHB clock (HCLK). Please refer to the register AHBCLK.

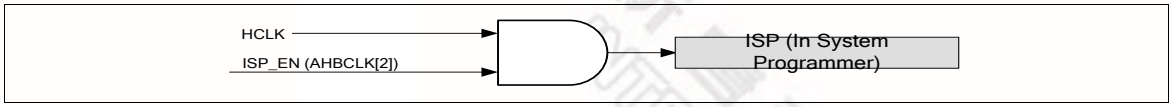


Figure 6.4-4 AHB Clock Source for HCLK

6.4.4 Module Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please refer to the CLKSEL1 and APBCLK register description in section **Error! Reference source not found.**.

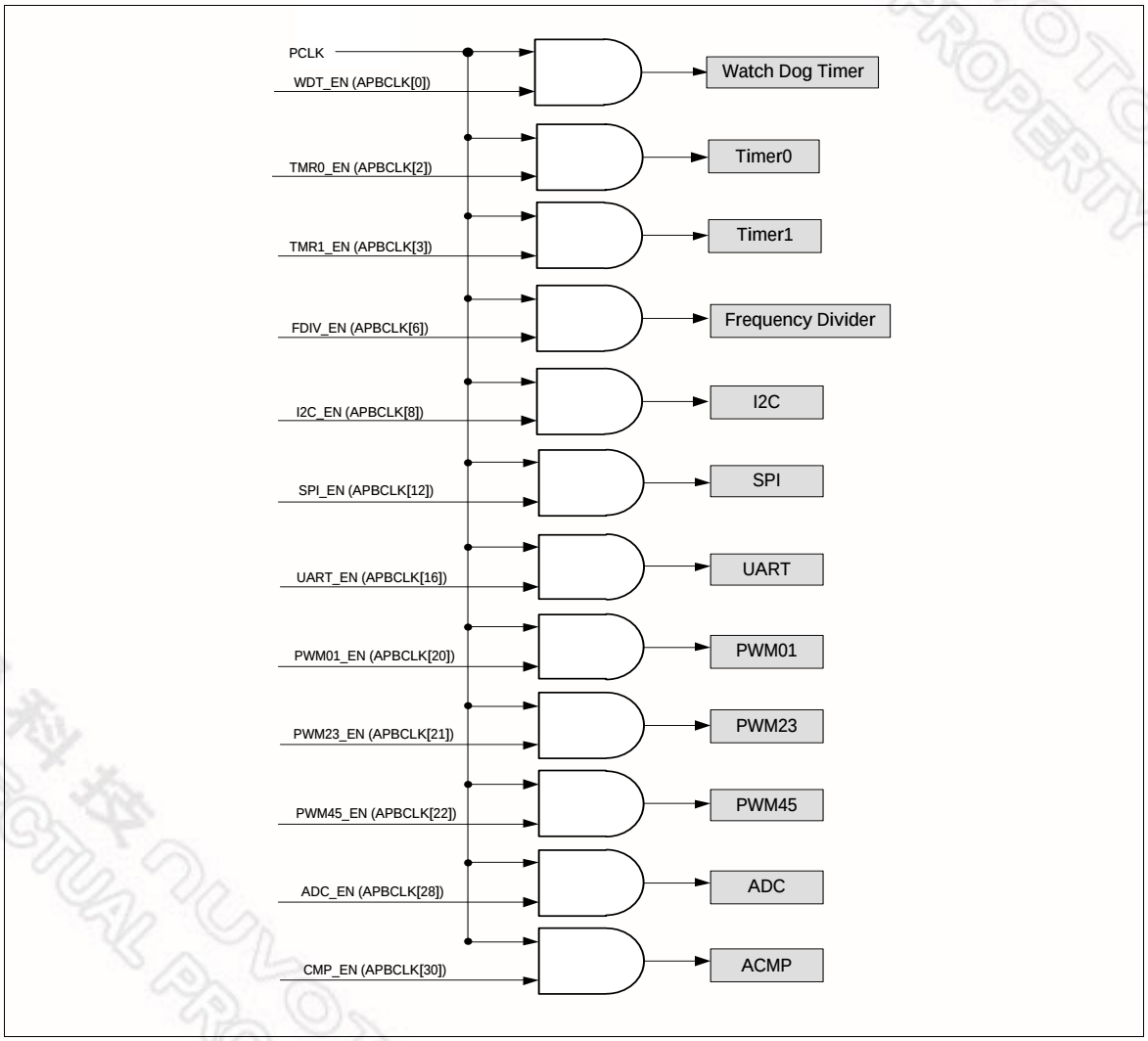


Figure 6.4-5 Peripherals Clock Source Selection for PCLK

	Ext. CLK (HXT Or LXT)	HIRC	LIRC	PCLK
WDT	Yes	No	Yes	Yes
Timer0	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes
I²C	No	No	No	Yes
SPI	No	No	No	Yes
UART	Yes	Yes	No	No
PWM	No	No	No	Yes
ADC	Yes	Yes	No	Yes
ACMP	No	No	No	Yes

Table 6.4-1 Peripheral Clock Source Selection Table

6.4.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripheral clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator (LIRC) clock
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PD_32K = 1 and XTLCLK_EN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

6.4.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\boldsymbol{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

if DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CKO pin directly.

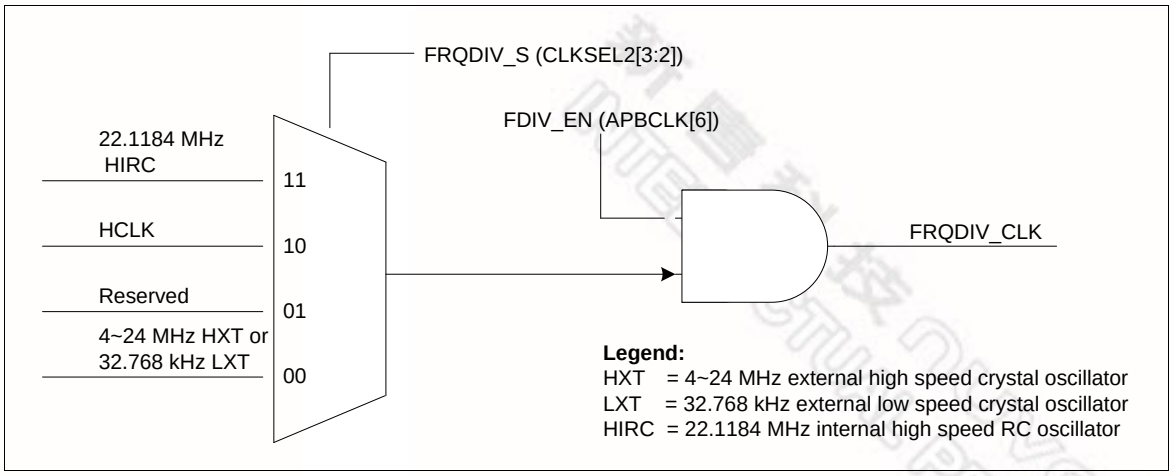


Figure 6.4-6 Clock Source of Frequency Divider

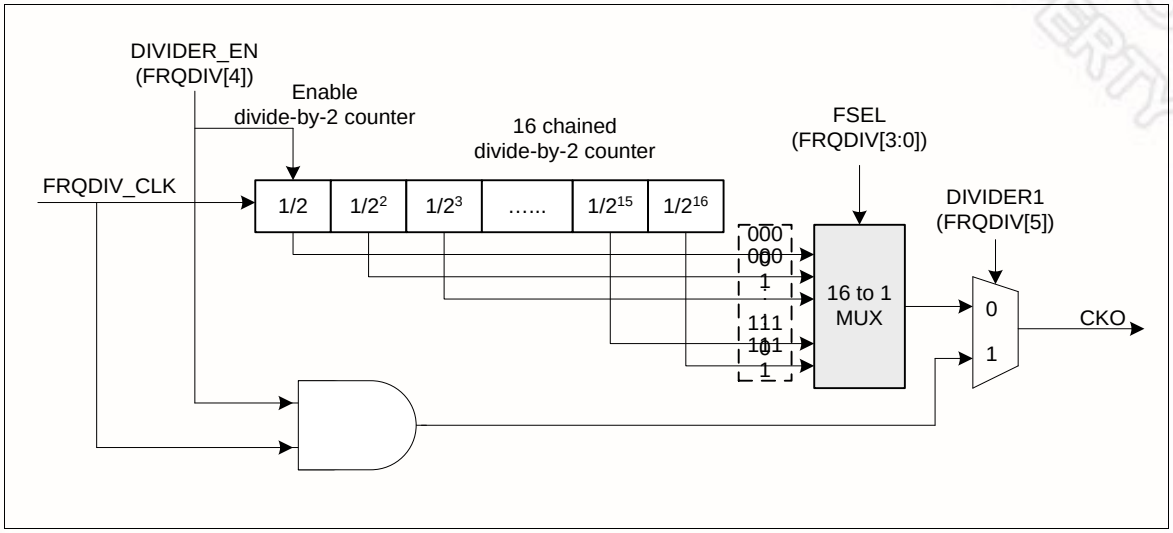


Figure 6.4-7 Block Diagram of Frequency Divider

6.5 Analog Comparator (ACMP)

6.5.1 Overview

The NuMicro Mini51™ Series contains two comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input greater than negative input, otherwise the output is 0. Each comparator can be configured to generate interrupt when the comparator output value changes.

6.5.2 Features

- Analog input voltage range: 0 ~ AV_{DD}
- Supports Hysteresis function
- Optional internal reference voltage source for each comparator negative input

6.6 Analog-to-Digital Converter (ADC)

6.6.1 Overview

The NuMicro Mini51™ series contains one 10-bit successive approximation analog-to-digital converters (SAR A/D converter) with eight input channels. The A/D converters can be started by software, external pin (STADC/P3.2) or PWM trigger.

6.6.2 Features

- Analog input voltage range: 0 ~ Analog Supply Voltage from AV_{DD}
- 10-bit resolution and 8-bit accuracy is guaranteed
- Up to eight single-end analog input channels
- 300 KSPS (AV_{DD} 4.5V - 5.5V) and 200 KSPS (AV_{DD} 2.5V - 5.5V) conversion rate
- An A/D conversion is performed one time on a specified channel
- An A/D conversion can be started by:
  - Software write 1 to ADST bit
  - External pin STADC
  - PWM trigger with optional start delay period
- Each conversion result is held in data register with valid and overrun indicators
- Conversion results can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 2 input sources: External analog voltage and internal fixed band-gap voltage

6.7 Flash Memory Controller (FMC)

6.7.1 Overview

The NuMicro Mini51™ series is equipped with 4K/8K/16K bytes on chip embedded flash memory for application program (APROM) that can be updated through ISP procedure. In-System-Programming (ISP) and In-Application-Programming (IAP) enable user to update program memory when chip is soldered on PCB. After chip power on Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro Mini51™ series also provides Data Flash region that is shared with APROM and its start address is configurable and defined by user in CONFIG1.

6.7.2 Features

- Running up to 24 MHz with zero wait state for discontinuous address read access
- 4/8/16 Kbytes application program memory (APROM)
- 2 Kbytes in system programming (ISP) loader program memory (LDROM)
- Programmable data flash start address
- All embedded flash memory supports 512 bytes page erase
- In System Program (ISP)/In Application Program (IAP) to update on chip flash memory

6.8 General Purpose I/O (GPIO)

6.8.1 Overview

The NuMicro Mini51™ series have up to 30 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 30 pins are arranged in 6 ports named as P0, P1, P2, P3, P4 and P5. Each of the 30 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each pin can be configured by software individually as Input, Push-pull output, Open-drain output, or Quasi-bidirectional mode. For Quasi-bidirectional mode, each I/O pin is equipped with a very weak individual pull-up resistor about 110 kΩ ~ 300 kΩ for V_{DD} is from 5.0 V to 2.5 V.

6.8.2 Features

- Four I/O modes:
  - Input-only with high impendence
  - Push-pull output
  - Open-drain output
  - Quasi-bidirectional
- TTL/Schmitt trigger input mode selected by Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function
- High driver and high sink I/O mode support
- Configurable default I/O mode of all pins after reset by CIOINI (Config0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in Input tri-state mode after chip reset (default)

6.9 I2C Serial Interface Controller (I2C)

6.9.1 Overview

I^2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I^2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. The I^2C also supports Power-down wake up function.

6.9.2 Features

The I^2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Master/Slave mode
- Bi-directional data transfer between masters and slaves
- Multi-master bus
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter that requests the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
- External pull-up needed for higher output pull-up speed
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address registers with mask option)
- Supports Power-down wake-up function
- Support FIFO function

6.10 Enhanced PWM Generator

6.10.1 Overview

The NuMicro Mini51™ series has built one PWM unit which is specially designed for motor driving control applications. The PWM unit supports six PWM generators which can be configured as six independent PWM outputs, PWM0~PWM5, or as three complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5) with three programmable dead-zone generators.

Every complementary PWM pairs share one 8-bit prescaler. There are six clock dividers providing five divided frequencies (1, 1/2, 1/4, 1/8, 1/16) for each channel. Each PWM output has independent 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The six PWM generators provide twelve independent PWM interrupt flags which are set by hardware when the corresponding PWM period counter comparison matched period and duty. Each PWM interrupt source with its corresponding enable bit can request PWM interrupt. The PWM generators can be configured as One-shot mode to produce only one PWM cycle signal or Auto-reload mode to output PWM waveform continuously.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit down counter/ comparator at the end of current period. The double buffering feature avoids glitch at PWM outputs.

Besides PWM, Motor controlling also need Timer, ACMP and ADC to work together. In order to control motor more precisely, we provide some registers that not only configure PWM but also Timer, ADC and ACMP, by doing so, it can save more CPU time and control motor with ease especially in BLDC.

6.10.2 Features

The PWM unit supports the following features:

- Independent 16-bit PWM duty control units with maximum six port pins:
  - Six independent PWM outputs – PWM0, PWM1, PWM2, PWM3, PWM4, and PWM5
  - Three complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-zone insertion – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
  - Three synchronous PWM pairs, with each pin in a pair in-phase – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
- Group control bit – PWM2 and PWM4 are synchronized with PWM0, PWM3 and PWM5 are synchronized with PWM1
- One-shot (only support edge alignment mode) or Auto-reload mode PWM
- Up to 16-bit resolution
- Supports Edge-aligned and Center-aligned mode
- Programmable dead-zone insertion between complementary paired PWMs
- Each pin of PWM0 to PWM5 has independent polarity setting control
- Hardware fault brake protections

- Two Interrupt source types:
  - Synchronously requested at PWM frequency when down counter comparison matched (edge- and center-aligned mode) or underflow (edge-aligned mode)
  - Requested when external fault brake asserted
    - BKP0: EINT0 or CPO1
    - BKP1: EINT1 or CPO0

- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.
- Supports independently rising CMR matching (in Center-aligned mode), CNR matching (in Center-aligned mode), falling CMR matching, period matching to trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change in BLDC application
- Supports ACMP output event trigger PWM to force PWM output at most one period low, this feature is usually for step motor control
- Provides interrupt accumulation function

6.11 Serial Peripheral Interface (SPI)

6.11.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. The SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. SPI controller can be configured as a master or a slave device.

6.11.2 Features

- Supports Master or Slave mode operation
- Configurable transfer bit length
- Provides four 32-bit FIFO buffers
- Supports MSB first or LSB first transfer
- Supports byte reorder function
- Supports byte or word suspend mode
- Supports Slave 3-wire mode

6.12 Timer Controller (TMR)

6.12.1 Overview

The Timer Controller includes two 32-bit timers, TIMER0 ~ TIMER1, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.12.2 Features

- Two sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each channel (TMR0_CLK, TMR1_CLK)
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}); T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin (T0, T1)
- 24-bit capture value is readable through TCAP (Timer Capture Data Register)
- Supports external capture pin (T0EX, T1EX) for interval measurement
- Supports internal signal (CPO0, CPO1) for interval measurement
- Supports external capture pin (T0EX, T1EX) to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.13 UART Controller (UART)

6.13.1 Overview

The NuMicro Mini51™ series provides one channel of Universal Asynchronous Receiver/Transmitters (UART). UART Controller performs Normal Speed UART, and supports flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, and RS-485 function mode.

6.13.2 Features

- Full duplex, asynchronous communications
- Separates 16-byte receive and transmitted FIFO for data payloads
- Supports hardware auto flow control, flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY(UA_TOR[15:8]) register
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit
  - Programmable stop bit, 1, 1.5, or 2 stop bit
- Supports IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enable to program RTS pin to control RS-485 transmission direction directly

6.14 Watchdog Timer (WDT)

6.14.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.14.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

7 ARM® CORTEX™-M0 CORE

7.1 Overview

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. The following figure shows the functional controller of the processor.

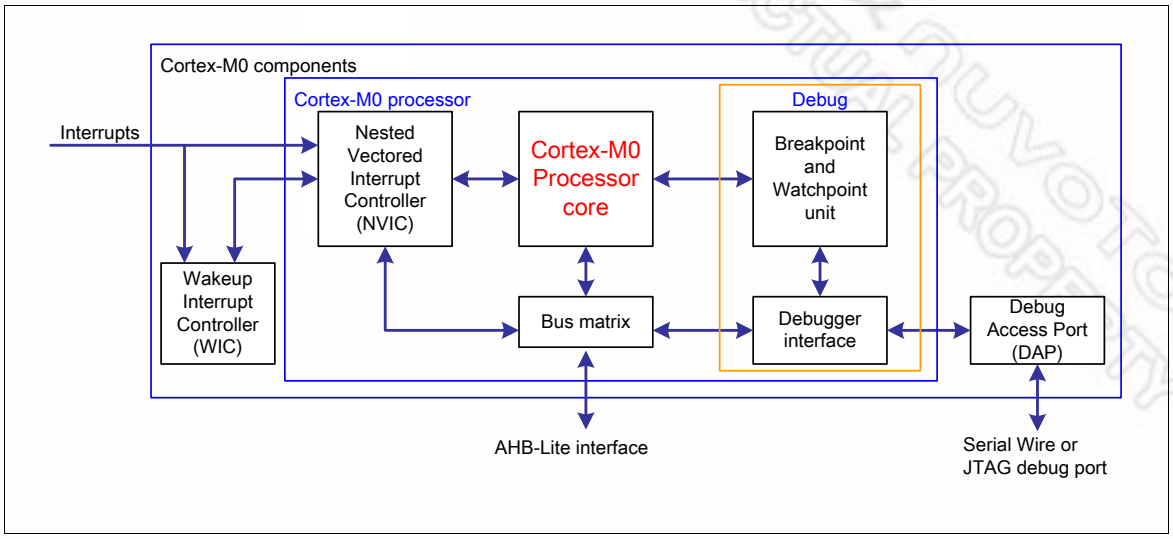


Figure 7.1-1 Functional Block Diagram

7.2 Features

- A low gate count processor
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model:

    This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power Idle mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Idle mode

- Debug support
  - Four hardware breakpoints
  - Two watch points
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

7.3 System Timer (SysTick)

The Cortex™-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

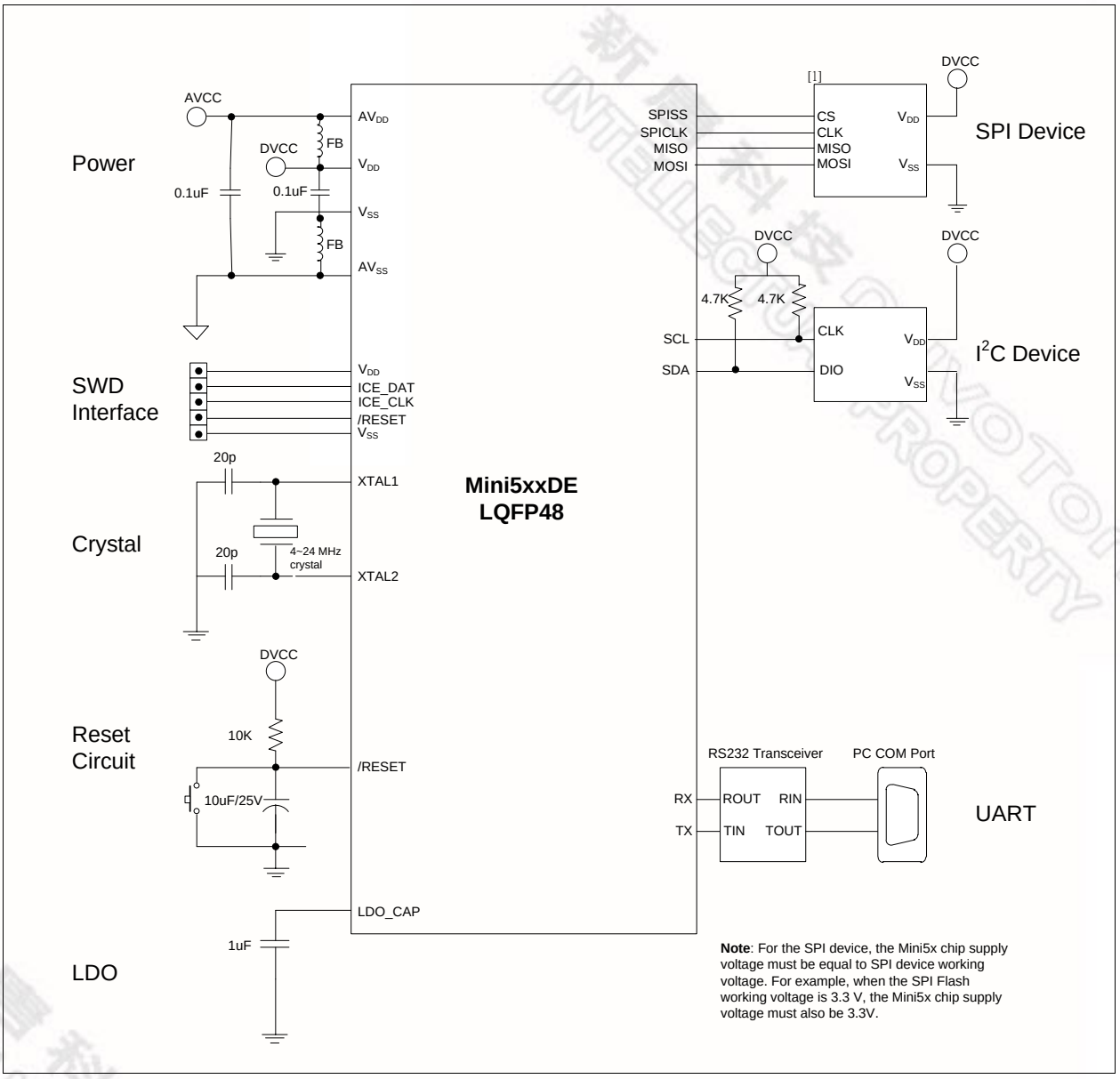
When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer to count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

8 APPLICATION CIRCUIT



9 MINI51XXDE ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

9.2 DC Electrical Characteristics

(VDD - VSS = 2.5 ~ 5.5 V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operation voltage	2.5	-	5.5	V	V_{DD} = 2.5V ~ 5.5V up to 24 MHz
V_{SS} / AV_{SS}	Power Ground	-0.3	-	-	V	
V_{LDO}	LDO Output Voltage	1.62	1.8	1.98	V	V_{DD} ≥ 2.5 V
V_{BG}	Band-gap Voltage	1.20	1.24	1.28	V	V_{DD} = 2.5V ~ 5.5V, T_A = 25°C
		1.18	1.24	1.32	V	V_{DD} = 2.5V ~ 5.5V, T_A = -40°C~105°C
V_{DD}-AV_{DD}	Allowed Voltage Difference for V_{DD} and AV_{DD}	-0.3	0	0.3	V	-
I_{DD1}	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	9.2	-	mA	V_{DD} 5.5V; HXT 24 MHz; HIRC Disable; All digital modules Enabled

I_{DD2}	Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){} Executed from Flash	-	7.0	-	mA	V_{DD} 5.5V HXT 24 MHz HIRC Disabled All digital modules Disabled
I_{DD3}		-	7.1	-	mA	V_{DD} 3.3V HXT 24 MHz HIRC Disable All digital modules Enabled
I_{DD4}		-	5.0	-	mA	V_{DD} 3.3 V HXT 24 MHz HIRC Disabled All digital modules Disabled
I_{DD5}		-	6.1	-	mA	V_{DD} 5.5V HXT Disabled HIRC Enabled All digital modules Enabled
I_{DD6}		-	3.9	-	mA	. V_{DD} 5.5V HXT Disabled HIRC Enabled All digital modules Disabled
I_{DD7}		-	6.0	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled All digital modules Enabled
I_{DD8}		-	3.9	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled All digital modules Disabled

I_{DD9}	Operating Current Normal Run Mode HCLK = 12MHz while(1){} Executed from Flash	-	5.5	-	mA	V_{DD} 5.5 V; HXT 12 MHz; HIRC Disabled; All digital modules Enabled
I_{DD10}		-	4.3	-	mA	V_{DD} 5.5 V; HXT 12 MHz; HIRC Disabled; All digital modules Disabled
I_{DD11}		-	3.9	-	mA	V_{DD} 3.3 V; HXT 12 MHz; HIRC Disabled; All digital modules Enabled
I_{DD12}		-	2.8	-	mA	V_{DD} 3.3 V; HXT 12 MHz; HIRC Disabled; All digital modules Disabled
I_{DD13}	Operating Current Normal Run Mode HCLK =4 MHz while(1){} Executed from Flash	-	3.2	-	mA	V_{DD} 5.5 V; HXT 4 MHz; HIRC Disabled; All digital modules Enabled
I_{DD14}		-	2.8	-	mA	V_{DD} 5.5 V; HXT 4 MHz; HIRC Disabled; All digital modules Disabled
I_{DD15}		-	1.8	-	mA	V_{DD} 3.3 V; HXT 4 MHz; HIRC Disabled; All digital modules Enabled

I_{DD16}		-	1.4	-	mA	V_{DD} 3.3 V HXT 4 MHz HIRC Disabled All digital modules Disabled
I_{DD17}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	225	-	μA	V_{DD} 5.5 V HXT Disabled HIRC □isabled LIRC Enabled All digital modules Enabled Only enable modules which support 10 kHz LIRC clock source
I_{DD18}		-	225	-	μA	V_{DD} 5.5 V HXT Disabled HIRC Disabled LIRC Enabled All digital modules Disabled
I_{DD19}		-	200	-	μA	V_{DD} 3.3 V HXT Disa□led HIRC Disabled LIRC Enabled All digital modules Enabled Only enable modules which support 10 kHz LIRC clock source
I_{DD20}		-	200	-	μA	V_{DD} 3.3 V HXT Disabled HIRC Disabled LIRC Enabled All digital modules Disa□led
I_{IDLE1}	Operating Current Idle Mode HCLK = 24MHz	-	7.1	-	mA	V_{DD} 5.5V HXT 24 MHz HIRC Disable All digital modules Enabled

I_{IDLE2}	Operating Current Idle Mode HCLK=22.1184 MHz	-	4.9	-	mA	V_{DD} 5.5V; HXT 24 MHz; HIRC Disabled; All digital modules Disabled
I_{IDLE3}		-	5.1	-	mA	V_{DD} 3.3V; HXT 24 MHz; HIRC Disable; All digital modules Enabled
I_{IDLE4}		-	2.9	-	mA	V_{DD} 5.5V; HXT 24 MHz; HIRC Disabled; All digital modules Disabled
I_{IDLE5}		-	4.1	-	mA	V_{DD} 5.5V; HXT Disabled; HIRC Enabled; All digital modules Enabled
I_{IDLE6}		-	2.0	-	mA	. V_{DD} 5.5V; HXT Disabled; HIRC Enabled; All digital modules Disabled
I_{IDLE7}		-	4.1	-	mA	V_{DD} 3.3V; HXT Disabled; HIRC Enabled; All digital modules Enabled
I_{IDLE8}		-	1.9	-	mA	V_{DD} 3.3V; HXT Disabled; HIRC Enabled; All digital modules Disabled

I_{IDLE9}	Operating Current Idle Mode HCLK =12 MHz	-	4.4	-	mA	V_{DD} 5.5 V HXT 12 MHz HIRC Disabled All digital modules Enabled
I_{IDLE10}		-	3.3	-	mA	V_{DD} 5.5 V HXT 12 MHz HIRC Disabled All digital modules Disabled
I_{IDLE11}		-	2.9	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled All digital modules Enabled
I_{IDLE12}		-	1.8	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled All digital modules Disabled
I_{IDLE13}	Operating Current Idle Mode HCLK =4 MHz	-	2.9	-	mA	V_{DD} 5.5 V HXT 4 MHz HIRC Disabled All digital modules Enabled
I_{IDLE14}		-	2.5	-	mA	V_{DD} 5.5 V HXT 4 MHz HIRC Disabled All digital modules Disabled
I_{IDLE15}		-	1.5	-	mA	V_{DD} 3.3 V HXT 4 MHz HIRC Disabled All digital modules Enabled

I_{IDLE16}	Operating Current Idle Mode at 10 kHz	-	1.1	-	mA	V_{DD} 3.3 V; HXT 4 MHz; HIRC Disabled; All digital modules Disabled
I_{IDLE17}		-	225	-	µA	V_{DD} 5.5 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Enabled; Only enable modules which support 10 kHz LIRC clock source
I_{IDLE18}		-	225	-	µA	V_{DD} 5.5 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Disabled
I_{IDLE19}		-	200	-	µA	V_{DD} 3.3 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Enabled; Only enable modules which support 10 kHz LIRC clock source
I_{IDLE20}		-	200	-	µA	V_{DD} 3.3 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Disabled
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	10	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.
I_{PWD2}		-	9	-	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off.
I_{IL}	Logic 0 Input Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-	-70	-75	µA	V_{DD} = 5.5 V, V_{IN} = 0V

I_{TL}	Logic 1 to 0 Transition Current P0/1/2/3/4/5 (Quasi-bidirectional Mode) [*3]	-	-690	-750	µA	V_{DD} = 5.5 V, V_{IN} = 2.0V
I_{LK}	Input Leakage Current P0/1/2/3/4/5	-1	-	+1	µA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage P0/1/2/3/4/5 (TTL Input)	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
V_{IH1}	Input High Voltage P0/1/2/3/4/5 (TTL Input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{IL3}	Input Low Voltage XTAL1[*2]	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 2.5 V
V_{IH3}	Input High Voltage XTAL1[*2]	3.5	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{ILS}	Negative-going Threshold (Schmitt Input), /RESET	-0.3	-	0.2V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), /RESET	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
R_{RST}	Internal /RESETPin Pull-up Resistor	40		150	kΩ	V_{DD} = 2.5 V ~ 5.5V
V_{ILS}	Negative-going Threshold (Schmitt input), P0/1/2/3/4/5	-0.3	-	0.3V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt input), P0/1/2/3/4/5	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
I_{SR11}	Source Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-300	-400	-	µA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR12}		-50	-80	-	µA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR13}		-40	-73	-	µA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SR21}	Source Current P0/1/2/3/4/5 (Push-pull Mode)	-20	-26	-	mA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR22}		-3	-5	-	mA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR23}		-2.5	-5	-	mA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SK11}	Sink Current P0/1/2/3/4/5 (Quasi-bidirectional, Open-	10	15	-	mA	V_{DD} = 4.5 V, V_S = 0.45 V
I_{SK12}		6	9	-	mA	V_{DD} = 2.7 V, V_S = 0.45 V

I_{SK13}	Drain and Push-pull Mode)	5	8	-	mA	V_{DD} = 2.5 V, V_S = 0.45 V

Notes:

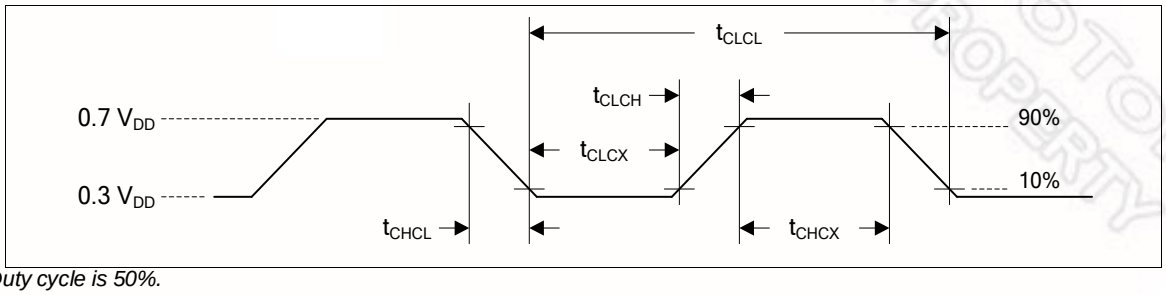
1. /RESET pin is a Schmitt trigger input.

2. XTAL1 is a CMOS input.

3. Pins of P0, P1, P2, P3, P4 and P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of VDD=5.5V, the transition current reaches its maximum value when VIN approximates to 2V.

9.3 AC Electrical Characteristics

9.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

9.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	2.5	-	mA	12 MHz, V_{DD} = 5.5V
		-	1.0	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

9.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4MHz ~ 24 MHz	10~20 pF	10~20 pF

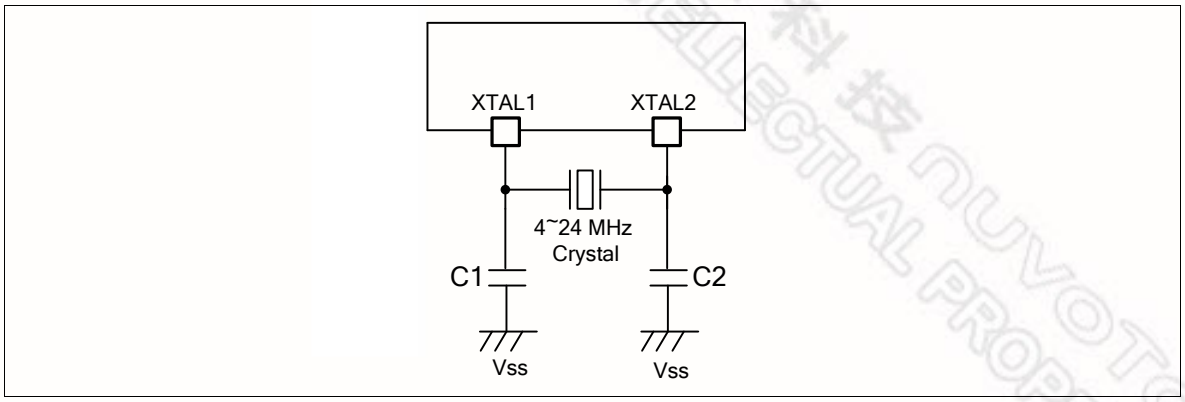
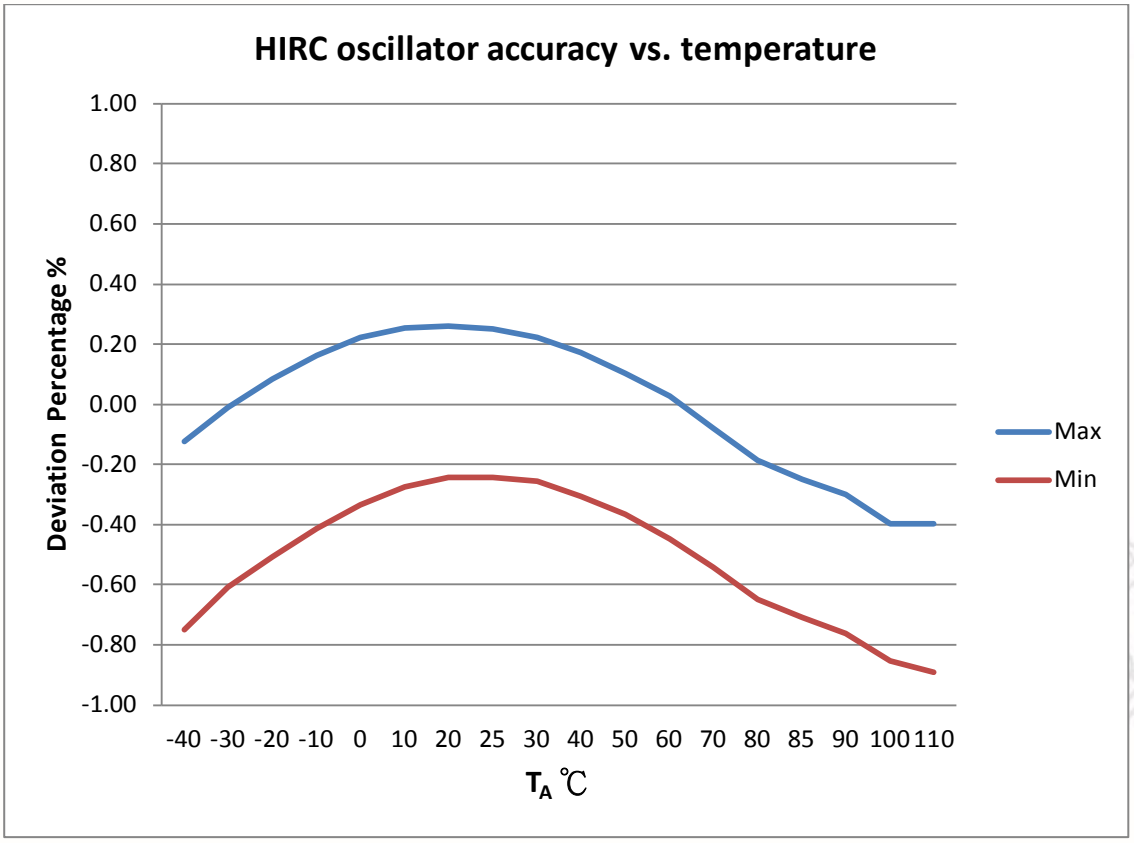


Figure 9-1Mini5xDE Typical Crystal Application Circuit

9.3.4 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5 V
		-2	-	+2	%	T_A = -40℃~105℃ V_{DD}=2.5 V~ 5.5 V
I_{HRC}	Operating Current	-	700	-	μA	T_A = 25 ℃,V_{DD} = 5 V



9.3.5 10 kHz Internal Low Speed RC Oscillator(LIRC)

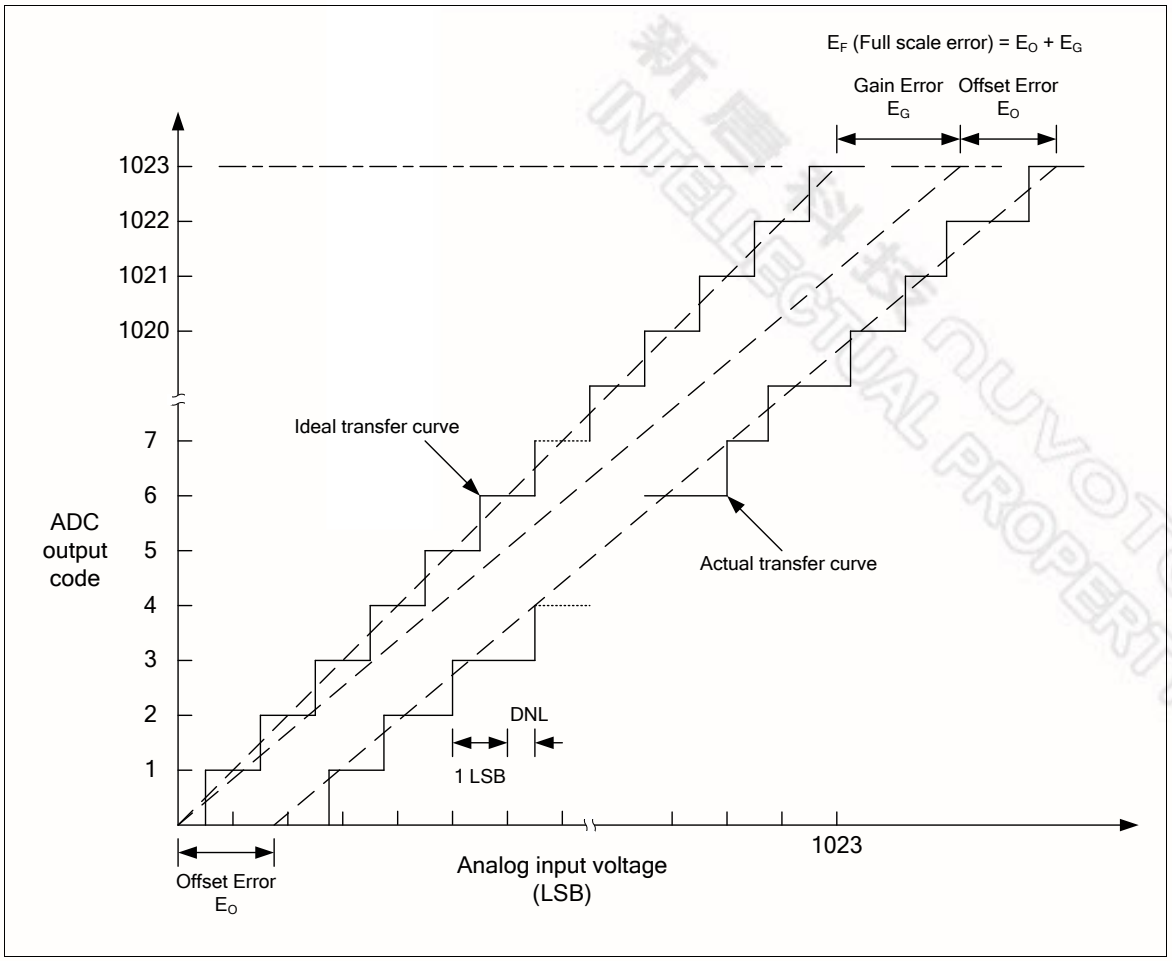
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	2.5	-	5.5	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-10	-	+10	%	V_{DD}=2.5V~ 5.5V T_A = 25℃
		-40	-	+40	%	V_{DD}=2.5V~ 5.5V T_A = -40℃~+105℃

9.4 Analog Characteristics

9.4.1 10-bit SARADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	10	Bit	-
DNL	Differential Nonlinearity Error	-	-1~1.5	-1~+2.5	LSB	-
INL	Integral Nonlinearity Error	-	±1	±2	LSB	-
E_O	Offset Error	-	1	2	LSB	-
E_G	Gain Error (Transfer Gain)	-	-1	-3	LSB	-
E_A	Absolute Error	-	3	4	LSB	-
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency	-	-	4.2	MHz	AV_{DD} = 4.5~5.5 V
		-	-	2.8		AV_{DD} =2.5~5.5 V
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	300	kSPS	AV_{DD} = 4.5~5.5 V
		-	-	200	kSPS	AV_{DD} = 2.5~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	N is sampling counter, N=0,1,2, 4,8, 16,32, 4, 128, 256,1024
T_{CONV}	Total Conversion Time	N+14			$1/F_{ADC}$	
AV_{DD}	Supply Voltage	2.5	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	600	-	μA	AV_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	3.2	-	pF	-
R_{IN}	Input Load	-	6	-	kΩ	-

Note: ADC voltage reference is same with AV_{DD}



9.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.5	-	5.5	V	-
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	-
T_A	Temperature	-40	25	105	℃	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

9.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-

T_A	Temperature	-40	25	105	℃	-
I_{LVR}	Quiescent Current	-	1	5	μA	AV_{DD} =5.5V
V_{LVR}	Threshold Voltage	1.90	2.00	2.10	V	T_A=25℃
		1.70	1.90	2.05	V	T_A=-40℃
		2.00	2.20	2.45	V	T_A =105℃

9.4.4 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	-	140	μA	AV_{DD} =5.5V
V_{BOD}	Brown-out Detector (Falling edge)	4.2	4.38	4.55	V	BOD_VL [1:0]=11
		3.5	3.68	3.85	V	BOD_VL [1:0]=10
		2.5	2.68	2.85	V	BOD_VL [1:0]=01
		2.0	2.18	2.35	V	BOD_VL [1:0]=00
V_{BOD}	Brown-out Detector (Rising edge)	4.3	4.52	4.75	V	BOD_VL [1:0]=11
		3.5	3.8	4.05	V	BOD_VL [1:0]=10
		2.5	2.77	3.05	V	BOD_VL [1:0]=01
		2.0	2.25	2.55	V	BOD_VL [1:0]=00

9.4.5 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Reset Voltage	1.6	2	2.4	V	-
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	100	mV	
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms	
t_{POR}	Minimum Time for V_{DD} Stays at VPOR to Ensure Power-on Reset	0.5	-	-	ms	

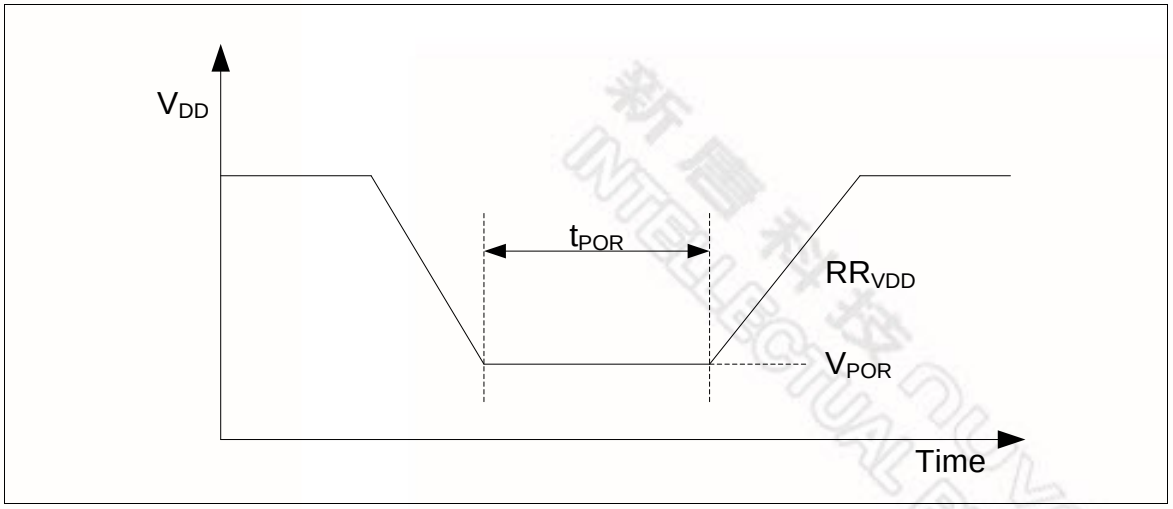


Figure 9-2Power-up Ramp Condition

9.4.6 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.5	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	40	80	μA	AV_{DD}=5V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} -0.1	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD}– 0.1	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{COM}=1.2 V, V_{DIFF}=0.1 V
V_{HYS}	Hysteresis	-	±30	±60	mV	V_{COM}=1.2 V
T_{STB}	Stable time	-	-	1	μs	

9.5 Flash DC Electrical Characteristics

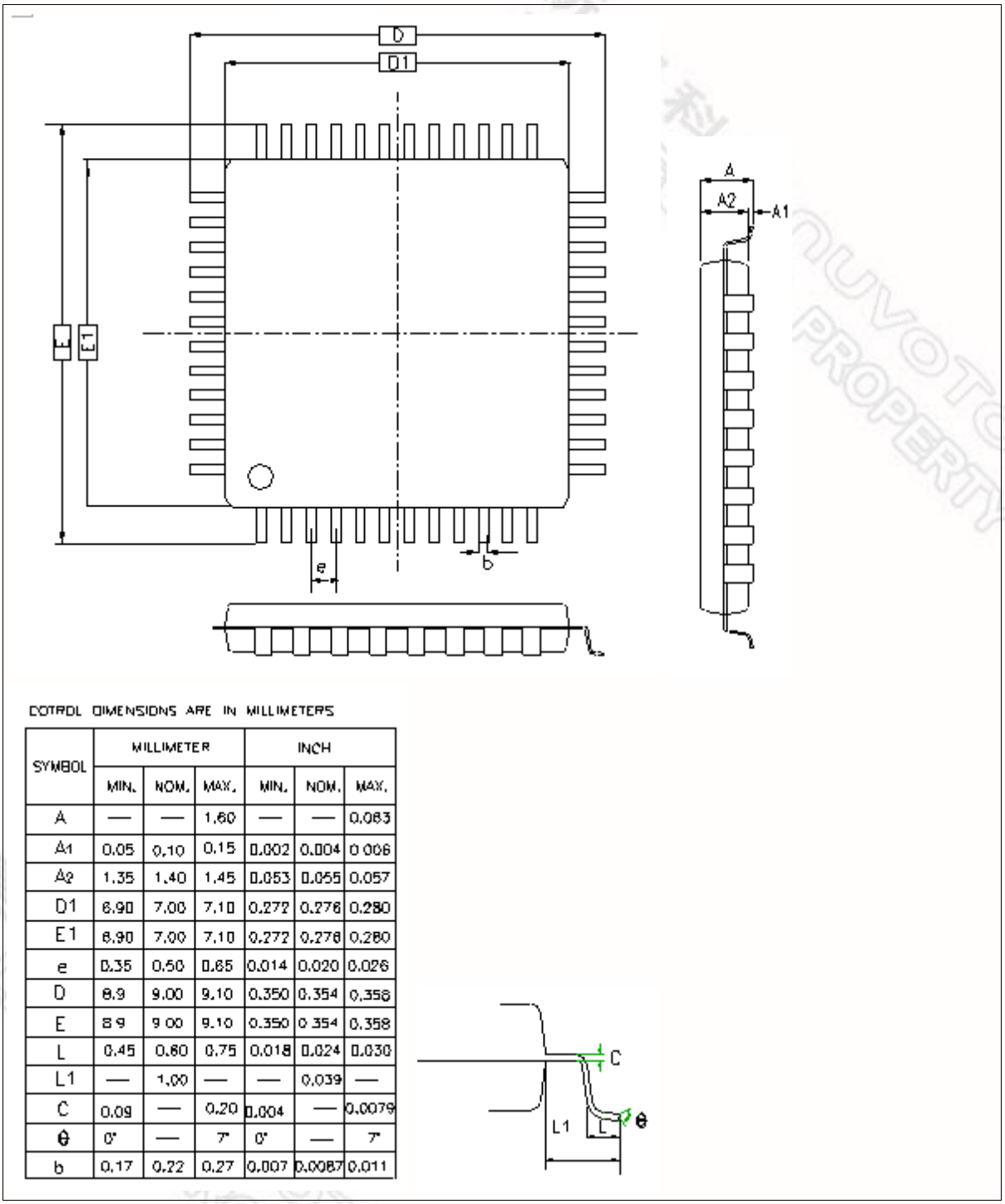
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.62	1.8	1.98	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A =85℃
T_{ERASE}	Page Erase Time	-	20	-	ms	
T_{PROG}	Program Time	-	60	-	us	
I_{DD1}	Read Current	-	6	-	mA	
I_{DD2}	Program Current	-	8	-	mA	
I_{DD3}	Erase Current	-	12	-	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
3. Guaranteed by design, not test in production.

10 PACKAGE DIMENSIONS

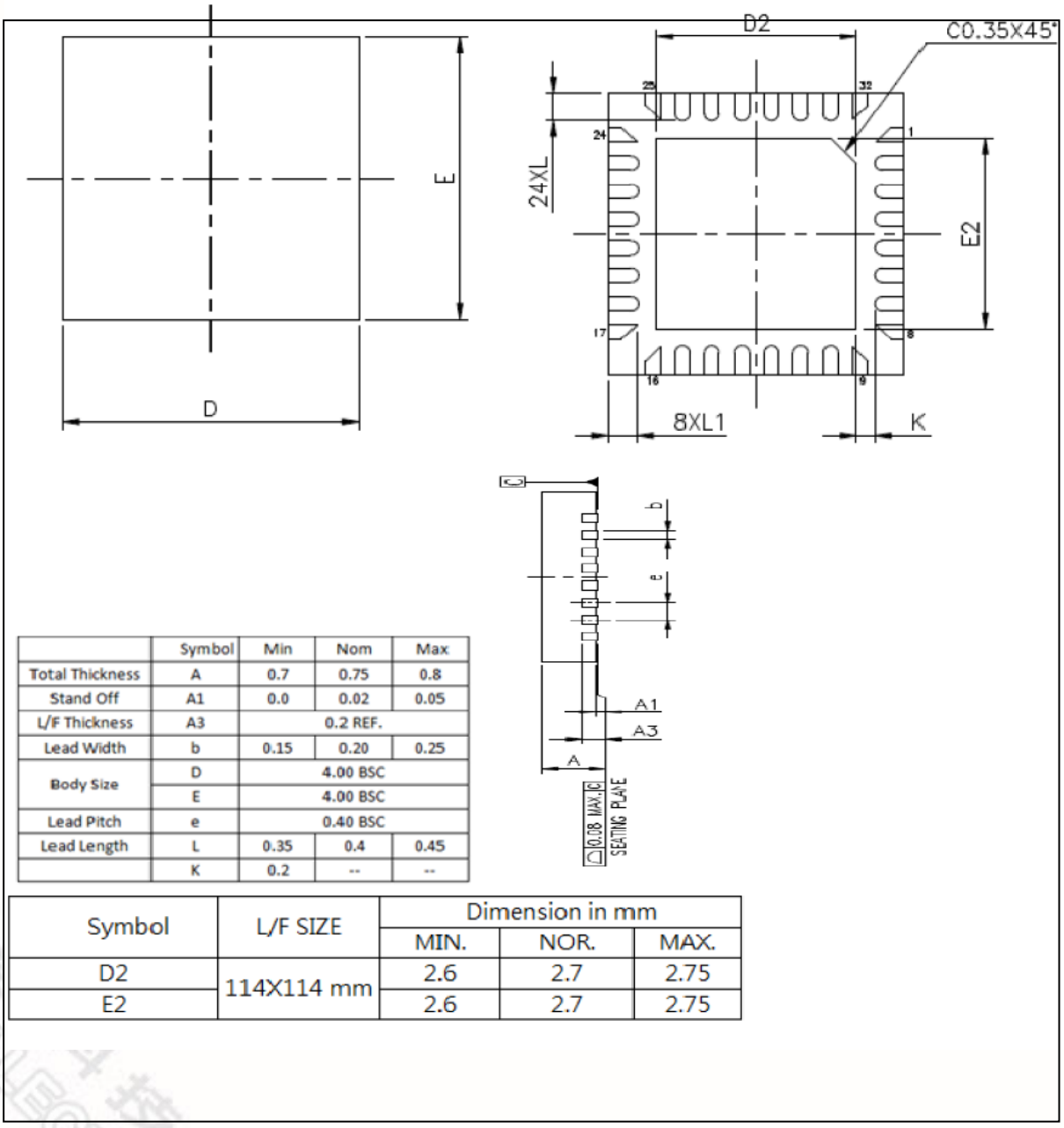
10.1 48-pin LQFP



CONTROL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.026
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.004	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

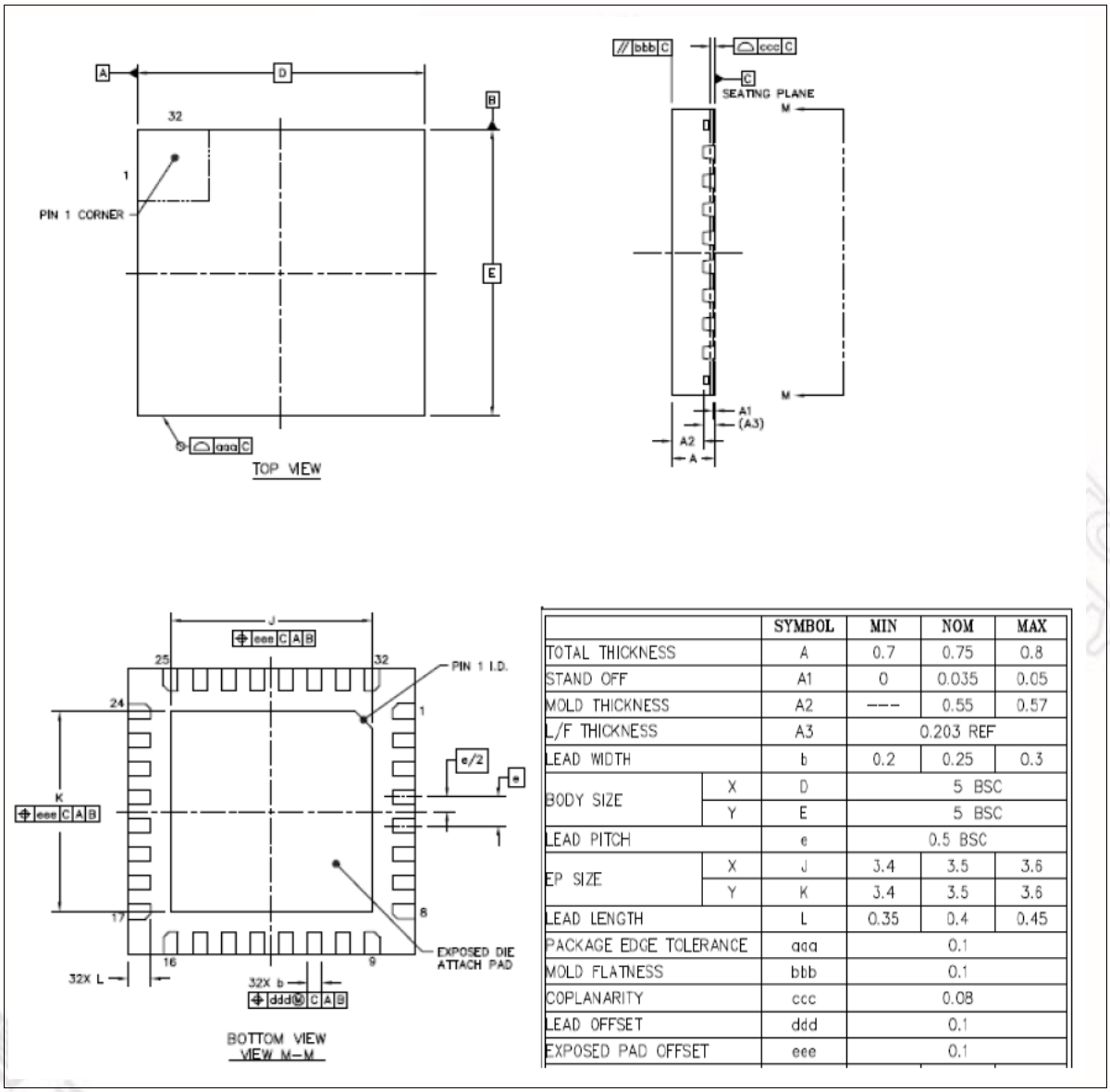
10.2 33-pin QFN (4 mm x 4 mm)



	Symbol	Min	Nom	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0.0	0.02	0.05
L/F Thickness	A3		0.2 REF.	
Lead Width	b	0.15	0.20	0.25
Body Size	D		4.00 BSC	
	E		4.00 BSC	
Lead Pitch	e		0.40 BSC	
Lead Length	L	0.35	0.4	0.45
	K	0.2	--	--

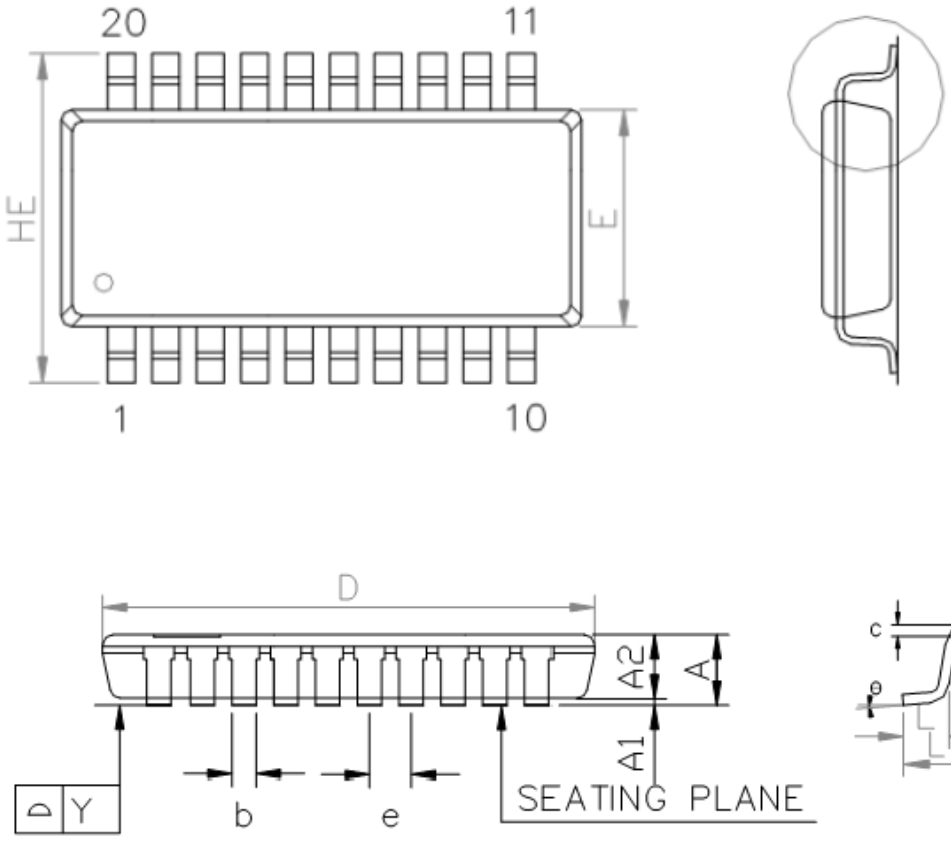
Symbol	L/F SIZE	Dimension in mm		
		MIN.	NOR.	MAX.
D2	114X114 mm	2.6	2.7	2.75
E2		2.6	2.7	2.75

10.3 33-pin QFN (5 mm x 5 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

10.4 20-pin TSSOP



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	—	0.30	0.007	—	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	—	0.20	0.004	—	0.008
θ	0°	—	8°	0°	—	8°
Y	0.10 BASIC			0.004 BASIC		

11 REVISION HISTORY

Revision	Date	Description
1.00	Oct. 18, 2013	Preliminary version
1.01	May 20, 2014	Supported the Mini54FHC for NuMicro Mini51 series.