# Low Skew, 1-TO-16 LVCMOS/LVTTL Fanout Buffer

# 83115

DATA SHEET

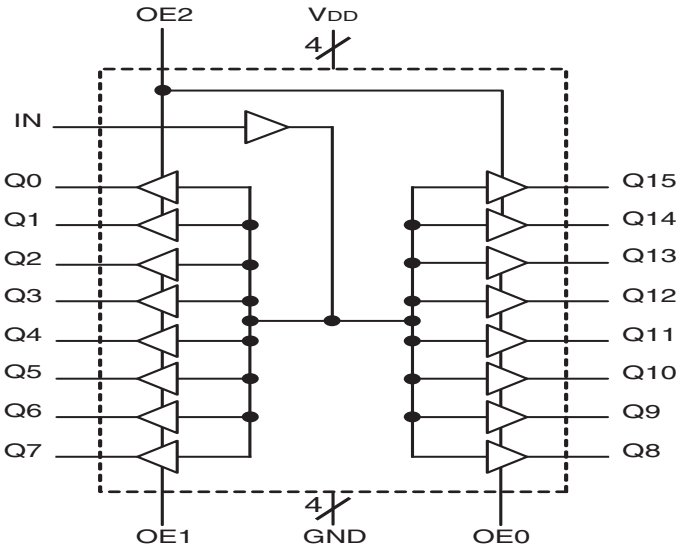
## General Description

The 83115 is a low skew, 1-to-16 LVCMOS/ LVTTL Fanout Buffer from IDT. The 83115 single-ended clock input accepts LVCMOS or LVTTL input levels. The 83115 operates at full 3.3V supply mode over the commercial temperature range. Guaranteed output and part-to-part skew characteristics make the 83115 ideal for those clock distribution applications demanding well defined performance and repeatability.

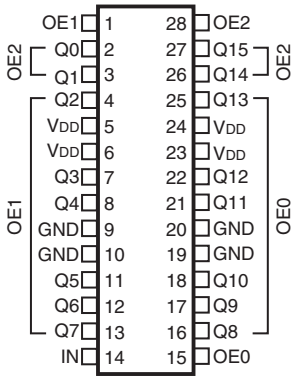
## Features

- Sixteen LVCMOS / LVTTL outputs, 15Ω output impedance
- One LVCMOS / LVTTL clock input
- Maximum output frequency: 200MHz
- All inputs are 5V tolerant
- Output skew: 250ps (maximum)
- Part-to-part skew: 800ps (maximum)
- Additive phase jitter, RMS: 0.09ps (typical)
- Full 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram




## Pin Assignment




**83115**

**28-Lead SSOP, 150mil**
**9.9mm x 3.9mm x 1.5mm package body**
**R Package**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | OE1 | Input | Pullup | Output enable pin. When LOW, forces outputs Q[2:7] to Hi-Z state. 5V tolerant. LVCMOS/LVTTL interface levels. See Table 3. |
| 2, 3, 4, 7, 8, 11, 12, 13, 16, 17, 18, 21, 22, 25, 26, 27 | Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15 | Output | | Single-ended clock outputs. 15Ω output impedance. LVCMOS/LVTTL interface levels. |
| 5, 6, 23, 24 | $V_{DD}$ | Power | | Positive supply pins. |
| 9, 10, 19, 20 | GND | Power | | Power supply ground. |
| 14 | IN | Input | Pulldown | Single-ended clock input. 5V tolerant. LVCMOS/LVTTL interface levels. |
| 15 | OE0 | Input | Pullup | Output enable pin. When LOW, forces outputs Q[8:13] to Hi-Z state. 5V tolerant. LVCMOS/LVTTL interface levels. See Table 3. |
| 28 | OE2 | Input | Pullup | Output enable pin. When LOW, forces outputs Q[0:1] and Q[14:15] to Hi-Z state. 5V tolerant. LVCMOS/LVTTL interface levels. See Table 3. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |
| $C_{PD}$ | Power Dissipation Capacitance (per output); NOTE 1 | $V_{DD}$ = 3.465V | | 11 | | pF |
| $R_{OUT}$ | Output Impedance | $V_{DD}$ = 3.3V | | 15 | | Ω |

## Function Tables

**Table 3. OEx Function Table**

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| OE0 | OE1 | OE2 | Control OE2 Q[0:1], Q[14:15] | Control OE1 Q[2:7] | Control OE0 Q[8:13] |
| 0 | 0 | 0 | Hi-Z | Hi-Z | Hi-Z |
| 0 | 0 | 1 | Active | Hi-Z | Hi-Z |
| 0 | 1 | 0 | Hi-Z | Active | Hi-Z |
| 0 | 1 | 1 | Active | Active | Hi-Z |
| 1 | 0 | 0 | Hi-Z | Hi-Z | Active |
| 1 | 0 | 1 | Active | Hi-Z | Active |
| 1 | 1 | 0 | Hi-Z | Active | Active |
| 1 | 1 | 1 | Active | Active | Active |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $V_O$ | -0.5V to $V_{DD}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 49°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | | 50 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | OE0:OE2 | | 2 | | $V_{DD}$ + 0.3 | V |
| | | IN | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | OE0:OE2 | | -0.3 | | 0.8 | V |
| | | IN | | -0.3 | | 1.3 | V |
| $I_{IH}$ | Input High Current | OE0:OE2 | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 5 | µA |
| | | IN | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | OE0:OE2 | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| | | IN | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{DD}$ = 3.3V ± 5% | 2.6 | | | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{DD}$ = 3.3V ± 5% | | | 0.5 | V |
| $I_{OZL}$ | Output Hi-Z Current Low | | | | | 5 | µA |
| $I_{OZH}$ | Output Hi-Z Current High | | | | | 5 | µA |

NOTE 1: Outputs terminated with 50Ω to $V_{DD}$/2. See Parameter Measurement Information, *Output Load Test Circuit diagram.*

# AC Electrical Characteristics

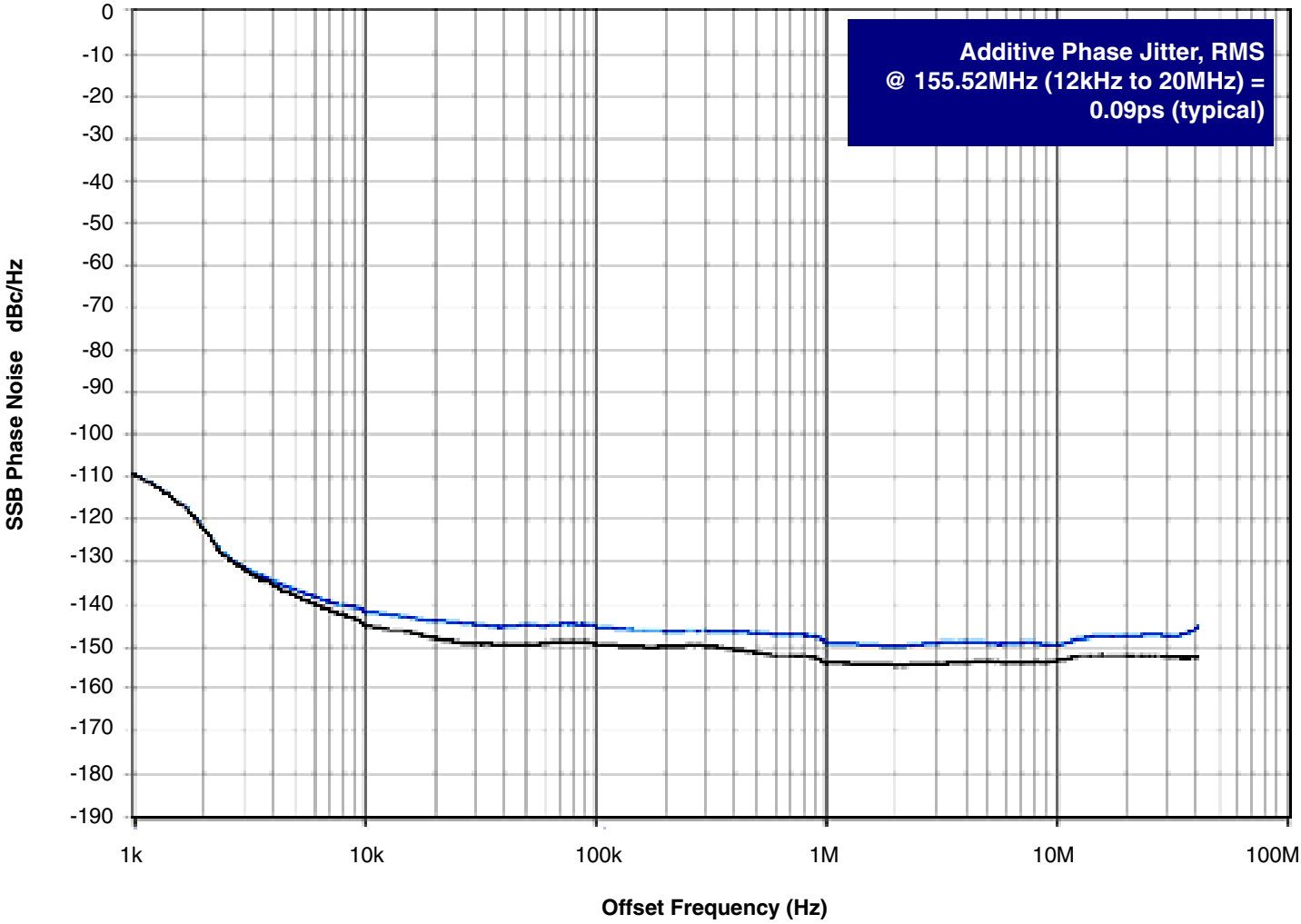
**Table 5. AC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C

| Parameter | Symbol | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 200 | MHz |
| *t*jit( | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | Integration Range: 12kHz – 20MHz | | 0.09 | | ps |
| $tp_{LH}$ | Propagation Delay; NOTE 1 | $f \leq$ 200MHz | 1.7 | 2.4 | 3.1 | ns |
| *t*sk(o) | Output Skew; NOTE 2, 4 | Measured on the Rising Edge @ $V_{DD}$/2 | | 150 | 250 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 4 | Measured on the Rising Edge @ $V_{DD}$/2 | | | 800 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time4 | 20% to 80% | 400 | | 800 | ps |
| odc | Output Duty Cycle | | 45 | | 55 | % |
| $t_{EN}$ | Output Enable Time | | | | 20 | ns |
| $t_{DIS}$ | Output Disable Time | | | | 20 | ns |

All parameters measured at $f_{MAX}$ unless noted otherwise.
NOTE 1: Measured from $V_{DD}$/2 of the input to $V_{DD}$/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}$/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}$/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

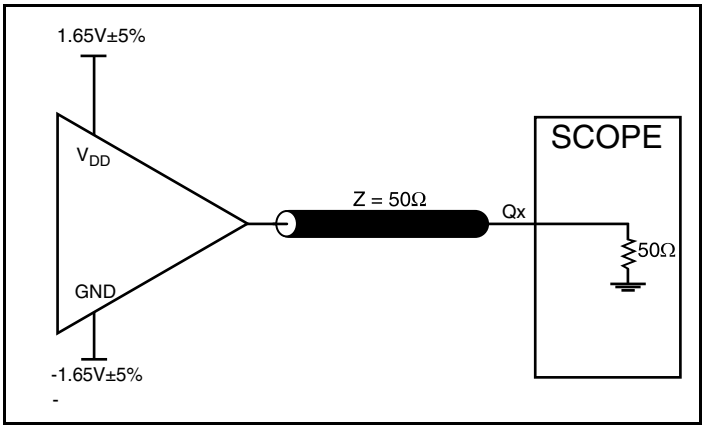
## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

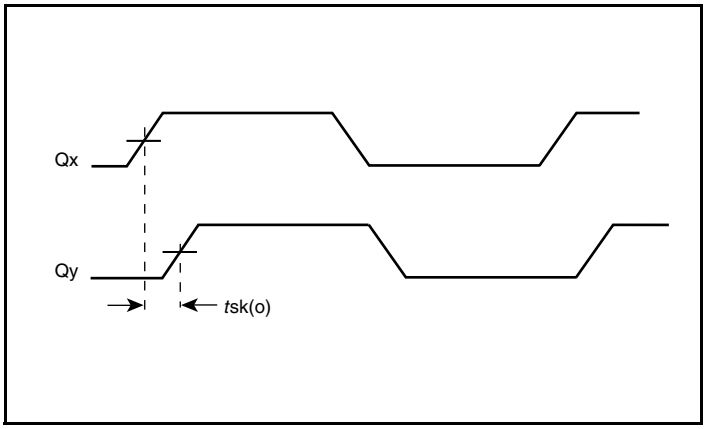



As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

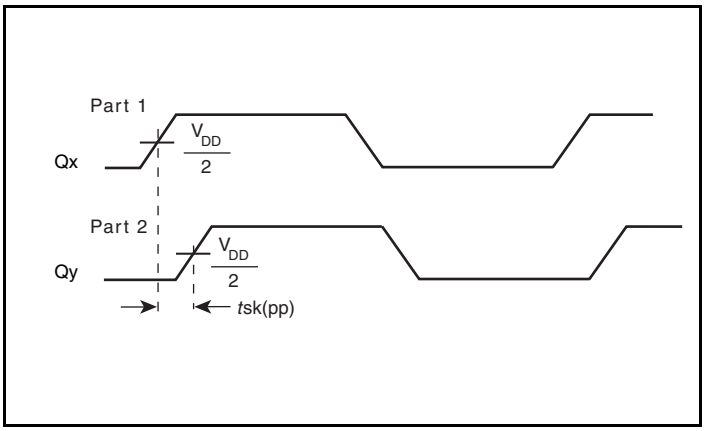
## Parameter Measurement Information



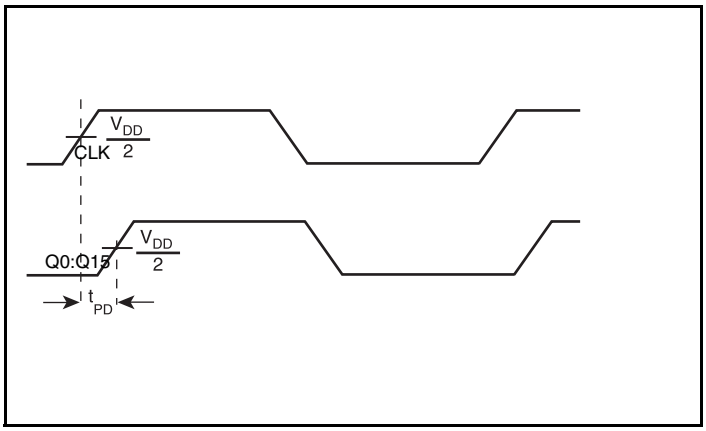

**3.3V Output Load AC Test Circuit**



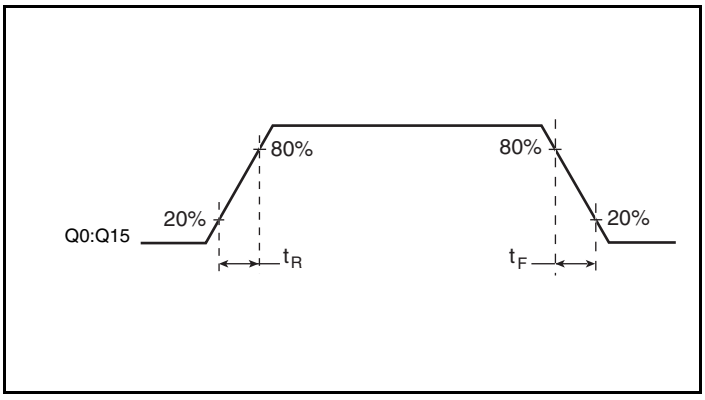

**Output Skew**



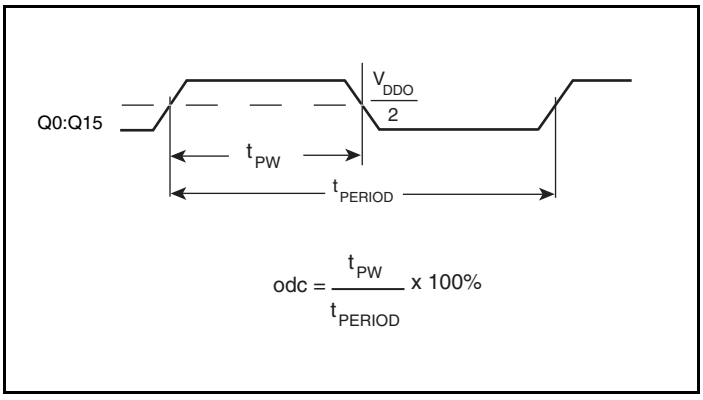

**Part-to-Part Skew**




**Propagation Delay**




**Output Rise/Fall Time**




**Output Duty Cycle/Pulse Width/Period**

# Application Information

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

# Reliability Information

**Table 6. $\theta_{JA}$ vs. Air Flow Table for a 28 Lead SSOP, 150MIL**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 49°C/W | 36°C/W | 30°C/W |

## Transistor Count

The transistor count for 83115: 985

# Package Outline and Package Dimension

## Package Outline - G Suffix for 28 Lead SSOP

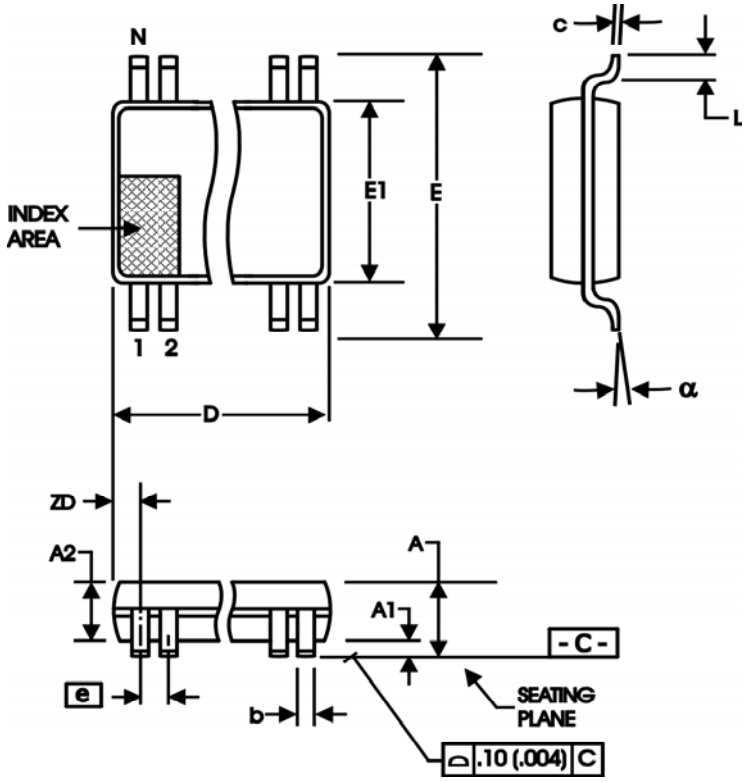



**Table 7. Package Dimensions for 28 Lead SSOP**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 28 | |
| **A** | 1.35 | 1.75 |
| **A1** | 0.10 | 0.25 |
| **A2** | | 1.50 |
| **b** | 0.20 | 0.30 |
| **c** | 0.18 | 0.25 |
| **D** | 9.80 | 10.00 |
| **E** | 5.80 | 6.20 |
| **E1** | 3.80 | 4.00 |
| **e** | 0.635 Basic | |
| **L** | 0.40 | 1.27 |
| α | 0° | 8° |
| **ZD** | 0.84 Ref | |

Reference Document: JEDEC Publication 95, MO-137

# Ordering Information

**Table 8. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| ICS83115BRLF | ICS83115BRLF | “Lead-Free” 28 Lead SSOP | Tube | 0°C to 70°C |
| ICS83115BRLFT | ICS83115BRLF | “Lead-Free” 28 Lead SSOP | Tape & Reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| C | T5 | 4 | AC Characteristics Table - changed Output Rise/Fall Time limits from 650ps min./1150ps max. to 400ps min./800ps max. | 3/14/08 |
| C | T8 | 9 | Ordering Information - removed leaded devices.<br>Updated data sheet format. | 3/20/15 |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