

## FEATURES

- Overvoltage protection up to  $-55\text{ V}$  and  $+55\text{ V}$**
- Power-off protection up to  $-55\text{ V}$  and  $+55\text{ V}$**
- Overvoltage detection on source pins**
- Interrupt flags indicate fault status**
- Low on resistance:  $10\ \Omega$  (typical)**
  - On-resistance flatness of  $0.5\ \Omega$  (maximum)**
- 4 kV human body model (HBM) ESD rating**
- Latch-up immune under any circumstance**
- Known state without digital inputs present**
- $V_{SS}$  to  $V_{DD}$  analog signal range**
  - $\pm 5\text{ V}$  to  $\pm 22\text{ V}$  dual supply operation**
  - 8 V to 44 V single-supply operation**
  - Fully specified at  $\pm 15\text{ V}$ ,  $\pm 20\text{ V}$ , 12 V, and 36 V**

## APPLICATIONS

- Analog input/output modules**
- Process control/distributed control systems**
- Data acquisition**
- Instrumentation**
- Avionics**
- Automatic test equipment**
- Communication systems**
- Relay replacement**

## GENERAL DESCRIPTION

The [ADG5404F](#) is an analog multiplexer composed of four single channels with fault protected inputs. The [ADG5404F](#) switches one of the four inputs to a common drain, D, as determined by the 2-bit binary address lines (A0 and A1). An enable digital input, EN, is used to disable all the switches. Each channel conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. The digital inputs are compatible with 3 V logic inputs over the full operating supply range.

When no power supplies are present, the switch remains in the off condition, and the channel inputs are high impedance. Under normal operating conditions, if the analog input signal levels on any  $S_x$  pin exceed  $V_{DD}$  or  $V_{SS}$  by a threshold voltage,  $V_T$ , the channel turns off and that  $S_x$  pin becomes high impedance. If the channel is on, the drain pin reacts according to the drain response (DR) input pin. If the DR pin is left floating or pulled high, the drain remains high impedance and floats. If the DR pin is pulled low, the drain pulls to the exceeded rail. Input signal levels up to  $+55\text{ V}$  or  $-55\text{ V}$  relative to ground are blocked, in both the powered and unpowered conditions.

Rev. B

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## FUNCTIONAL BLOCK DIAGRAM

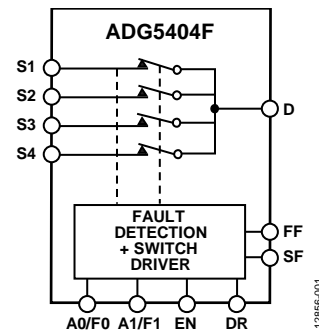


Figure 1.

The low on resistance of the [ADG5404F](#), combined with on-resistance flatness over a significant portion of the signal range, makes it an ideal solution for data acquisition and gain switching applications where excellent linearity and low distortion are critical.

Note that, throughout this data sheet, the dual function pin names are referenced only by the relevant function where applicable. See the Pin Configurations and Function Descriptions for full pin names and function descriptions.

## PRODUCT HIGHLIGHTS

1. Source pins are protected against voltages greater than the supply rails, up to  $-55\text{ V}$  and  $+55\text{ V}$ .
2. Source pins are protected against voltages between  $-55\text{ V}$  and  $+55\text{ V}$  in an unpowered state.
3. Overvoltage detection with digital output indicates operating state of switches.
4. Trench isolation guards against latch-up.
5. Optimized for low on resistance and on-resistance flatness.
6. The [ADG5404F](#) operates from a dual supply of  $\pm 5\text{ V}$  up to  $\pm 22\text{ V}$ , or a single power supply of 8 V up to 44 V.

# ADG5404F\* PRODUCT PAGE QUICK LINKS

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADG5404F Evaluation Board

## DOCUMENTATION

### Data Sheet

- Fault Protection and Detection, 10  $\Omega$  RON, 4-Channel Multiplexer Data Sheet

### User Guides

- UG-790: Evaluation Board for the ADG5404F Overvoltage Protected 4:1 Mux

## REFERENCE MATERIALS

### Press

- Analog Devices Introduces Industry's First Analog Fault Detection and Protection Switch Family for Analog Input/Output Modules in Harsh Environments

### Technical Articles

- Replacing Discrete Protection Components with Overvoltage Fault Protected Analog Switches

## DESIGN RESOURCES

- ADG5404F Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADG5404F EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

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### 4/15—Rev. 0 to Rev. A

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### 12/14—Revision 0: Initial Version

## SPECIFICATIONS

## ±15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $C_{DECOUPLING} = 0.1\text{ }\mu\text{F}$ , unless otherwise noted.

Table 1.

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	$V_{DD} = 13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$ , see Figure 31
On Resistance, $R_{ON}$	10			$\Omega$ typ	Voltage on the Sx pins ( $V_S$ ) = $\pm 10\text{ V}$ , $I_S = -10\text{ mA}$
	11.2	14	16.5	$\Omega$ max	
	9.5			$\Omega$ typ	$V_S = \pm 9\text{ V}$ , $I_S = -10\text{ mA}$
	10.7	13.5	16	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.65			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$
	0.9	1.05	1.2	$\Omega$ max	
	0.65			$\Omega$ typ	$V_S = \pm 9\text{ V}$ , $I_S = -10\text{ mA}$
	0.9	1.05	1.2	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.6			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$
	0.9	1.1	1.1	$\Omega$ max	
	0.1			$\Omega$ typ	$V_S = \pm 9\text{ V}$ , $I_S = -10\text{ mA}$
	0.4	0.5	0.5	$\Omega$ max	
Threshold Voltage, $V_T$	0.7			V typ	See Figure 27
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
	$\pm 1.5$	$\pm 5.0$	$\pm 21$	nA max	$V_S = \pm 10\text{ V}$ , voltage on the D pin ( $V_D$ ) = $\mp 10\text{ V}$ , see Figure 32
Drain Off Leakage, $I_D$ (Off)	$\pm 0.3$			nA typ	$V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ , see Figure 32
	$\pm 1.5$	$\pm 16.0$	$\pm 66$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.3$			nA typ	$V_S = V_D = \pm 10\text{ V}$ , see Figure 33
	$\pm 1.5$	$\pm 14.0$	$\pm 56$	nA max	
<b>FAULT</b>					
Source Leakage Current, $I_S$ With Overvoltage			$\pm 81$	$\mu\text{A}$ typ	$V_{DD} = 16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 36
Power Supplies Grounded or Floating			$\pm 44$	$\mu\text{A}$ typ	$V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$ , $EN = 0\text{ V}$ or floating, $Ax = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$ , see Figure 37
Drain Leakage Current, $I_D$ With Overvoltage	$\pm 6$			nA typ	$DR = \text{floating or } > 2\text{ V}$
	$\pm 15$	$\pm 35$	$\pm 80$	nA max	$V_{DD} = 16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 36
Power Supplies Grounded	$\pm 10$			nA typ	$V_{DD} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , $EN = 0\text{ V}$ , see Figure 37
	$\pm 30$	$\pm 50$	$\pm 100$	nA max	
Power Supplies Floating	$\pm 10$	$\pm 10$	$\pm 10$	$\mu\text{A}$ typ	$V_{DD} = \text{floating}$ , $V_{SS} = \text{floating}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , $EN = 0\text{ V}$ , see Figure 37
<b>DIGITAL INPUTS/OUTPUTS</b>					
Input Voltage High, $V_{INH}$			2.0	V min	
Input Voltage Low, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	$\pm 0.7$			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 1.2$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	6.0			pF typ	
Output Voltage High, $V_{OH}$	2.0			V min	
Output Voltage Low, $V_{OL}$	0.8			V max	

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{\text{TRANSITION}}$	400			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	540	555	570	ns max	$V_S = 10 \text{ V}$ , see Figure 47
$t_{\text{ON}} (\text{EN})$	430			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	535	555	575	ns max	$V_S = 10 \text{ V}$ , see Figure 46
$t_{\text{OFF}} (\text{EN})$	180			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	225	230	235	ns max	$V_S = 10 \text{ V}$ , see Figure 46
Break-Before-Make Time Delay, $t_D$	320			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
			185	ns min	$V_S = 10 \text{ V}$ , see Figure 45
Overvoltage Response Time, $t_{\text{RESPONSE}}$	600			ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 40
	775	820	840	ns max	
Overvoltage Recovery Time, $t_{\text{RECOVERY}}$	700			ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 41
	1000	1050	1100	ns max	
Interrupt Flag Response Time, $t_{\text{DIGRESP}}$	85		115	ns typ	$C_L = 12 \text{ pF}$ , see Figure 42
Interrupt Flag Recovery Time, $t_{\text{DIGREC}}$	60		85	$\mu\text{s}$ typ	$C_L = 12 \text{ pF}$ , see Figure 43
	600			ns typ	$C_L = 12 \text{ pF}$ , $R_{\text{PULLUP}} = 1 \text{ k}\Omega$ , see Figure 44
Charge Injection, $Q_{\text{INJ}}$	680			pC typ	$V_S = 0 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ , see Figure 48
Off Isolation	-72			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 34
Channel to Channel Crosstalk	-72			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 35
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	$R_L = 10 \text{ k}\Omega$ , $V_S = 15 \text{ V p-p}$ , $f = 20 \text{ Hz to } 20 \text{ kHz}$ , see Figure 39
-3 dB Bandwidth	108			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , see Figure 38
Insertion Loss	-0.9			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 38
Source Capacitance ( $C_S$ ), Off	11			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
Drain Capacitance ( $C_D$ ), Off	51			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (On), $C_S$ (On)	63			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
<b>POWER REQUIREMENTS</b>					
					$V_{\text{DD}} = 16.5 \text{ V}$ , $V_{\text{SS}} = -16.5 \text{ V}$ , $\text{GND} = 0 \text{ V}$ , digital inputs = 0 V, 5 V, or $V_{\text{DD}}$
Normal Mode					
$I_{\text{DD}}$	0.9			mA typ	
	1.2		1.3	mA max	
$I_{\text{GND}}$	0.4			mA typ	
	0.55		0.6	mA max	
$I_{\text{SS}}$	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					$V_S = \pm 55 \text{ V}$
$I_{\text{DD}}$	1.2			mA typ	
	1.6		1.8	mA max	
$I_{\text{GND}}$	0.8			mA typ	
	1.0		1.1	mA max	
$I_{\text{SS}}$	0.5			mA typ	Digital inputs = 5 V
	1.0		1.8	mA max	$V_S = \pm 55 \text{ V}$ , $V_D = 0 \text{ V}$
$V_{\text{DD}}/V_{\text{SS}}$			$\pm 5$	V min	$\text{GND} = 0 \text{ V}$
			$\pm 22$	V max	$\text{GND} = 0 \text{ V}$

<sup>1</sup> Guaranteed by design. Not subject to production test.

**±20 V DUAL SUPPLY**

$V_{DD} = 20\text{ V} \pm 10\%$ ,  $V_{SS} = -20\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $C_{DECOUPLING} = 0.1\text{ }\mu\text{F}$ , unless otherwise noted.

**Table 2.**

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	$V_{DD} = 18\text{ V}$ , $V_{SS} = -18\text{ V}$ , see Figure 31
On Resistance, $R_{ON}$	10			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$
	11.5	14.5	16.5	$\Omega$ max	
	9.5			$\Omega$ typ	$V_S = \pm 13.5\text{ V}$ , $I_S = -10\text{ mA}$
	11	14	16.5	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.65			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$
	0.9	1.05	1.2	$\Omega$ max	
	0.65			$\Omega$ typ	$V_S = \pm 13.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.9	1.05	1.2	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.0			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$
	1.4	1.5	1.5	$\Omega$ max	
	0.1			$\Omega$ typ	$V_S = \pm 13.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.4	0.5	0.5	$\Omega$ max	
Threshold Voltage, $V_T$	0.7			V typ	See Figure 27
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 22\text{ V}$ , $V_{SS} = -22\text{ V}$
	$\pm 1.5$	$\pm 5.0$	$\pm 21$	nA max	$V_S = \pm 15\text{ V}$ , $V_D = \pm 15\text{ V}$ , see Figure 32
Drain Off Leakage, $I_D$ (Off)	$\pm 0.3$			nA typ	$V_S = \pm 15\text{ V}$ , $V_D = \pm 15\text{ V}$ , see Figure 32
	$\pm 1.5$	$\pm 16.0$	$\pm 66$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.3$			nA typ	$V_S = V_D = \pm 15\text{ V}$ , see Figure 33
	$\pm 1.5$	$\pm 14.0$	$\pm 56$	nA max	
<b>FAULT</b>					
Source Leakage Current, $I_S$ With Overvoltage			$\pm 85$	$\mu\text{A}$ typ	$V_{DD} = +22\text{ V}$ , $V_{SS} = -22\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 36
Power Supplies Grounded or Floating			$\pm 44$	$\mu\text{A}$ typ	$V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$ , $I_{NX} = 0\text{ V}$ or floating, $A_X = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$ , see Figure 37
Drain Leakage Current, $I_D$ With Overvoltage	$\pm 400$			nA typ	$DR = \text{floating or } > 2\text{ V}$ $V_{DD} = +22\text{ V}$ , $V_{SS} = -22\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 36
	$\pm 1.5$	$\pm 1.5$	$\pm 1.5$	$\mu\text{A}$ max	
Power Supplies Grounded	$\pm 10$			nA typ	$V_{DD} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S =$ $\pm 55\text{ V}$ , $EN = 0\text{ V}$ , see Figure 37
	$\pm 30$	$\pm 50$	$\pm 100$	nA max	
Power Supplies Floating	$\pm 10$	$\pm 10$	$\pm 10$	$\mu\text{A}$ typ	$V_{DD} = \text{floating}$ , $V_{SS} = \text{floating}$ , $GND =$ $0\text{ V}$ , $V_S = \pm 55\text{ V}$ , $EN = 0\text{ V}$ , see Figure 37
<b>DIGITAL INPUTS</b>					
Input Voltage High, $V_{INH}$			2.0	V min	
Input Voltage Low, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.7			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			1.2	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	6.0			pF typ	
Output Voltage High, $V_{OH}$	2.0			V min	
Output Voltage Low, $V_{OL}$	0.8			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{\text{TRANSITION}}$	405			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	540	555	570	ns max	$V_S = 10 \text{ V}$ , see Figure 47
$t_{\text{ON}} (\text{EN})$	430			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	535	560	585	ns max	$V_S = 10 \text{ V}$ , see Figure 46
$t_{\text{OFF}} (\text{EN})$	170			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	205	210	215	ns max	$V_S = 10 \text{ V}$ , see Figure 46
Break-Before-Make Time Delay, $t_D$	330			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
			200	ns min	$V_S = 10 \text{ V}$ , see Figure 45
Overvoltage Response Time, $t_{\text{RESPONSE}}$	480			ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 40
	640	680	700	ns max	
Overvoltage Recovery Time, $t_{\text{RECOVERY}}$	800			ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 41
	1150	1250	1500	ns max	
Interrupt Flag Response Time, $t_{\text{DIGRESP}}$	85		115	ns typ	$C_L = 12 \text{ pF}$ , see Figure 42
Interrupt Flag Recovery Time, $t_{\text{DIGREC}}$	60		85	$\mu\text{s}$ typ	$C_L = 12 \text{ pF}$ , see Figure 43
	600			ns typ	$C_L = 12 \text{ pF}$ , $R_{\text{PULLUP}} = 1 \text{ k}\Omega$ , see Figure 44
Charge Injection, $Q_{\text{INJ}}$	695			pC typ	$V_S = 0 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ , see Figure 48
Off Isolation	−73			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 34
Channel to Channel Crosstalk	−73			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 35
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	$R_L = 10 \text{ k}\Omega$ , $V_S = 20 \text{ V p-p}$ , $f = 20 \text{ Hz}$ to $20 \text{ kHz}$ , see Figure 39
−3 dB Bandwidth	110			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , see Figure 38
Insertion Loss	−0.9			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 38
$C_S$ (Off)	11			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (Off)	47			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (On), $C_S$ (On)	61			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$V_{\text{DD}} = 22 \text{ V}$ , $V_{\text{SS}} = -22 \text{ V}$ , digital inputs = 0 V, 5 V, or $V_{\text{DD}}$					
Normal Mode					
$I_{\text{DD}}$	0.9			mA typ	
	1.2		1.3	mA max	
$I_{\text{GND}}$	0.4			mA typ	
	0.55		0.6	mA max	
$I_{\text{SS}}$	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					$V_S = \pm 55 \text{ V}$
$I_{\text{DD}}$	1.2			mA typ	
	1.6		1.8	mA max	
$I_{\text{GND}}$	0.8			mA typ	
	1.0		1.1	mA max	
$I_{\text{SS}}$	0.5			mA typ	Digital inputs = 5 V
	1.0		1.8	mA max	$V_S = \pm 55 \text{ V}$ , $V_D = 0 \text{ V}$
$V_{\text{DD}}/V_{\text{SS}}$			$\pm 5$	V min	GND = 0 V
			$\pm 22$	V max	GND = 0 V

<sup>1</sup> Guaranteed by design. Not subject to production test.

**12 V SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ ,  $C_{DECOUPLING} = 0.1\text{ }\mu\text{F}$ , unless otherwise noted.

**Table 3.**

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 to $V_{DD}$	V	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$ , see Figure 31
On Resistance, $R_{ON}$	22			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	24.5	31	37	$\Omega$ max	
	10			$\Omega$ typ	$V_S = 3.5\text{ V to }8.5\text{ V}$ , $I_S = -10\text{ mA}$
	11.2	14	16.5	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.65			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	1.1	1.2	1.3	$\Omega$ max	
	0.65			$\Omega$ typ	$V_S = 3.5\text{ V to }8.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.9	1.05	1.2	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	14.5	19	23	$\Omega$ max	
	0.6			$\Omega$ typ	$V_S = 3.5\text{ V to }8.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.9	1.1	1.3	$\Omega$ max	
Threshold Voltage, $V_T$	0.7			V typ	See Figure 27
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ , see Figure 32
	$\pm 1.5$	$\pm 5.0$	$\pm 21$	nA max	
Drain Off Leakage, $I_D$ (Off)	$\pm 0.3$			nA typ	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ , see Figure 32
	$\pm 1.5$	$\pm 16.0$	$\pm 66$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.3$			nA typ	$V_S = V_D = 1\text{ V}/10\text{ V}$ , see Figure 33
	$\pm 1.5$	$\pm 14.0$	$\pm 56$	nA max	
<b>FAULT</b>					
Source Leakage Current, $I_S$ With Overvoltage			$\pm 73$	$\mu\text{A}$ typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 36
Power Supplies Grounded or Floating			$\pm 44$	$\mu\text{A}$ typ	$V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$ , $EN = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$ , see Figure 37
Drain Leakage Current, $I_D$ With Overvoltage	$\pm 6$			nA typ	$DR = \text{floating or } >2\text{ V}$ $V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $A_X = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$ , see Figure 36
	$\pm 15$	$\pm 35$	$\pm 80$	nA max	
Power Supplies Grounded	$\pm 10$			nA typ	$V_{DD} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , $EN = 0\text{ V}$ , see Figure 37
	$\pm 30$	$\pm 50$	$\pm 100$	nA max	
Power Supplies Floating	$\pm 10$	$\pm 10$	$\pm 10$	$\mu\text{A}$ typ	$V_{DD} = \text{floating}$ , $V_{SS} = \text{floating}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , $EN = 0\text{ V}$ , see Figure 37
<b>DIGITAL INPUTS</b>					
Input Voltage High, $V_{INH}$			2.0	V min	
Input Voltage Low, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.7			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			1.2	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	6.0			pF typ	
Output Voltage High, $V_{OH}$	2.0			V min	
Output Voltage Low, $V_{OL}$	0.8			V max	



Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{\text{TRANSITION}}$	400			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	545	560	570	ns max	$V_S = 10 \text{ V}$ , see Figure 47
$t_{\text{ON}} (\text{EN})$	430			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	530	545	560	ns max	$V_S = 8 \text{ V}$ , see Figure 46
$t_{\text{OFF}} (\text{EN})$	205			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	255	265	270	ns max	$V_S = 8 \text{ V}$ , see Figure 46
Break-Before-Make Time Delay, $t_D$	290			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
			175	ns min	$V_S = 8 \text{ V}$ , see Figure 45
Overvoltage Response Time, $t_{\text{RESPONSE}}$	700			ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 40
	875	940	975	ns max	
Overvoltage Recovery Time, $t_{\text{RECOVERY}}$	630			ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 41
	780	830	920	ns max	
Interrupt Flag Response Time, $t_{\text{DIGRESP}}$	85		115	ns typ	$C_L = 12 \text{ pF}$ , see Figure 42
Interrupt Flag Recovery Time, $t_{\text{DIGREC}}$	60		85	$\mu\text{s}$ typ	$C_L = 12 \text{ pF}$ , see Figure 43
	600			ns typ	$C_L = 12 \text{ pF}$ , $R_{\text{PULLUP}} = 1 \text{ k}\Omega$ , see Figure 44
Charge Injection, $Q_{\text{INJ}}$	322			pC typ	$V_S = 6 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ , see Figure 48
Off Isolation	-68			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 34
Channel to Channel Crosstalk	-70			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 35
Total Harmonic Distortion Plus Noise, THD + N	0.007			% typ	$R_L = 10 \text{ k}\Omega$ , $V_S = 6 \text{ V p-p}$ , $f = 20 \text{ Hz}$ to $20 \text{ kHz}$ , see Figure 39
-3 dB Bandwidth	90			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , see Figure 38
Insertion Loss	-0.9			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 38
$C_S$ (Off)	14			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (Off)	66			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (On), $C_S$ (On)	76			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$V_{\text{DD}} = 13.2 \text{ V}$ , $V_{\text{SS}} = 0 \text{ V}$ , digital inputs = $0 \text{ V}$ , $5 \text{ V}$ , or $V_{\text{DD}}$					
Normal Mode					
$I_{\text{DD}}$	0.9			mA typ	
	1.2		1.3	mA max	
$I_{\text{GND}}$	0.4			mA typ	
	0.55		0.6	mA max	
$I_{\text{SS}}$	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					$V_S = \pm 55 \text{ V}$
$I_{\text{DD}}$	1.2			mA typ	
	1.6		1.8	mA max	
$I_{\text{GND}}$	0.8			mA typ	
	1.0		1.1	mA max	
$I_{\text{SS}}$	0.5			mA typ	Digital inputs = $5 \text{ V}$
	1.0		1.8	mA max	$V_S = \pm 55 \text{ V}$ , $V_D = 0 \text{ V}$
$V_{\text{DD}}$			8	V min	$\text{GND} = 0 \text{ V}$
			44	V max	$\text{GND} = 0 \text{ V}$

<sup>1</sup> Guaranteed by design. Not subject to production test.

**36 V SINGLE SUPPLY**

$V_{DD} = 36\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ ,  $C_{DECOUPLING} = 0.1\text{ }\mu\text{F}$ , unless otherwise noted.

**Table 4.**

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 to $V_{DD}$	V	$V_{DD} = 32.4\text{ V}$ , $V_{SS} = 0\text{ V}$ , see Figure 31
On Resistance, $R_{ON}$	22			$\Omega$ typ	$V_S = 0\text{ V to }30\text{ V}$ , $I_S = -10\text{ mA}$
	24.5	31	37	$\Omega$ max	
	10			$\Omega$ typ	$V_S = 4.5\text{ V to }28\text{ V}$ , $I_S = -10\text{ mA}$
	11	14	16.5	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.65			$\Omega$ typ	$V_S = 0\text{ V to }30\text{ V}$ , $I_S = -10\text{ mA}$
	1.1	1.2	1.3	$\Omega$ max	
	0.65			$\Omega$ typ	$V_S = 4.5\text{ V to }28\text{ V}$ , $I_S = -10\text{ mA}$
	0.9	1.05	1.2	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			$\Omega$ typ	$V_S = 0\text{ V to }30\text{ V}$ , $I_S = -10\text{ mA}$
	14.5	19	23	$\Omega$ max	
	0.1			$\Omega$ typ	$V_S = 4.5\text{ V to }28\text{ V}$ , $I_S = -10\text{ mA}$
	0.4	0.5	0.5	$\Omega$ max	
Threshold Voltage, $V_T$	0.7			V typ	See Figure 27
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/30\text{ V}$ , $V_D = 30\text{ V}/1\text{ V}$ , see Figure 32
	$\pm 1.5$	$\pm 5.0$	$\pm 21$	nA max	
Drain Off Leakage, $I_D$ (Off)	$\pm 0.3$			nA typ	$V_S = 1\text{ V}/30\text{ V}$ , $V_D = 30\text{ V}/1\text{ V}$ , see Figure 32
	$\pm 1.5$	$\pm 16.0$	$\pm 66$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.3$			nA typ	$V_S = V_D = 1\text{ V}/30\text{ V}$ , see Figure 33
	$\pm 1.5$	$\pm 14.0$	$\pm 56$	nA max	
<b>FAULT</b>					
Source Leakage Current, $I_S$ With Overvoltage			$\pm 68$	$\mu\text{A}$ typ	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = +55\text{ V}$ , $-40\text{ V}$ , see Figure 36
Power Supplies Grounded or Floating			$\pm 44$	$\mu\text{A}$ typ	$V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$ , $A_X = 0\text{ V}$ or floating, $V_S = +55\text{ V}$ , $-40\text{ V}$ , see Figure 37 DR = floating or $>2\text{ V}$
Drain Leakage Current, $I_D$ With Overvoltage	$\pm 6$			nA typ	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = +55\text{ V}$ , $-40\text{ V}$ , see Figure 36
	$\pm 15$	$\pm 35$	$\pm 80$	nA max	
Power Supplies Grounded	$\pm 10$			nA typ	$V_{DD} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = +55\text{ V}$ , $-40\text{ V}$ , $EN = 0\text{ V}$ , see Figure 37
	$\pm 30$	$\pm 50$	$\pm 100$	nA max	
Power Supplies Floating	$\pm 10$	$\pm 10$	$\pm 10$	$\mu\text{A}$ typ	$V_{DD} = \text{floating}$ , $V_{SS} = \text{floating}$ , $GND = 0\text{ V}$ , $V_S = +55\text{ V}$ , $-40\text{ V}$ , $EN = 0\text{ V}$ , see Figure 37
<b>DIGITAL INPUTS</b>					
Input Voltage High, $V_{INH}$			2.0	V min	$V_{IN} = V_{GND}$ or $V_{DD}$
Input Voltage Low, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.7			$\mu\text{A}$ typ	
			1.2	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	6.0			pF typ	
Output Voltage High, $V_{OH}$	2.0			V min	
Output Voltage Low, $V_{OL}$	0.8			V max	

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{\text{TRANSITION}}$	400			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	540	555	570	ns max	$V_S = 10 \text{ V}$ , see Figure 47
$t_{\text{ON}} (\text{EN})$	430			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	530	550	570	ns max	$V_S = 18 \text{ V}$ , see Figure 46
$t_{\text{OFF}} (\text{EN})$	175			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	210	215	220	ns max	$V_S = 18 \text{ V}$ , see Figure 46
Break-Before-Make Time Delay, $t_D$	340			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
			200	ns min	$V_S = 18 \text{ V}$ , see Figure 45
Overvoltage Response Time, $t_{\text{RESPONSE}}$	270			ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 40
	360	375	385	ns max	
Overvoltage Recovery Time, $t_{\text{RECOVERY}}$	1400			ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 41
	1900	2100	2400	ns max	
Interrupt Flag Response Time, $t_{\text{DIGRESP}}$	85		115	ns typ	$C_L = 12 \text{ pF}$ , see Figure 42
Interrupt Flag Recovery Time, $t_{\text{DIGREC}}$	60		85	$\mu\text{s typ}$	$C_L = 12 \text{ pF}$ , see Figure 43
	600			ns typ	$C_L = 12 \text{ pF}$ , $R_{\text{PULLUP}} = 1 \text{ k}\Omega$ , see Figure 44
Charge Injection, $Q_{\text{INJ}}$	588			pC typ	$V_S = 18 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ , see Figure 48
Off Isolation	-72			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 34
Channel to Channel Crosstalk	-73			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 35
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	$R_L = 10 \text{ k}\Omega$ , $V_S = 18 \text{ V p-p}$ , $f = 20 \text{ Hz}$ to $20 \text{ kHz}$ , see Figure 39
-3 dB Bandwidth	108			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , see Figure 38
Insertion Loss	-0.9			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 38
$C_S$ (Off)	11			pF typ	$V_S = 18 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (Off)	48			pF typ	$V_S = 18 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (On), $C_S$ (On)	60			pF typ	$V_S = 18 \text{ V}$ , $f = 1 \text{ MHz}$
<b>POWER REQUIREMENTS</b>					
Normal Mode					$V_{\text{DD}} = 39.6 \text{ V}$ , $V_{\text{SS}} = 0 \text{ V}$ , digital inputs = 0V, 5V, or $V_{\text{DD}}$
$I_{\text{DD}}$	0.9			mA typ	
	1.2		1.3	mA max	
$I_{\text{GND}}$	0.4			mA typ	
	0.55		0.6	mA max	
$I_{\text{SS}}$	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					$V_S = +55 \text{ V}$ , $-40 \text{ V}$
$I_{\text{DD}}$	1.2			mA typ	
	1.6		1.8	mA max	
$I_{\text{GND}}$	0.8			mA typ	
	1.0		1.1	mA max	
$I_{\text{SS}}$	0.5			mA typ	Digital inputs = 5V
	1.0		1.8	mA max	$V_S = +55 \text{ V}$ , $-40 \text{ V}$ , $V_D = 0 \text{ V}$
$V_{\text{DD}}$			8	V min	$\text{GND} = 0 \text{ V}$
			44	V max	$\text{GND} = 0 \text{ V}$

<sup>1</sup> Guaranteed by design. Not subject to production test.

**CONTINUOUS CURRENT**

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
14-Lead TSSOP $\theta_{JA} = 112.6^{\circ}\text{C/W}$	147	95	58	mA max	$V_S = V_{SS} + 4.5\text{ V to }V_{DD} - 4.5\text{ V}$
	115	77	50	mA max	$V_S = V_{SS}\text{ to }V_{DD}$
16-Lead LFCSP $\theta_{JA} = 30.4^{\circ}\text{C/W}$	280	156	75	mA max	$V_S = V_{SS} + 4.5\text{ V to }V_{DD} - 4.5\text{ V}$
	220	130	70	mA max	$V_S = V_{SS}\text{ to }V_{DD}$

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 6.

Parameter	Rating
$V_{DD}$ to $V_{SS}$	48 V
$V_{DD}$ to GND	-0.3 V to +48 V
$V_{SS}$ to GND	-48 V to +0.3 V
$S_x$ to GND	-55 V to +55 V
$S_x$ to $V_{DD}$ or $V_{SS}$	80 V
$V_S$ to $V_D$	80 V
D Pin <sup>1</sup> to GND	$V_{SS} - 0.7\text{ V}$ to $V_{DD} + 0.7\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs to GND	GND - 0.7 V to 48 V or 30 mA, whichever occurs first
Peak Current, $S_x$ or D Pins	363 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, $S_x$ or D Digital Output	Data <sup>2</sup> + 15% GND - 0.7 V to 6 V or 30 mA, whichever occurs first
D Pin, Overvoltage State, DR = GND, Load Current	1 mA
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, $\theta_{JA}$	
14-Lead TSSOP, Thermal Impedance (4-Layer Board)	112.6°C/W
16-Lead LFCSP, Thermal Impedance (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb-Free	As per JEDEC J-STD-020
ESD Rating, Human Body Model (HBM): ANSI/ESD STM5.1-2007	
Input/Output (I/O) Port to Supplies	4 kV
I/O Port to I/O Port	4 kV
All Other Pins	4 kV

<sup>1</sup> Overvoltages at the D pin are clamped by internal diodes. Limit current to the maximum ratings given.

<sup>2</sup> See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

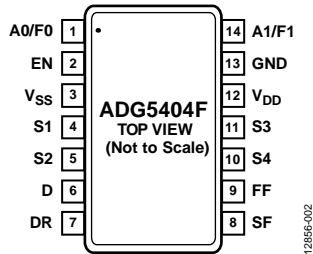
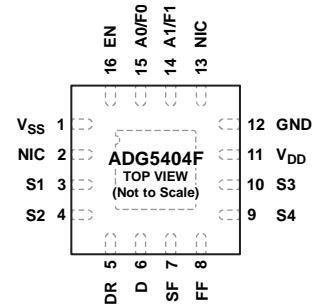


Figure 2. TSSOP Pin Configuration



**NOTES**

1. NIC = NOT INTERNALLY CONNECTED.
2. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE,  $V_{SS}$ .

Figure 3. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	A0/F0 <sup>1</sup>	Logic Control Input (A0). Decoder for the SF Pin (F0).
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic control inputs determine the on switches.
3	1	$V_{SS}$	Most Negative Power Supply Potential.
4	3	S1	Overvoltage Protected Source Terminal 1. This pin can be an input or an output.
5	4	S2	Overvoltage Protected Source Terminal 2. This pin can be an input or an output.
6	6	D	Drain Terminal. This pin can be an input or an output.
7	5	DR	Drain Response Digital Input. Tying this pin to GND enables the drain to pull to $V_{DD}$ or $V_{SS}$ during an overvoltage fault condition. The default condition of the drain is open circuit when the pin is left floating or if it is tied to $V_{DD}$ .
8	7	SF	Specific Fault Digital Output. This pin has a high output when the device is in normal operation and a low output when a fault condition is detected on a specific pin, depending on the state of A0/F0 and A1/F1 (see Table 9).
9	8	FF	Fault Flag Digital Output. This pin has a high output when the device is in normal operation and a low output when a fault condition occurs on any of the Sx inputs.
10	9	S4	Overvoltage Protected Source Terminal 4. This pin can be an input or an output.
11	10	S3	Overvoltage Protected Source Terminal 3. This pin can be an input or an output.
12	11	$V_{DD}$	Most Positive Power Supply Potential.
13	12	GND	Ground (0 V) Reference.
14	14	A1/F1 <sup>1</sup>	Logic Control Input (A1). Decoder for the SF Pin (F1).
N/A <sup>2</sup>	2, 13	NIC	Not internally connected
N/A <sup>2</sup>	17	EP	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, $V_{SS}$ .

<sup>1</sup> Throughout the data sheet, dual function pin names are referenced by the relevant function where applicable.

<sup>2</sup> N/A means not applicable.

**Table 8. Truth Table**

EN	A1	A0	Connected Sx Pin
0	X <sup>1</sup>	X <sup>1</sup>	All switches off
1	0	0	S1
1	0	1	S2
1	1	0	S3
1	1	1	S4

<sup>1</sup> X means don't care.

**Table 9. Fault Diagnostic Output Truth Table**

Switch in Fault <sup>1</sup>	State of Specific Fault Pin (SF) with Decoder Pins (F1, F0)				State of the Fault Flag Pin (FF)
	F1 = 0, F0 = 0	F1 = 0, F0 = 1	F1 = 1, F0 = 0	F1 = 1, F0 = 1	
No switch in fault	1	1	1	1	1
S1	0	1	1	1	0
S2	1	0	1	1	0
S3	1	1	0	1	0
S4	1	1	1	0	0

<sup>1</sup> More than one source input can be in fault at the same time.

TYPICAL PERFORMANCE CHARACTERISTICS

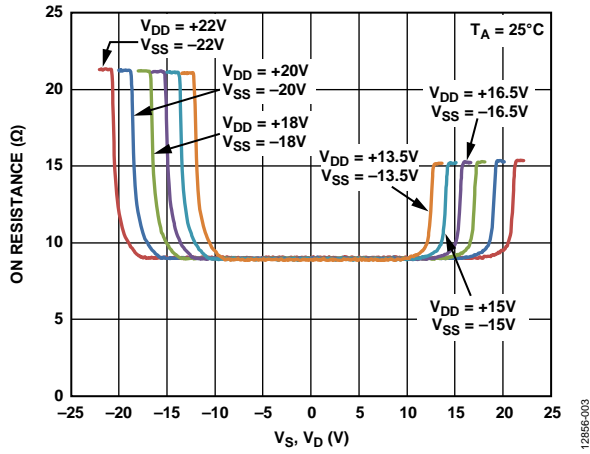


Figure 4.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$ , Dual Supply

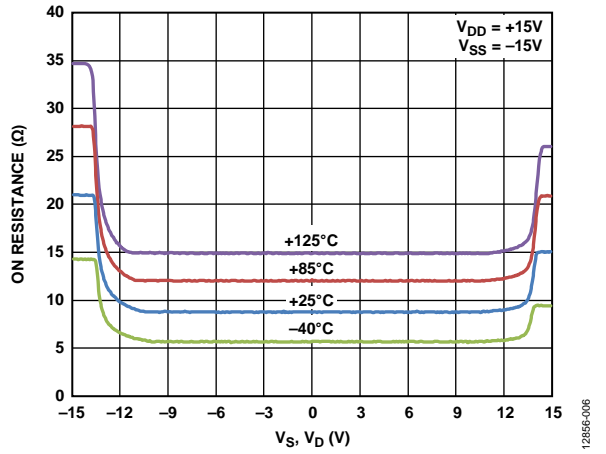


Figure 7.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  for Different Temperatures,  $\pm 15$  V Dual Supply

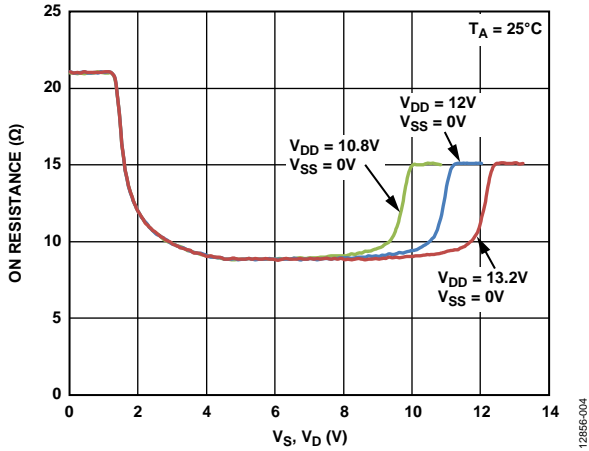


Figure 5.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$ , 12 V Single Supply

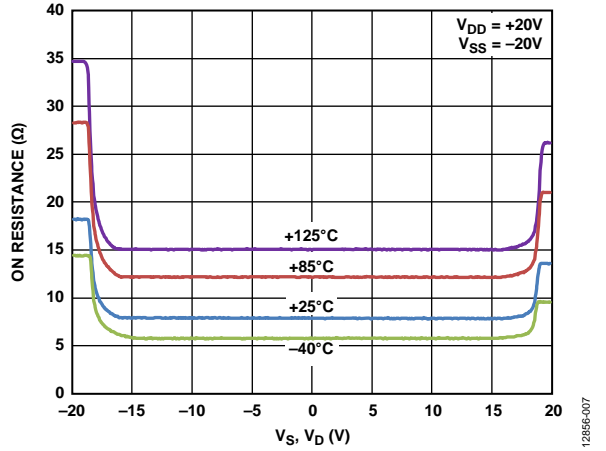


Figure 8.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  for Different Temperatures,  $\pm 20$  V Dual Supply

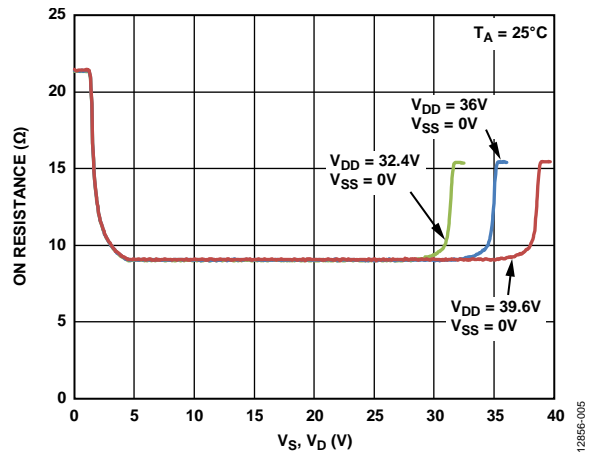


Figure 6.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$ , 36 V Single Supply

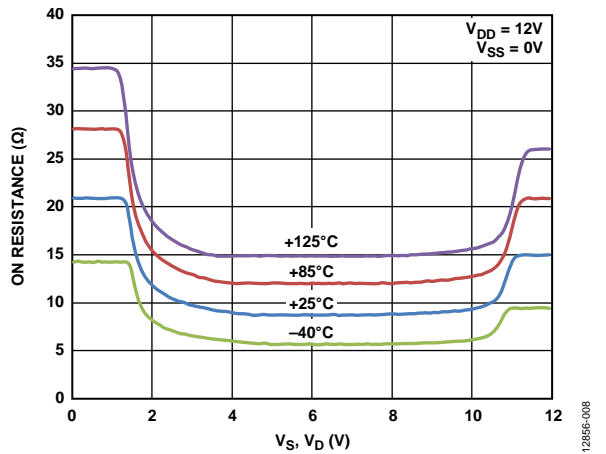


Figure 9.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  for Different Temperatures, 12 V Single Supply



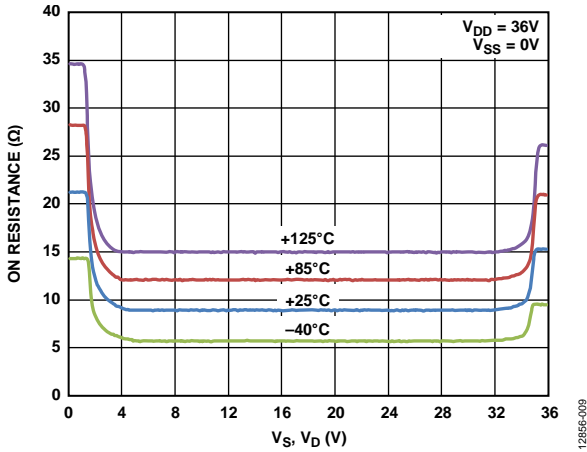


Figure 10.  $R_{ON}$  as a Function of  $V_S$  and  $V_D$  for Different Temperatures, 36 V Single Supply

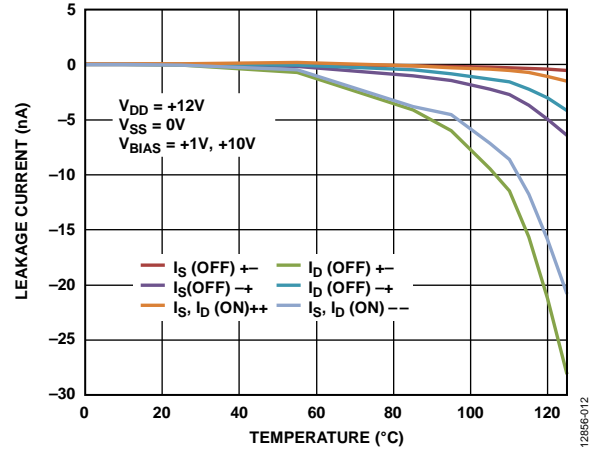


Figure 13. Leakage Current vs. Temperature, 12 V Single Supply

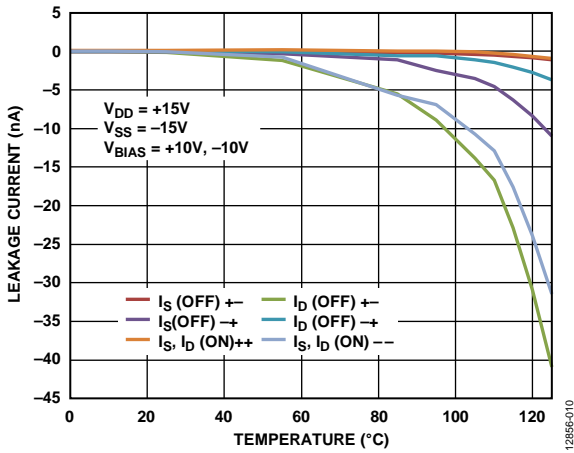


Figure 11. Leakage Current vs. Temperature, ±15 V Dual Supply

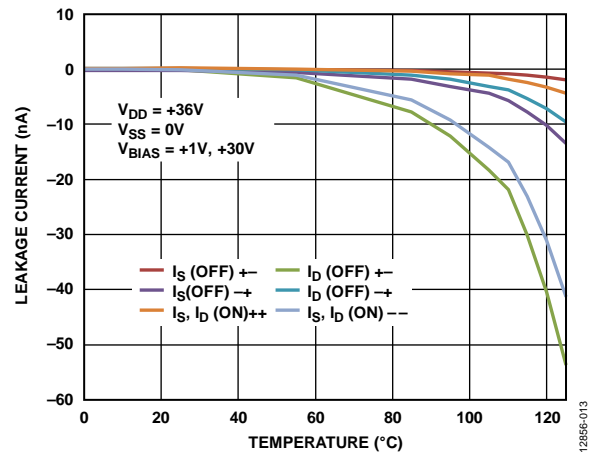


Figure 14. Leakage Current vs. Temperature, 36 V Single Supply

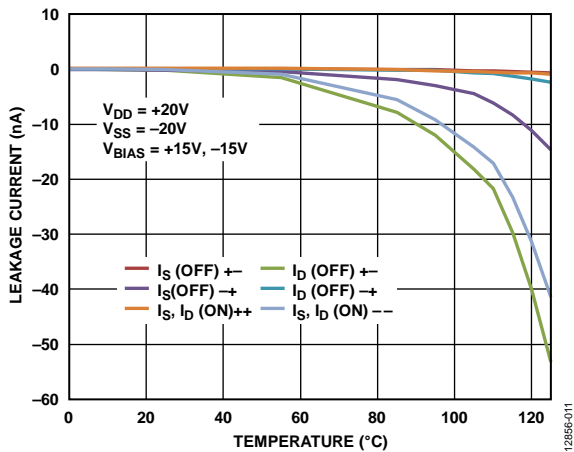


Figure 12. Leakage Current vs. Temperature, ±20 V Dual Supply

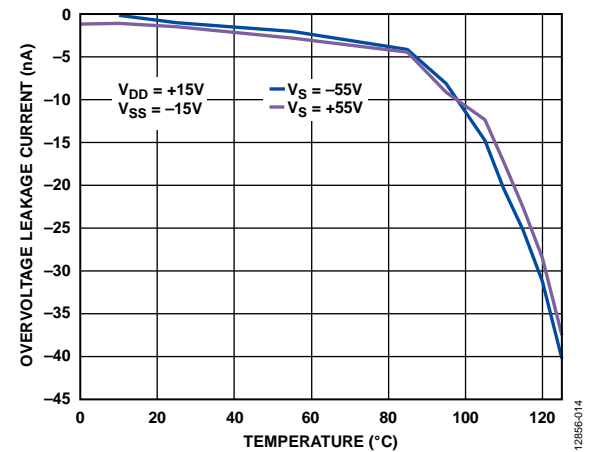


Figure 15. Overvoltage Leakage Current vs. Temperature, ±15 V Dual Supply

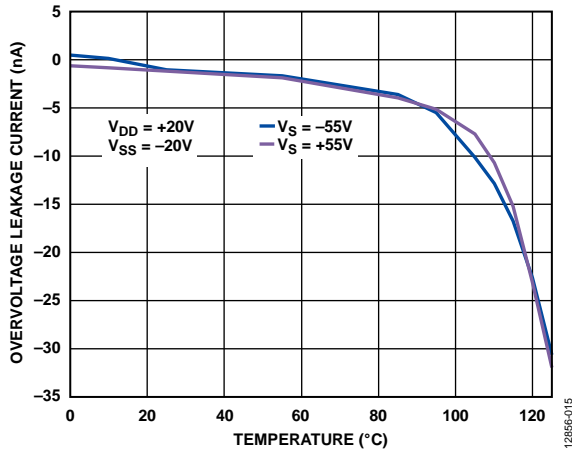


Figure 16. Overvoltage Leakage Current vs. Temperature, ±20 V Dual Supply

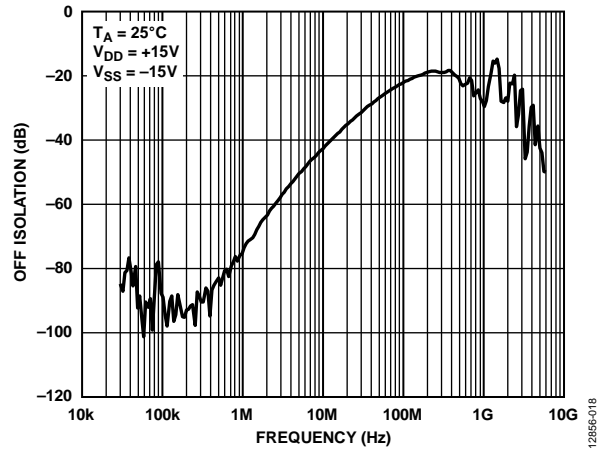


Figure 19. Off Isolation vs. Frequency

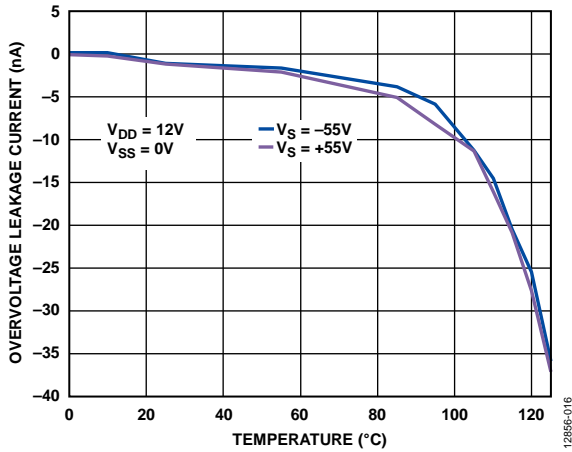


Figure 17. Overvoltage Leakage Current vs. Temperature, 12 V Single Supply

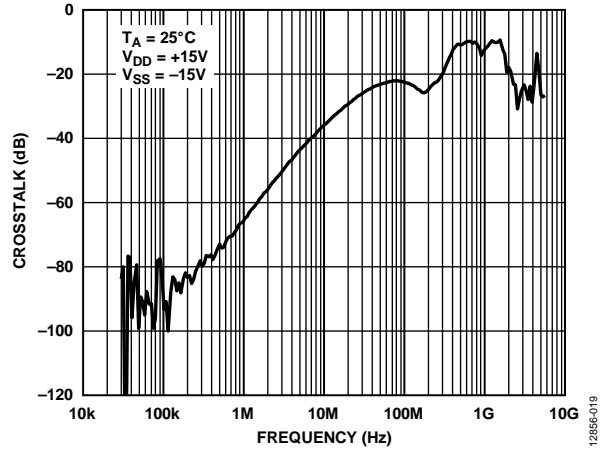


Figure 20. Crosstalk vs. Frequency

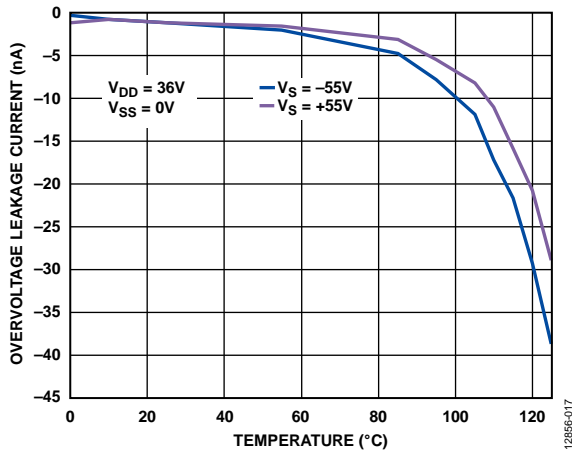


Figure 18. Overvoltage Leakage Current vs. Temperature, 36 V Single Supply

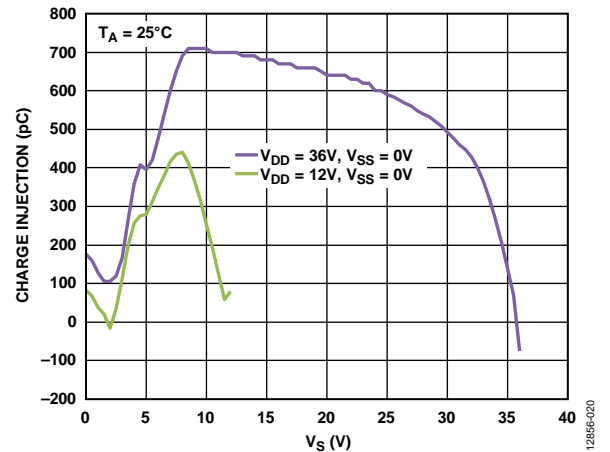


Figure 21. Charge Injection vs. Source Voltage ( $V_S$ ), Single Supply

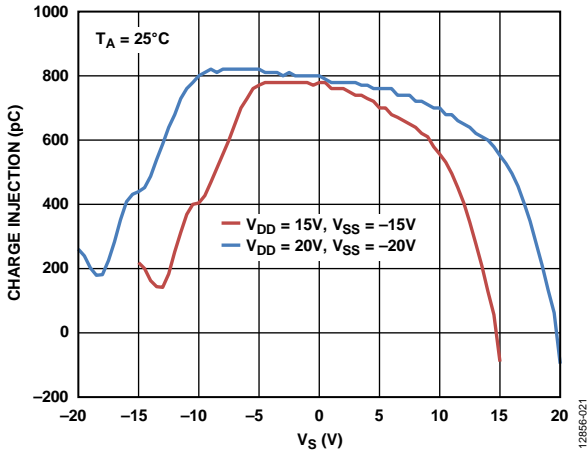


Figure 22. Charge Injection vs. Source Voltage ( $V_S$ ), Dual Supply

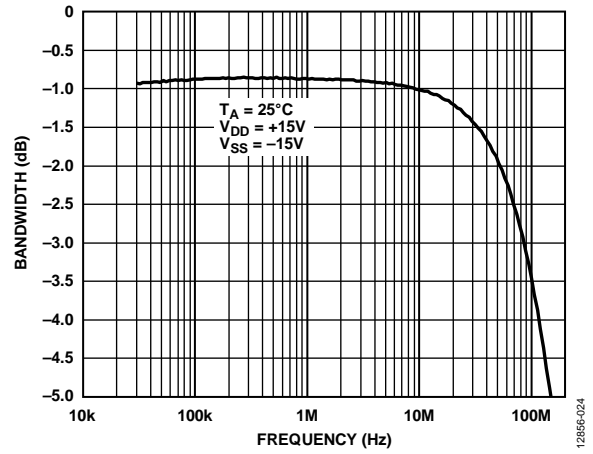


Figure 25. Bandwidth vs. Frequency

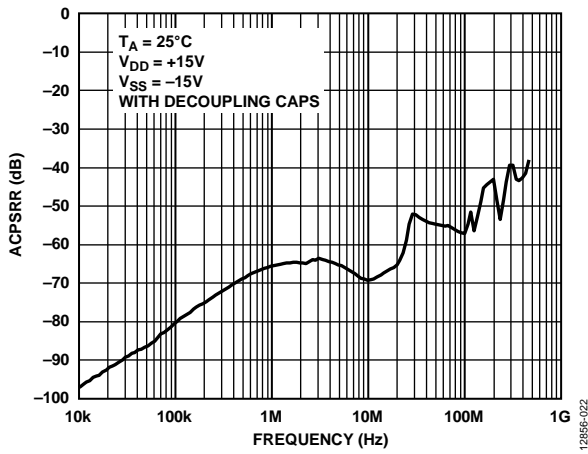


Figure 23. ACPSRR vs. Frequency

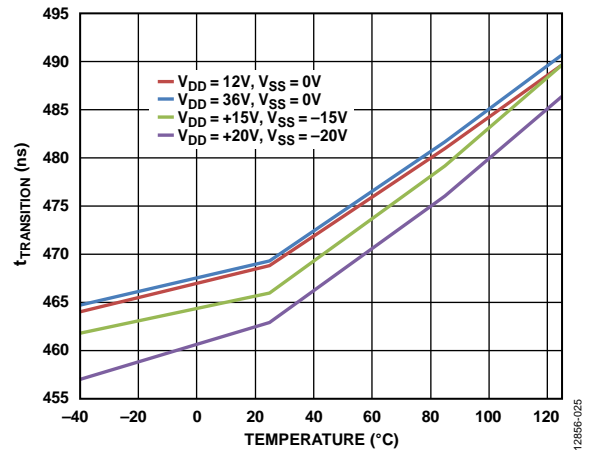


Figure 26.  $t_{TRANSITION}$  vs. Temperature

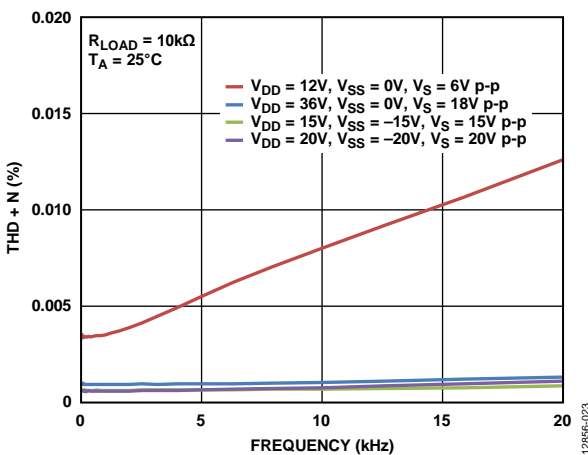


Figure 24. THD + N vs. Frequency

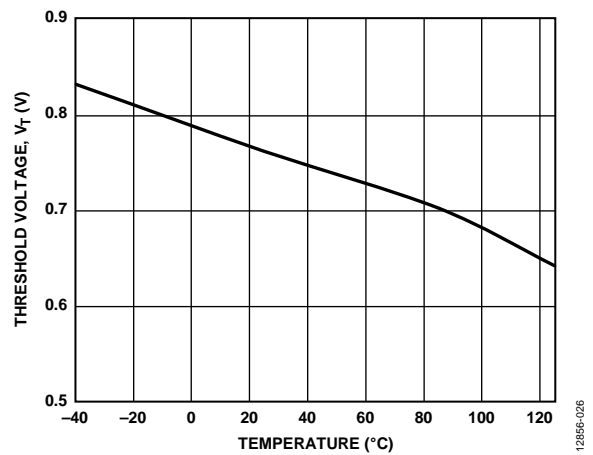


Figure 27. Threshold Voltage ( $V_T$ ) vs. Temperature

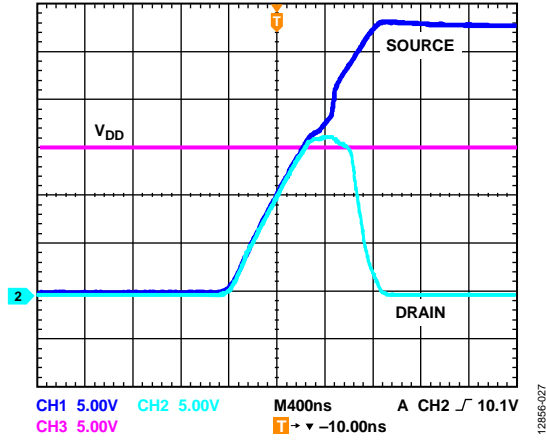


Figure 28. Drain Output Response to Positive Overvoltage

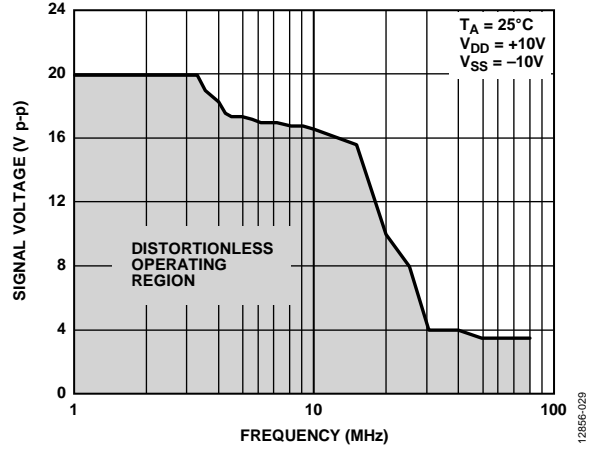


Figure 30. Large Signal Voltage Tracking vs. Frequency

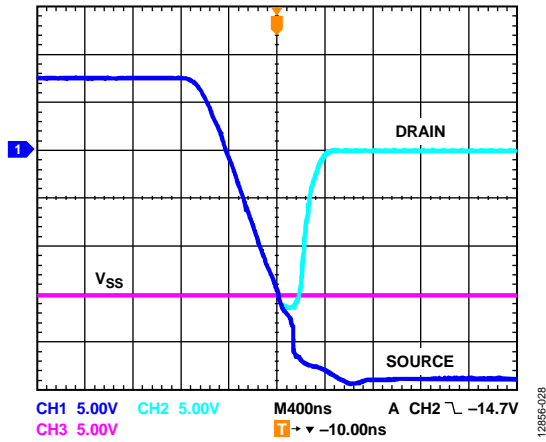


Figure 29. Drain Output Response to Negative Overvoltage

TEST CIRCUITS

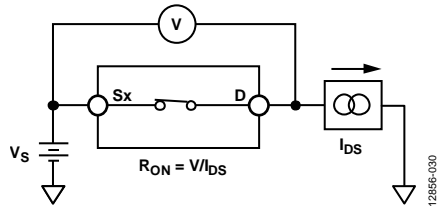


Figure 31. On Resistance

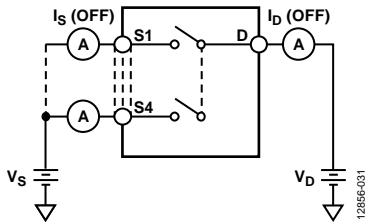


Figure 32. Off Leakage

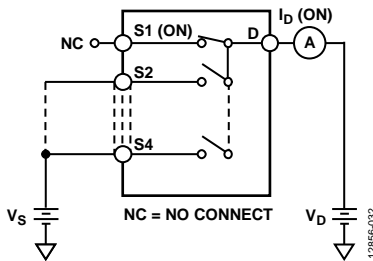


Figure 33. Channel On Leakage

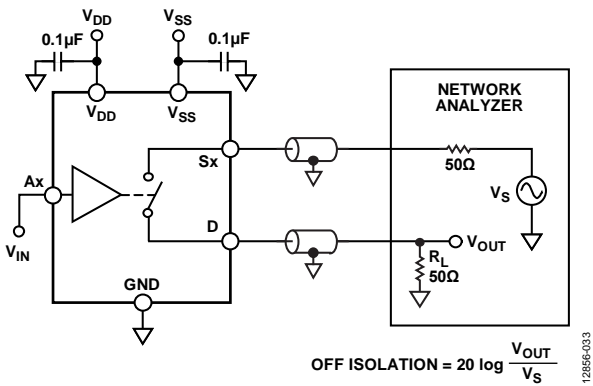


Figure 34. Off Isolation

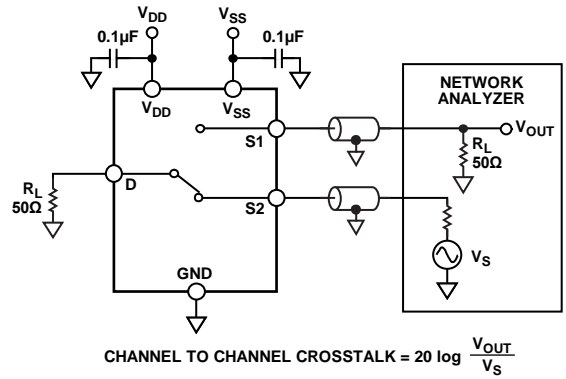


Figure 35. Channel to Channel Crosstalk

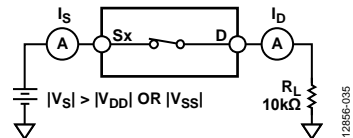


Figure 36. Switch Overvoltage Leakage

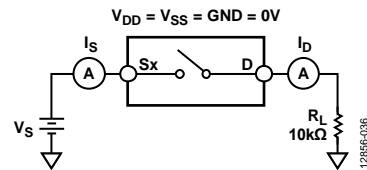


Figure 37. Switch Unpowered Leakage

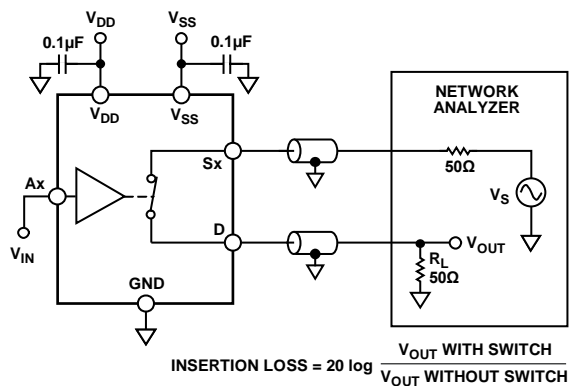


Figure 38. Bandwidth

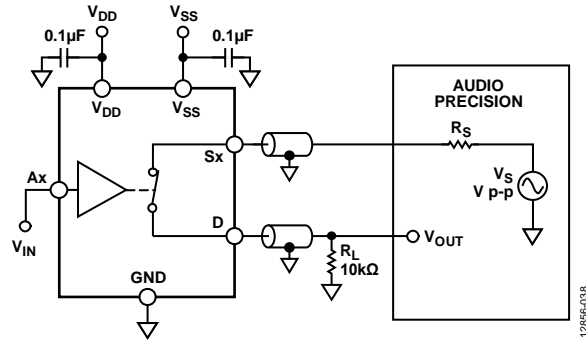
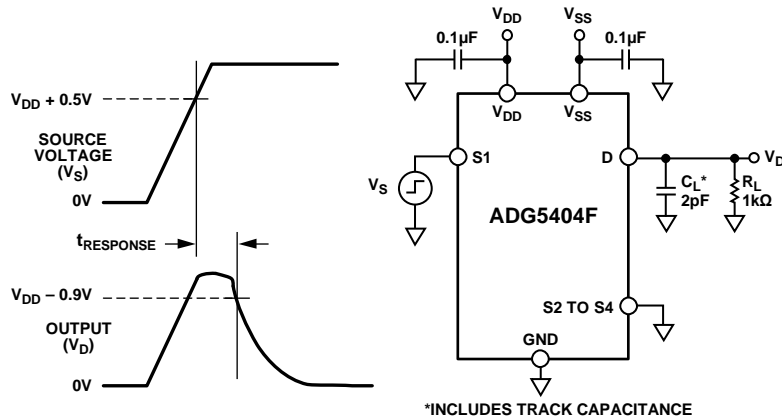
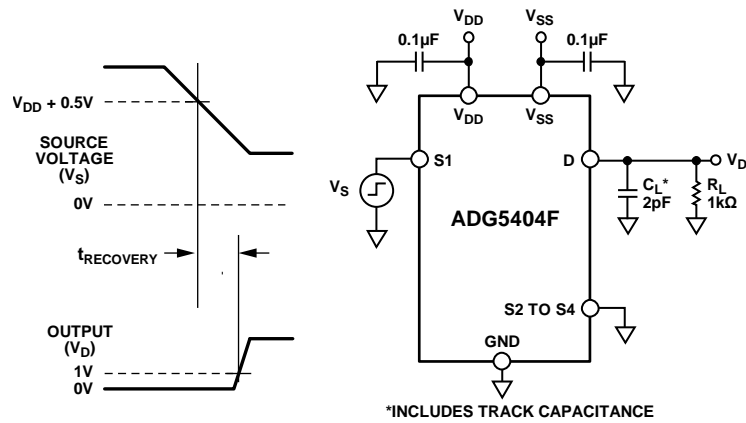


Figure 39. THD + N



\*INCLUDES TRACK CAPACITANCE  
Figure 40. Overtolerance Response Time,  $t_{RESPONSE}$



\*INCLUDES TRACK CAPACITANCE  
Figure 41. Overtolerance Recovery Time,  $t_{RECOVERY}$

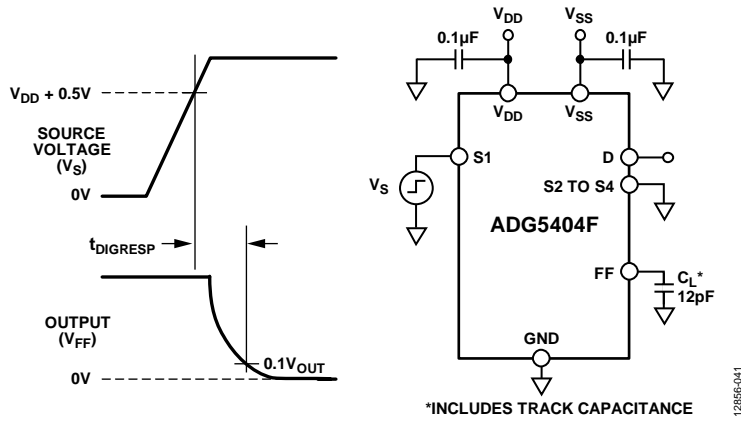


Figure 42. Interrupt Flag Response Time,  $t_{DIGRESP}$

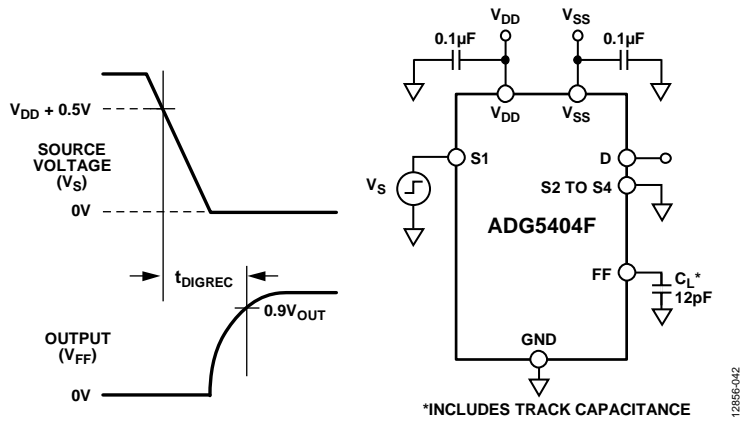


Figure 43. Interrupt Flag Recovery Time,  $t_{DIGREC}$

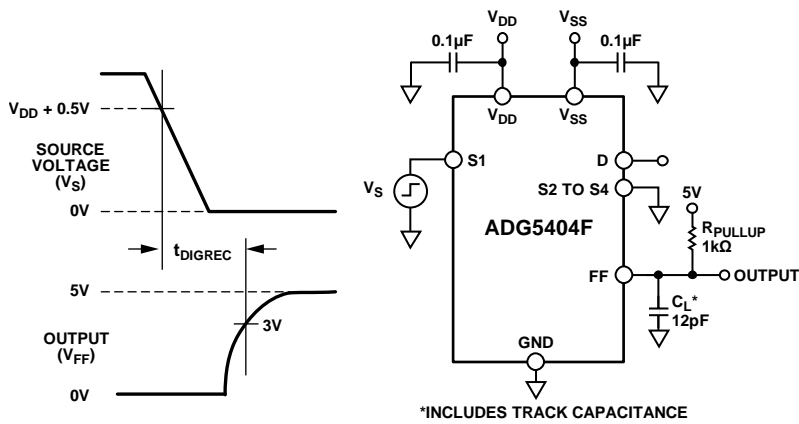


Figure 44. Interrupt Flag Recovery Time,  $t_{DIGREC}$ , with a 1 kΩ Pull-Up Resistor

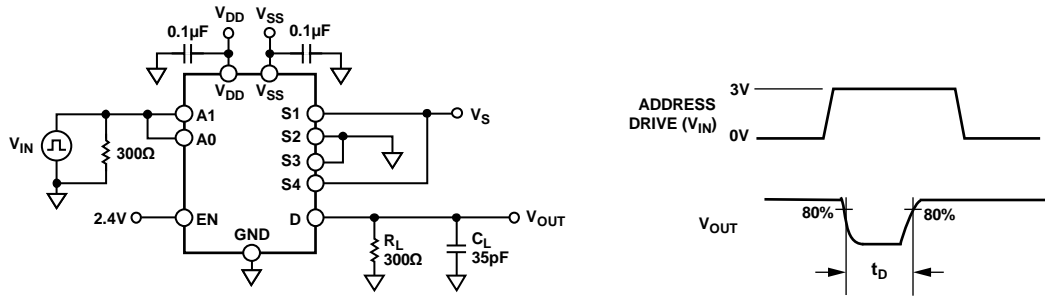


Figure 45. Break-Before-Make Time Delay,  $t_D$

12856-044

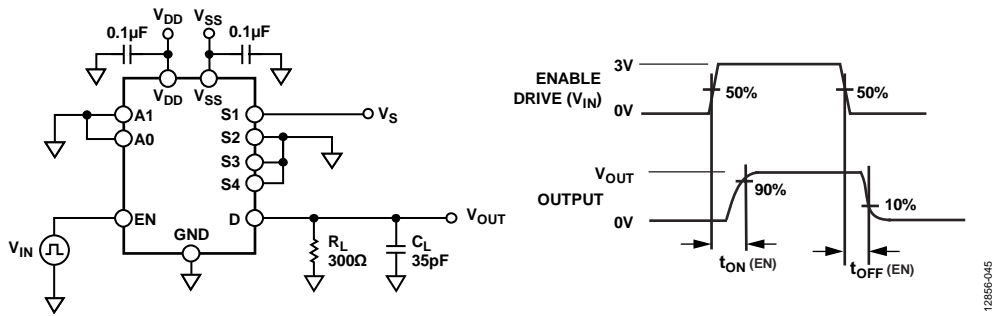


Figure 46. Enable Delay,  $t_{ON}(EN)$ ,  $t_{OFF}(EN)$

12856-045

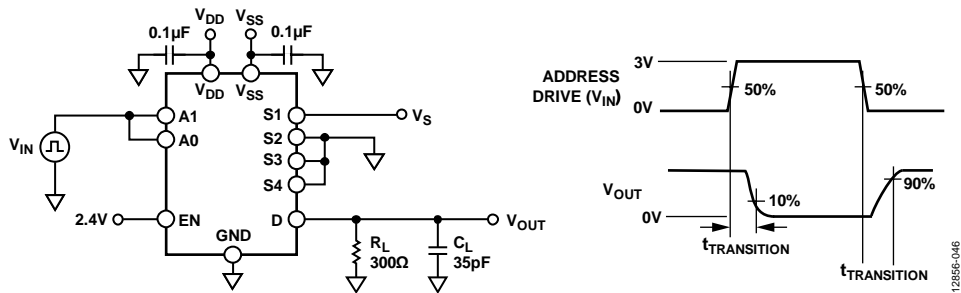


Figure 47. Address to Output Switching Times,  $t_{TRANSITION}$

12856-046

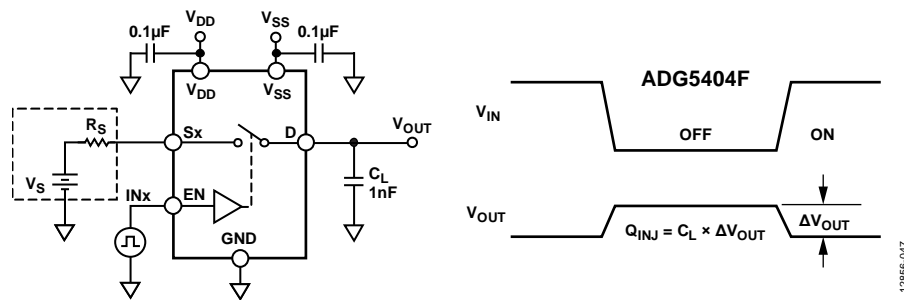


Figure 48. Charge Injection,  $Q_{INJ}$

12856-047



## TERMINOLOGY

### $I_{DD}$

$I_{DD}$  represents the positive supply current.

### $I_{SS}$

$I_{SS}$  represents the negative supply current.

### $V_D, V_S$

$V_D$  and  $V_S$  represent the analog voltage on the D pin and the Sx pins, respectively.

### $R_{ON}$

$R_{ON}$  represents the ohmic resistance between the D pin and the Sx pins.

### $\Delta R_{ON}$

$\Delta R_{ON}$  represents the difference between the  $R_{ON}$  of any two channels.

### $R_{FLAT(ON)}$

$R_{FLAT(ON)}$  is the flatness defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

### $I_S$ (Off)

$I_S$  (Off) is the source leakage current with the switch off.

### $I_D$ (Off)

$I_D$  (Off) is the drain leakage current with the switch off.

### $I_D$ (On), $I_S$ (On)

$I_D$  (On) and  $I_S$  (On) represent the channel leakage currents with the switch on.

### $V_{INL}$

$V_{INL}$  is the maximum input voltage for Logic 0.

### $V_{INH}$

$V_{INH}$  is the minimum input voltage for Logic 1.

### $I_{INL}, I_{INH}$

$I_{INL}$  and  $I_{INH}$  represent the low and high input currents of the digital inputs.

### $C_D$ (Off)

$C_D$  (Off) represents the off switch drain capacitance, which is measured with reference to ground.

### $C_S$ (Off)

$C_S$  (Off) represents the off switch source capacitance, which is measured with reference to ground.

### $C_D$ (On), $C_S$ (On)

$C_D$  (On) and  $C_S$  (On) represent on switch capacitances, which are measured with reference to ground.

### $C_{IN}$

$C_{IN}$  is the digital input capacitance.

### $t_{ON}$

$t_{ON}$  represents the delay between applying the digital control input and the output switching on (see Figure 46).

### $t_{OFF}$

$t_{OFF}$  represents the delay between applying the digital control input and the output switching off (see Figure 46).

### $t_D$

$t_D$  represents the off time measured between the 90% point of both switches when switching from one address state to another.

### $t_{DIGRESP}$

$t_{DIGRESP}$  is the time required for the FF pin to go low (0.3 V), measured with respect to the voltage on the source pin exceeding the supply voltage by 0.5 V.

### $t_{DIGREC}$

$t_{DIGREC}$  is the time required for the FF pin to return high, measured with respect to the voltage on the Sx pin falling below the supply voltage plus 0.5 V.

### $t_{RESPONSE}$

$t_{RESPONSE}$  represents the delay between the source voltage exceeding the supply voltage by 0.5 V and the drain voltage falling to 90% of the supply voltage.

### $t_{RECOVERY}$

$t_{RECOVERY}$  represents the delay between an overvoltage on the Sx pin falling below the supply voltage plus 0.5 V and the drain voltage rising from 0 V to 10% of the supply voltage.

### Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

### Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

### Channel to Channel Crosstalk

Channel to channel crosstalk is a measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.

### –3 dB Bandwidth

–3 dB bandwidth is the frequency at which the output is attenuated by –3 dB.

### On Response

On response is the frequency response of the on switch.

### Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

### Total Harmonic Distortion Plus Noise (THD + N)

THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

**AC Power Supply Rejection Ratio (ACPSRR)**

ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. ACPSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

 **$V_T$** 

$V_T$  is the voltage threshold at which the overvoltage protection circuitry engages (see Figure 27).

## THEORY OF OPERATION

### SWITCH ARCHITECTURE

Each channel of the [ADG5404F](#) consists of a parallel pair of NDMOS and PDMOS transistors. This construction provides excellent performance across the signal range. The [ADG5404F](#) channels operate as standard switches when input signals with a voltage between  $V_{SS}$  and  $V_{DD}$  are applied. For example, the on resistance is  $10\ \Omega$  typically, and opening or closing the switch is controlled using the appropriate control pins.

Additional internal circuitry enables the switch to detect overvoltage inputs by comparing the voltage on the source pin with  $V_{DD}$  and  $V_{SS}$ . A signal is considered overvoltage if it exceeds the supply voltages by the voltage threshold,  $V_T$ . The threshold voltage is typically 0.7 V, but can range from 0.8 V at  $-40^\circ\text{C}$  down to 0.6 V at  $+125^\circ\text{C}$ . See Figure 27 to see the change in  $V_T$  with operating temperature.

The maximum voltage that can be applied to any source input is  $-55\ \text{V}$  or  $+55\ \text{V}$ . When the device is powered using the single supply of 25 V or greater, the maximum signal level is reduced. It reduces from  $-55\ \text{V}$  at  $V_{DD} = +25\ \text{V}$  to  $-40\ \text{V}$  at  $V_{DD} = +40\ \text{V}$  to remain within the 80 V maximum rating. The construction of the process allows the channel to withstand 80 V across the switch when it is opened. These overvoltage limits apply whether the power supplies are present or not.

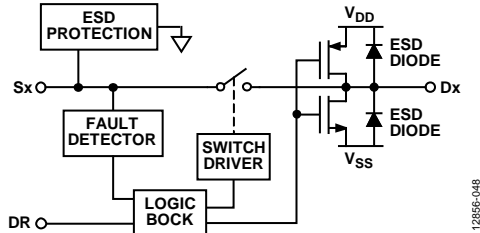


Figure 49. Switch Channel and Control Function

When an overvoltage condition is detected on a source pin ( $S_x$ ), the switch automatically opens and the source pin ( $S_x$ ) becomes high impedance and ensures that no current flows through the switch. If the DR pin is driven low, the drain pin, D, is pulled to the supply that was exceeded. For example, if the source voltage exceeds  $V_{DD}$ , the drain output pulls to  $V_{DD}$ . The same is true for  $V_{SS}$ . If the DR pin is allowed to float or is driven high, Pin D also becomes open circuit. The voltage on Pin D follows the voltage on the source pin,  $S_x$ , until the switch turns off completely and the drain voltage discharges through the load. The maximum voltage on the drain is limited by the internal ESD diodes and the rate at which the output voltage discharges is dependent on the load at the pin.

During overvoltage conditions, the leakage current into and out of the source pins ( $S_x$ ) is limited to tens of microamperes. If the DR pin is allowed to float or is driven high, only nanoamperes of leakage are seen on the drain pin (D). If the DR pin is driven low, the drain pin (D) is pulled to the rail. The device that pulls the drain pin to the rail has an impedance of approximately  $40\ \text{k}\Omega$ , so the  $D_x$  pin current will be limited to about 1 mA during a shorted load condition. This internal impedance will also determine the minimum external load resistance required to ensure the drain pin is pulled to the desired voltage level during a fault.

When an overvoltage event occurs, the channels undisturbed by the overvoltage input continue to operate normally without additional crosstalk.

### ESD Performance

The [ADG5404F](#) has an ESD (HBM) rating of 4 kV.

The drain pin has ESD protection diodes to the rails, and the voltage at this pin must not exceed supply voltage. The source pins have specialized ESD protection that allow the signal voltage to reach from  $-55\ \text{V}$  to  $+55\ \text{V}$  with a  $\pm 22\ \text{V}$  dual supply, and from  $-40\ \text{V}$  to  $+55\ \text{V}$  with a 40 V single supply. See Figure 49 for the switch channel overview.

### Trench Isolation

In the [ADG5404F](#), an insulating oxide layer (trench) is placed between the NDMOS and the PDMOS transistors of each switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a switch that is latch-up immune under all circumstances. This device passes a JESD78D latch-up test of  $\pm 500\ \text{mA}$  for 1 sec, the strictest test in the specification.

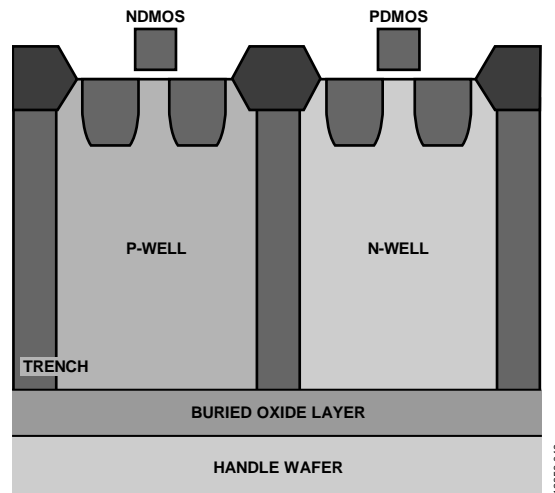


Figure 50. Trench Isolation

## FAULT PROTECTION

When the voltages at the source inputs exceed  $V_{DD}$  or  $V_{SS}$  by  $V_T$ , the switch turns off, or, if the device is unpowered, the switch remains off. The switch input remains high impedance regardless of the digital input state or the load resistance, and the output acts as a virtual open circuit. Signal levels up to +55 V and -55 V are blocked in both the powered and unpowered conditions as long as the 80 V limitation between the source and supply pins is met.

### Power-On Protection

The following three conditions must be satisfied for the switch to be in the on condition:

- $V_{DD}$  to  $V_{SS} \geq 8$  V.
- Input signal is between  $V_{SS} - V_T$  and  $V_{DD} + V_T$ .
- The digital logic control input, Ax, is turned on.

When the switch is turned on, the signal levels up to the supply rails are passed.

The switch responds to an analog input that exceeds  $V_{DD}$  or  $V_{SS}$  by a threshold voltage,  $V_T$ , by turning off. The absolute input voltage limits are -55 V and +55 V, while maintaining an 80 V limit between the source pin and the supply rails. The switch remains off until the voltage at the source pin returns to between  $V_{DD}$  and  $V_{SS}$ .

The fault response time ( $t_{RESPONSE}$ ) when powered by a  $\pm 15$  V dual supply is typically 600 ns, and the fault recovery time ( $t_{RECOVERY}$ ) is 700 ns. These vary with supply voltages and output load conditions.

Exceeding  $\pm 55$  V on any source input may damage the ESD protection circuitry on the device.

The maximum stress across the switch channel is 80 V.

Therefore, the user must pay close attention to this limit when using the device with a 40 V single supply. In this case, the maximum undervoltage condition is -40 V to maintain the 80 V across the switch channel.

For undervoltage and overvoltage conditions, consider the case where the device is set up as shown in Figure 51.

- $V_{DD}/V_{SS} = \pm 22$  V,  $S_4 = 22$  V, and  $S_4$  is on. Therefore,  $D = 22$  V
- $S_1$  and  $S_2$  have a -55 V fault and  $S_3$  has a +55 V fault.
- The voltage between  $S_1$  and  $D$  or between  $S_2$  and  $D = +22$  V - (-55 V) = +77 V.
- The voltage between  $S_3$  and  $D = 22$  V - 55 V = -33 V.

These calculations are all within the device specifications: a 55 V maximum fault on source inputs and a maximum of 80 V across the off switch channel.

FF is low due to the fault condition on  $S_1$ ,  $S_2$ , and  $S_3$ . SF is high because there is no fault condition on  $S_4$  as decoded by  $F_1 = 1$ ,  $F_0 = 1$ .

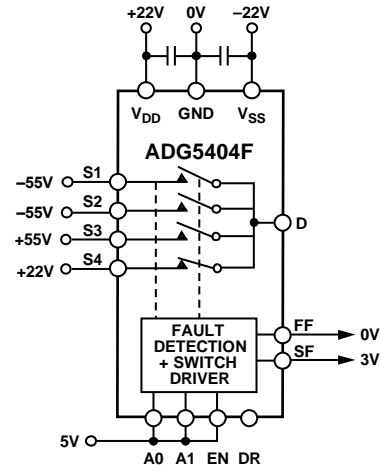


Figure 51. Example Fault Condition Setup

### Power-Off Protection

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance. This state ensures that no current flows and prevents damage to the switch or downstream circuitry. The switch output is a virtual open circuit.

The switch remains off regardless of whether the  $V_{DD}$  and  $V_{SS}$  supplies are 0 V or floating. A GND reference must always be present to ensure proper operation. Signal levels of up to  $\pm 55$  V are blocked in the unpowered condition.

### Digital Input Protection

The ADG5404F can tolerate unpowered digital input signals present on the device. When the device is unpowered, the switch is guaranteed to be in the off state, regardless of the state of the digital logic signals.

The digital inputs are protected against positive faults up to 44 V. The digital inputs do not offer protection against negative overvoltages. ESD protection diodes connected to GND are present on the digital inputs.

### Overvoltage Interrupt Flag

The voltages on the source inputs of the ADG5404F are continuously monitored, and the state of the switch is indicated by an active low digital output pin, FF.

The voltage on the FF pin indicates if any of the source input pins are experiencing a fault condition. The output of the FF pin is a nominal 3 V when all source pins are within normal operating range. If any source pin voltage exceeds the supply voltage by  $V_T$ , the FF output reduces to below 0.8 V.

Use the specific fault digital output pin, SF, to decode which inputs are experiencing a fault condition. The SF pin reduces to below 0.8 V when a fault condition is detected on a specific pin, depending on the state of  $F_0$  and  $F_1$  (see Table 9).

The specific fault feature also works with the switches disabled (EN pin low), which allows the user to cycle through and check the fault conditions without connecting the fault to the drain output.

## APPLICATIONS INFORMATION

The overvoltage protected family of switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments where overvoltage signals can be present and the system must remain operational both during and after the overvoltage has occurred.

### POWER SUPPLY RAILS

To guarantee correct operation of the device, 0.1  $\mu\text{F}$  decoupling capacitors are required on the supply rails..

The ADG5404F can operate with bipolar supplies between  $\pm 5\text{ V}$  and  $\pm 22\text{ V}$ . The supplies on  $V_{\text{DD}}$  and  $V_{\text{SS}}$  do not need to be symmetrical, but the  $V_{\text{DD}}$  to  $V_{\text{SS}}$  range must not exceed 44 V. The ADG5404F can also operate with single supplies between 8 V and 44 V, with  $V_{\text{SS}}$  connected to GND.

The ADG5404F is fully specified at the  $\pm 15\text{ V}$ ,  $\pm 20\text{ V}$ , 12 V, and 36 V supply ranges.

### POWER SUPPLY SEQUENCING PROTECTION

The switch channel remains open when the device is unpowered, and signals from  $-55\text{ V}$  to  $+55\text{ V}$  can be applied without damaging the device. Only when the supplies are connected, a suitable digital control signal is placed on the Ax pins, and the signal is within normal operating range does the switch channel close. Placing the ADG5404F between external connectors and sensitive components offers protection in systems where a signal is presented to the source pins before the supply voltages are available.

### SIGNAL RANGE

The ADG5404F has overvoltage detection circuitry on the inputs that compares the voltage levels at the source terminals with  $V_{\text{DD}}$  and  $V_{\text{SS}}$ . To protect downstream circuitry from overvoltage conditions, supply the ADG5404F with voltages that match the intended signal range. The low on-resistance switch allows signals up to the supply rails to be passed with very little distortion. A signal that exceeds the supply rail by the threshold voltage is then blocked. This signal block offers protection to both the device and any downstream circuitry.

### LOW IMPEDANCE CHANNEL PROTECTION

The ADG5404F can be used as a protective element in signal chains that are sensitive to both channel impedance and overvoltage signals. Traditionally, series resistors limit the current during an overvoltage condition to protect susceptible components.

These series resistors affect the performance of the signal chain and reduce the signal chain precision. A compromise must be reached on the value of the series resistance that is high enough to sufficiently protect sensitive components, but low enough that the precision performance of the signal chain is not sacrificed.

The ADG5404F enables the designer to remove these resistors and retain precision performance without compromising the protection of the circuit.

### POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 52. The ADP7118 and ADP7182 can be used to generate clean positive and negative rails from the ADP5070 dual switching regulator output. These rails can be used to power the ADG5404F, the amplifier, and/or the precision converter in a typical signal chain.

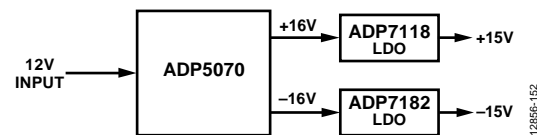


Figure 52. Bipolar Power Solution

Table 10. Recommended Power Management Devices

Product	Description
ADP5070	1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs
ADP7118	20 V, 200 mA, low noise, CMOS LDO
ADP7142	40 V, 200 mA, low noise, CMOS LDO
ADP7182	-28 V, -200 mA, low noise, linear regulator

### HIGH VOLTAGE SURGE SUPPRESSION

The ADG5404F is not intended for use in very high voltage applications. The maximum operating voltage of the transistor is 80 V. In applications where the inputs are likely to be subject to overvoltage conditions exceeding the breakdown voltage, use transient voltage suppressors (TVSs) or similar devices.

### INTELLIGENT FAULT DETECTION

The ADG5404F digital output pin, FF, can interface with a microprocessor or control system and can be used as an interrupt flag. This feature provides real-time diagnostic information on the state of the device and the system to which it connects.

The control system can use the digital interrupt, FF, to start a variety of actions, as follows:

- Initiating an investigation into the source of an overvoltage fault.
- Shutting down critical systems in response to the overvoltage condition.
- Using data recorders to mark data during these events as unreliable or out of specification.

For systems sensitive during a start-up sequence, the active low operation of the flag allows the system to ensure that the [ADG5404F](#) is powered on and that all input voltages are within the normal operating range before initiating operation.

The FF pin is a weak pull-up, which allows the signals to combine into a single interrupt for larger modules that contain multiple devices.

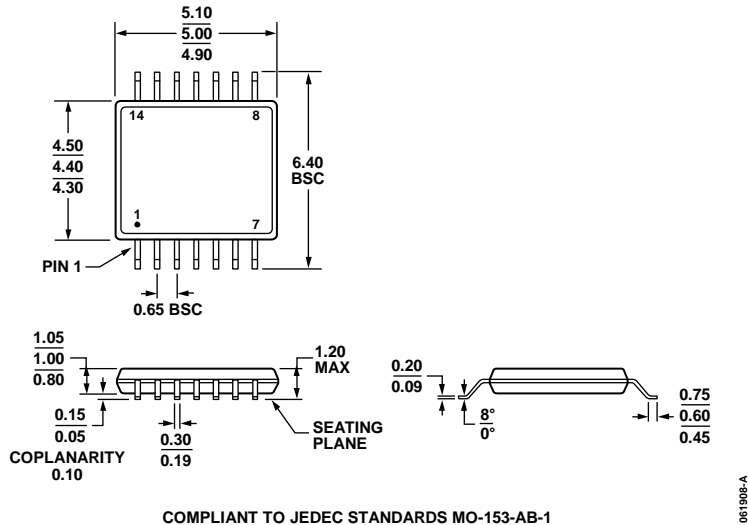
The recovery time,  $t_{DIGREC}$ , can be decreased from a typical 60  $\mu$ s to 600 ns by using a 1 k $\Omega$  pull-up resistor.

The specific fault digital output, SF can be used to decode which inputs are experiencing a fault condition. The SF pin reduces to below 0.8 V when a fault condition is detected on a specific pin, depending on the state of F0 and F1 (see Table 9).

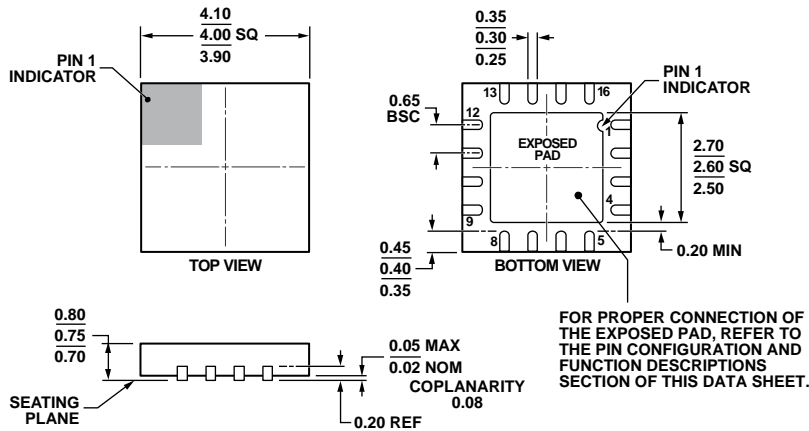
### **LARGE VOLTAGE, HIGH FREQUENCY SIGNALS**

Figure 30 shows the voltage range and frequencies that the [ADG5404F](#) can reliably convey. For signals extending across the full signal range from  $V_{SS}$  to  $V_{DD}$ , keep the frequency below 3 MHz. If the required frequency is greater than 3 MHz, decrease the signal range appropriately to ensure signal integrity.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1  
 Figure 53. 14-Lead Thin Shrink Small Outline Package [TSSOP]  
 (RU-14)  
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.  
 Figure 54. 16-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
 4 mm × 4 mm Body, Very Very Thin Quad  
 (CP-16-17)  
 Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG5404FBRUZ	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG5404FBRUZ-RL7	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG5404FBCPZ-RL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17

<sup>1</sup> Z = RoHS Compliant Part.