# 3.3 VOLT TIME SLOT INTERCHANGE DIGITAL SWITCH 128 x 128

## IDT72V8981

## FEATURES:

- 128 x 128 channel non-blocking switch
- Serial Telecom Bus Compatible (ST-BUS®)
- 4 RX inputs—32 channels at 64 Kbit/s per serial line
- 4 TX output—32 channels at 64 Kbit/s per serial line
- Three-state serial outputs
- Microprocessor Interface (8-bit data bus)
- 3.3V Power Supply
- Available in 44-pin Plastic Leaded Chip Carrier (PLCC), and 44-pin Plastic Quad Flatpack (PQFP)
- Operating Temperature Range  -40°C to +85°C
- 3.3V I/O with 5V Tolerant Inputs

## DESCRIPTION:

The IDT72V8981 is a ST-BUS® compatible digital switch controlled by a microprocessor. The IDT72V8981 can handle as many as 128, 64 Kbit/s input and output channels. Those 128 channels are divided into 4 serial inputs and outputs, each of which consists of 32 channels (64 Kbit/s per channel) to form a multiplexed 2.048 Mb/s stream.
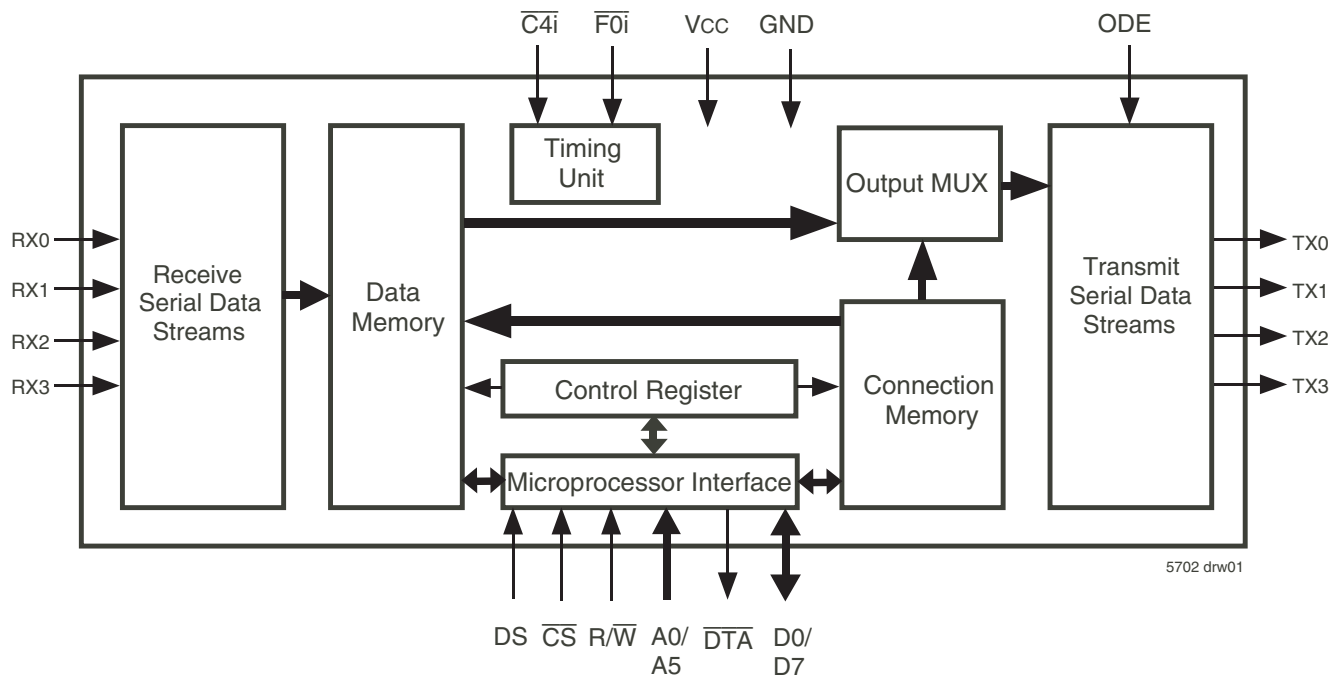
## FUNCTIONAL DESCRIPTION

A functional block diagram of the IDT72V8981 device is shown below. The serial streams operate continuously at 2.048 Mb/s and are arranged in 125 µs wide frames each containing 32, 8-bit channels. Four input (RX0-3) and four output (TX0-3) serial streams are provided in the IDT72V8981 device allowing a complete 128 x 128 channel non-blocking switch matrix to be constructed. The serial interface clock ($\overline{C4i}$) for the device is 4.096 MHz.
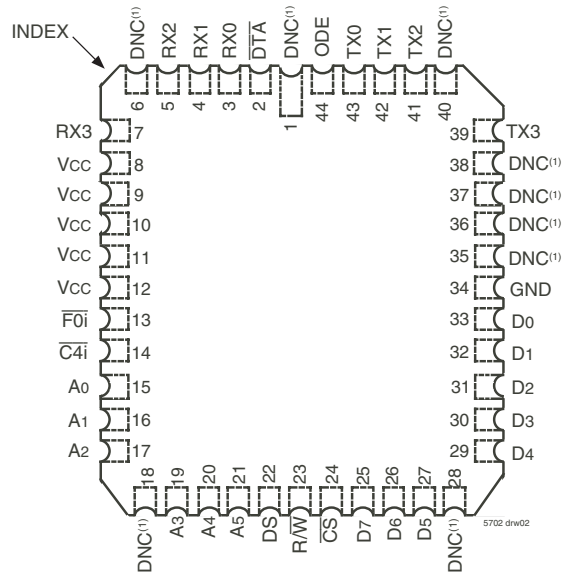
The received serial data is internally converted to a parallel format by the on chip serial-to-parallel converters and stored sequentially in a 128-position Data Memory. By using an internal counter that is reset by the input 8 KHz frame pulse, $\overline{F0i}$, the incoming serial data streams can be framed and sequentially addressed.

Data to be output on the serial streams may come from two sources: Data Memory or Connection Memory. The Connection Memory is 16 bits wide and
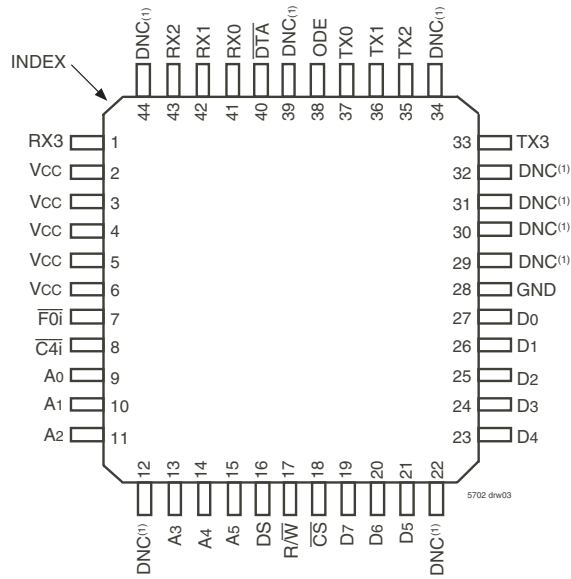
## FUNCTIONAL BLOCK DIAGRAM



5702 drw01

**AUGUST 2003**

DSC-5702/4

# PIN CONFIGURATION

INDEX →

Pins (top, left to right): DNC[1] (6), RX2 (5), RX1 (4), RX0 (3), DTA (2), DNC[1] (1), ODE (44), TX0 (43), TX1 (42), TX2 (41), DNC[1] (40)

Left side (top to bottom): RX3 (7), Vcc (8), Vcc (9), Vcc (10), Vcc (11), Vcc (12), F0i (13), C4i (14), A0 (15), A1 (16), A2 (17)

Right side (top to bottom): TX3 (39), DNC[1] (38), DNC[1] (37), DNC[1] (36), DNC[1] (35), GND (34), D0 (33), D1 (32), D2 (31), D3 (30), D4 (29)

Bottom (left to right): DNC[1] (18), A3 (19), A4 (20), A5 (21), DS (22), R/W (23), CS (24), D7 (25), D6 (26), D5 (27), DNC[1] (28)

5702 drw02

**PLCC: 0.05in. pitch, 0.65in. x 0.65in.**
**(J44-1, order code: J)**
**TOP VIEW**

INDEX →

Pins (top, left to right): DNC[1] (44), RX2 (43), RX1 (42), RX0 (41), DTA (40), DNC[1] (39), ODE (38), TX0 (37), TX1 (36), TX2 (35), DNC[1] (34)

Left side (top to bottom): RX3 (1), Vcc (2), Vcc (3), Vcc (4), Vcc (5), Vcc (6), F0i (7), C4i (8), A0 (9), A1 (10), A2 (11)

Right side (top to bottom): TX3 (33), DNC[1] (32), DNC[1] (31), DNC[1] (30), DNC[1] (29), GND (28), D0 (27), D1 (26), D2 (25), D3 (24), D4 (23)

Bottom (left to right): DNC[1] (12), A3 (13), A4 (14), A5 (15), DS (16), R/W (17), CS (18), D7 (19), D6 (20), D5 (21), DNC[1] (22)

5702 drw03

**PQFP: 0.80mm pitch, 10mm x 10mm**
**(DB44-1, order code: DB)**
**TOP VIEW**

NOTE:
1. DNC - Do Not Connect

## PIN DESCRIPTIONS

| SYMBOL | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| GND | Ground. | | Ground Rail. |
| Vcc | Vcc | | +3.3 Volt Power Supply. |
| $\overline{DTA}$ | Data Acknowledgment (Open Drain) | O | This active LOW output indicates that a data bus transfer is complete. A pull-up resistor is required at this output. |
| RX0-3 | RX Input 0 to 3 | I | Serial data input streams. These streams have 32 channels at data rates of 2.048 Mb/s. |
| $\overline{F0i}$ | Frame Pulse | I | This input identifies frame synchronization signals formatted to ST-BUS® specifications. |
| $\overline{C4i}$ | Clock | I | 4.096 MHz serial clock for shifting data in and out of the data streams. |
| A0-A5 | Address 0 to 5 | I | These lines provide the address to IDT72V8981 internal registers. |
| DS | Data Strobe | I | This is the input for the active HIGH data strobe on the microprocessor interface. This input operates with $\overline{CS}$ to enable the internal read and write generation. |
| R/$\overline{W}$ | Read/Write | I | This input controls the direction of the data bus lines (D0-D7) during a microprocessor access. |
| $\overline{CS}$ | Chip Select | I | Active LOW input enabling a microprocessor read or write of control register or internal memories. |
| D0-D7 | Data Bus 0 to 7 | I/O | These pins provide microprocessor access to data in the internal control register. Connection Memory HIGH, Connection Memory LOW and data memory. |
| TX0-3 | TX Outputs 0 to 3 (Three-state Outputs) | O | Serial data output streams. These streams are composed of 32, 64 Kbit/s channels at data rates of 2.048 Mb/s. |
| ODE | Output Drive Enable | I | This is an output enable for the TX0-3 serial outputs. If this input is LOW, TX0-3 are high-impedance. If this is HIGH, each channel may still be put into high-impedance by software control. |

# FUNCTIONAL DESCRIPTION (Cont'd)

is split into two 8-bit blocks—Connection Memory HIGH and Connection Memory LOW. Each location in Connection Memory is associated with a particular channel in an output stream so as to provide a one-to-one correspondence between Connection and Data Memories. This correspondence allows for per channel control for each TX output stream.

In Processor Mode, data output on the TX is taken from the Connection Memory Low and originates from the microprocessor (Figure 2). Where as in Connection Mode (Figure 1), data is read from Data Memory using the address in Connection Memory. Data destined for a particular channel on the serial output stream is read during the previous channel time slot to allow time for memory access and internal parallel-to-serial conversion.

## CONNECTION MODE

In Connection Mode, the addresses of input source for all output channels are stored in the Connection Memory Low. The Connection Memory Low locations are mapped to corresponding 8-bit x 32-channel output. The contents of the Data Memory at the selected address are then transferred to the parallel-to-serial converters. By having the output channel to specify the input channel through the Connection Memory, input channels can be broadcast to several output channels.

## PROCESSOR MODE

In Processor Mode the CPU writes data to specific Connection Memory Low locations which are to be output on the TX streams. The contents of the Connection Memory Low are transferred to the parallel-to-serial converter one channel before it is to be output and are transmitted each frame to the output until it is changed by the CPU.

## CONTROL

The Connection Memory High bits (Table 4) control the per-channel functions available in the IDT72V8981. Output channels are selected into specific modes such as: Processor mode or Connection mode and Output Drivers Enabled or in three-state condition.

## OUTPUT DRIVE ENABLE (ODE)

The ODE pin is the master three-state output control pin. If the ODE input is held LOW all TX outputs will be placed in high impedance regardless Connection Memory High programming. However, if ODE is HIGH, the contents of Connection Memory High control the output state on a per-channel basis.

## DELAY THROUGH THE IDT72V8981

The transfer of information from the input serial streams to the output serial streams results in a delay through the device. The delay through the IDT72V8981 device varies according to the combination of input and output streams and the movement within the stream from channel to channel. Data received on an input stream must first be stored in Data Memory before it is sent out.
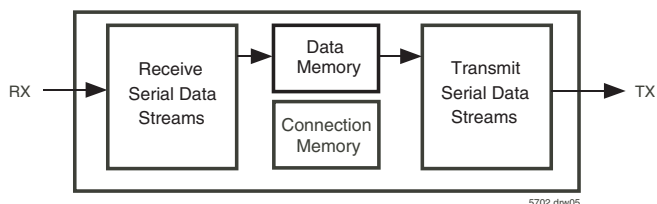
As information enters the IDT72V8981 it must first pass through an internal serial-to-parallel converter. Likewise, before data leaves the device, it must pass through the internal parallel-to-serial converter. This data preparation has an effect on the channel positioning in the frame immediately following the incoming frame—mainly, data cannot leave in the same time slot. Therefore, information that is to be output in the same channel position as the information is input, relative to the frame pulse, will be output in the following frame.

Whether information can be output during a following timeslot after the information entered the IDT72V8981 depends on which RX stream the channel information enters on and which TX stream the information leaves on. This is caused by the order in which input stream information is placed into Data Memory and the order in which stream information is queued for output. Table 1 shows the allowable input/output stream combinations for the minimum two channel delay.

# SOFTWARE CONTROL

If the A5 address line input is LOW then the IDT72V8981 Internal Control Register is addressed. If A5 input line is high, then the remaining address input lines are used to select the 32 possible channels per input or output stream. The address input lines and the Stream Address bits (STA) of the Control register give the user the capability of selecting all positions of IDT72V8981 Data and Connection memories. The IDT72V8981 memory mapping is illustrated in Table 2 and Figure 3.

The data in the control register (Table 3) consists of Memory Select and Stream Address bits, Split Memory and Processor Mode bits. In Split Memory mode (Bit 7 of the Control register) reads are from the Data Memory and writes are to the Connection Memory as specified by the Memory Select Bits (Bits 4 and 3 of the Control Register). The Memory Select bits allow the Connection Memory HIGH or LOW or the Data Memory to be chosen, and the Stream Address bits define internal memory subsections corresponding to input or output streams.

The Processor Enable bit (bit 6) places EVERY output channel on every output stream in Processor mode; i.e., the contents of the Connection Memory LOW (CML, see Table 5) are output on the TX output streams once every frame unless the ODE input pin is LOW. If PE bit is HIGH, then the IDT72V8981 behaves as if bits 2 (Channel Source) and 0 (Output Enable) of every Connection Memory High (CMH) locations were set to HIGH, regardless of the actual value. If PE is LOW, then bit 2 and 0 of each Connection Memory High location operates normally. In this case, if bit 2 of the CMH is HIGH, the associated TX output channel is in Processor Mode. If bit 2 of the CMH is LOW, then the contents of the CML define the source information (stream and channel) of the time slot that is to be switched to an output.

If the ODE input pin is LOW, then all the serial outputs are high-impedance. If ODE is HIGH, then bit 0 (Output Enable) of the CMH location enables (if HIGH) or disables (if LOW) the output stream and channel.
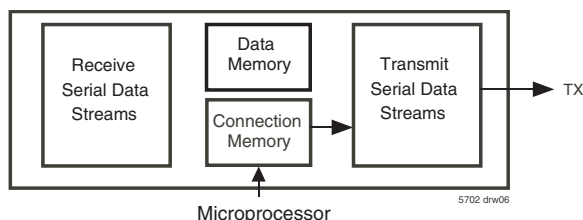


5702 drw05

*Figure 1. Connection Mode*



5702 drw06

Microprocessor

*Figure 2. Processor Mode*

## INITIALIZATION OF THE IDT72V8981

On initialization or power up, the contents of the Connection Memory High can be in any state. This is a potentially hazardous condition when multiple TX outputs are tied together to form matrices. The ODE pin should be held low on power up to keep all outputs in the high impedance condition until the contents of the CMH are programmed.

During the microprocessor initialization routine, the microprocessor should program the desired active paths through the matrices, and put all other channels into the high impedance state. Care should be taken that no two connected TX outputs drive the bus simultaneously. With the CMH setup, the microprocessor controlling the matrices can bring the ODE signal high to relinquish high impedance state control to the Connection Memory High bits outputs.

## TABLE 1 — INPUT STREAM TO OUTPUT STREAM COMBINATIONS THAT CAN PROVIDE THE MINIMUM 2-CHANNEL DELAY

| Input | Output Stream |
|-------|---------------|
| 0 | 1,2,3 |
| 1 | 3 |

## TABLE 2 — ADDRESS MAPPING

| A5 | A4 | A3 | A2 | A1 | A0 | HEX ADDRESS | LOCATION |
|----|----|----|----|----|----|-------------|----------|
| 0 | X | X | X | 0 | 0 | 00-1F | Control Register[1] |
| 1 | 0 | 0 | 0 | 0 | 0 | 20 | Channel 0[2] |
| 1 | 0 | 0 | 0 | 0 | 1 | 21 | Channel 1[2] |
| 1 | . | . | . | . | . | . | . |
| 1 | . | . | . | . | . | . | . |
| 1 | . | . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 1 | 3F | Channel 31[2] |

NOTES:
1. Writing to the Control Register is the only fast transaction.
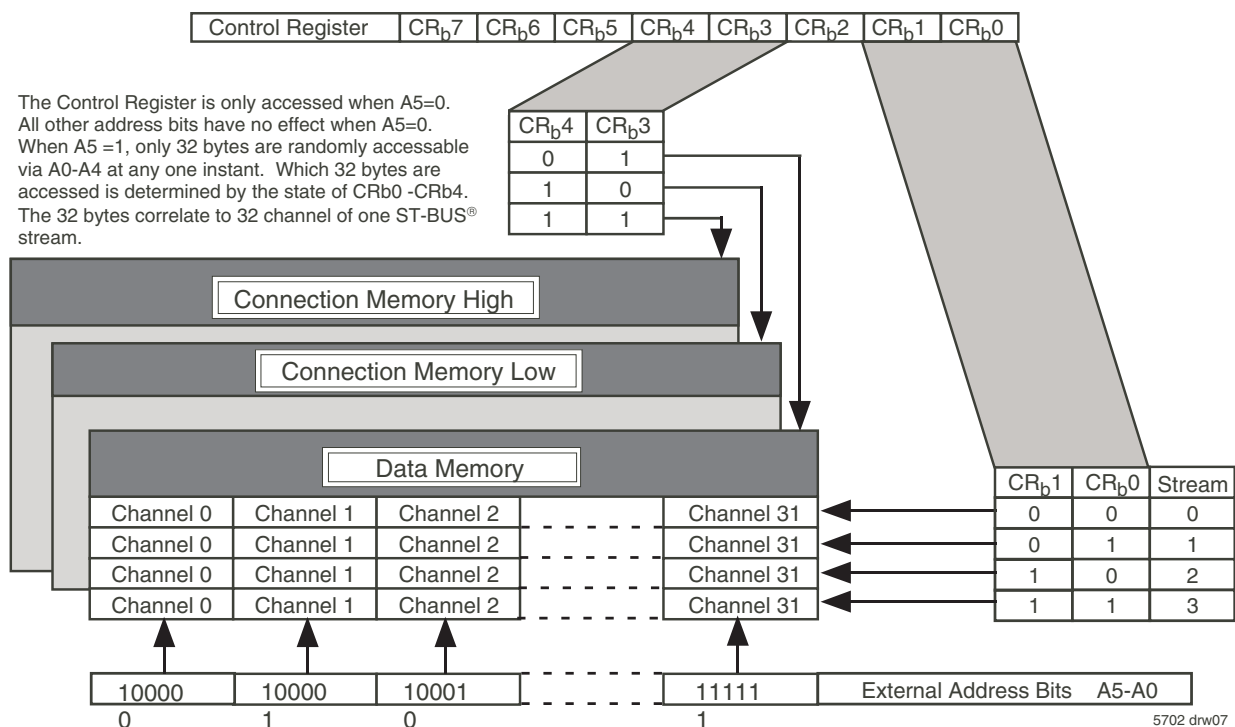2. Memory and stream are specified by the contents of the Control Register.



The Control Register is only accessed when A5=0. All other address bits have no effect when A5=0. When A5 =1, only 32 bytes are randomly accessable via A0-A4 at any one instant. Which 32 bytes are accessed is determined by the state of CRb0 -CRb4. The 32 bytes correlate to 32 channel of one ST-BUS® stream.

*Figure 3. Address Mapping*

## TABLE 3 — CONTROL REGISTER CONFIGURATION

| | Mode Control Bits | | (unused) | Memory Select Bits | | (unused) | Stream Address Bits | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Bit | Name | Description |
|---|---|---|
| 7 | SM (Split Memory) | When 1, all subsequent reads are from the Data Memory and writes are to the Connection Memory LOW, except when the Control Register is accessed again. When 0, the Memory Select bits specify the memory for the operations. In either case, the Stream Address Bits select the subsection of the memory which is made available. |
| 6 | PE (Processor Mode) | When 1, the contents of the Connection Memory LOW are output on the Serial Output streams except when the ODE pin is LOW. When 0, the Connection Memory bits for each channel determine what is output. |
| 5 | | unused |
| 4-3 | MS1-MS0 (Memory Select Bits) | 0-0 - Not to be used.<br>0-1 - Data Memory (read only from the microprocessor port)<br>1-0 - Connection Memory LOW<br>1-1 - Connection Memory is HIGH |
| 2 | | unused |
| 1-0 | STA1-0 (Stream Address Bits) | The number expressed in binary notation on these bits refers to the input or output stream which corresponds to the subsection of memory made accessible for subsequent operations. |

## TABLE 4 — CONNECTION MEMORY HIGH REGISTER

| No Corresponding Memory - These bits give 0s if read | | | | | CS | (unused) | OE |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Bit | Name | Description |
|---|---|---|
| 2 | CS (Channel Source) | When 1, the contents of the corresponding location in Connection Memory LOW are output on the location's channel and stream. When 0, the contents of the corresponding location in Connection Memory LOW act as an address for the Data Memory and determine the source of the connection to the location's channel and stream. |
| 1 | | unused |
| 0 | OE (Output Enable) | If the ODE pin is HIGH and bit 6 of the Control Register is 0, then this bit enables the output driver for the location's channel and stream. This allows individuals channels on individuals streams to be made high-impedance, allowing switching matrices to be constructed. A 1 enables the driver and a 0 disables it. |

## TABLE 5 — CONNECTION MEMORY LOW REGISTER

| (unused) | Stream Address Bits | | Channel Address Bits | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Bit | Name | Description |
|---|---|---|
| 7 | | unused |
| 6-5[1] | Stream Address Bits | The number expressed in binary notation on these 2 bits are the number of the stream for the source of the connection. Bit 6 is the most significant bit, e.g., If bit 6 is 1, bit 5 is 0 then the source of the connection is a channel on RX2. |
| 4-0[1] | Channel Address Bits | The number expressed in binary notation on these 5 bits is the number of the channel which is the source of the connection (the stream where the channel lies is defined by bits 7, 6 and 5). Bit 4 is the most significant bit, e.g., if bit 4 is 1, bit 3 is 0, bit 2 is 0, bit 1 is 1 and bit 0 is 1, then the source of the connection is channel 19. |

NOTE:
1. If bit 2 of the corresponding Connection HIGH location is 1 or bit 6 of the Control Register is 1, then these entire 8 bits are output on the channel and stream associated with this location. Otherwise, the bits are used as indicated to define the source of the connection which is output on the channel and stream associated with this location.

## ABSOLUTE MAXIMUM RATINGS [1]

| Symbol | Parameter | Min. | Max. | Unit |
|--------|-----------|------|------|------|
| $V_{CC}$ | Symbol Voltage | -0.3 | 5 | V |
| $V_I$ | Voltage on Digital Inputs | GND - 0.3 | $V_{CC}$ +0.5 | V |
| $V_O$ | Voltage on Digital Outputs | GND - 0.3 | $V_{CC}$ +0.3 | V |
| $I_O$ | Current at Digital Outputs | | 20 | mA |
| $T_S$ | Storage Temperature | -55 | +125 | °C |
| $P_D$ | Package Power Dissapation | | 1 | W |

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ.[1] | Max. | Unit |
|--------|-----------|------|---------|------|------|
| $V_{CC}$ | Positive Supply | 3.0 | — | 3.6 | V |
| $V_I$ | Input Voltage | 0 | — | 5.25 | V |
| $T_{OP}$ | Operating Temperature Commercial | -40 | 25 | +85 | °C |

**NOTE:**

1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Min. | Typ.[1] | Max. | Units | Test Conditions |
|--------|-----------|------|---------|------|-------|-----------------|
| $I_{CC}$ | Supply Current | — | 3 | 5 | mA | Outputs Unloaded |
| $V_{IH}$ | Input High Voltage | 2.0 | — | — | V | |
| $V_{IL}$ | Input Low Voltage | — | — | 0.8 | V | |
| $I_{IL}$ | Input Leakage | — | — | 15 | µA | $V_I$ between GND and $V_{CC}$ |
| $C_I$ | Input Capacitance | — | — | — | pF | |
| $V_{OH}$ | Output High Voltage | 2.4 | — | — | V | $I_{OH}$ = 10mA |
| $I_{OH}$ | Output High Current | 10 | — | — | mA | Sourcing. $V_{OH}$ = 2.4V |
| $V_{OL}$ | Output Low Voltage | — | — | 0.4 | V | $I_{OL}$ = 5mA |
| $I_{OL}$ | Output Low Current | 5 | — | — | mA | Sinking. $V_{OL}$ = 0.4V |
| $I_{OZ}$ | High Impedance Leakage | — | — | 5 | µA | $V_O$ between GND and $V_{CC}$ |
| $C_O$ | Output Pin Capacitance | — | — | 10 | pF | |

**NOTE:**

1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
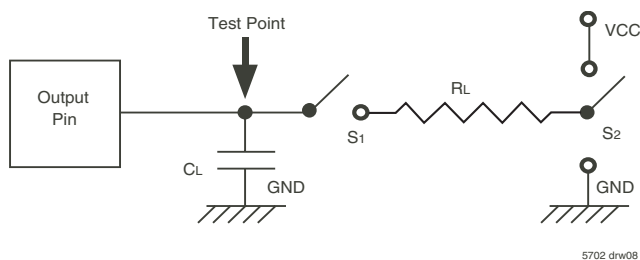


S1 is open circuit except when testing output levels or high impedance states.

S2 is switched to VCC or GND when testing output levels or high impedance states.
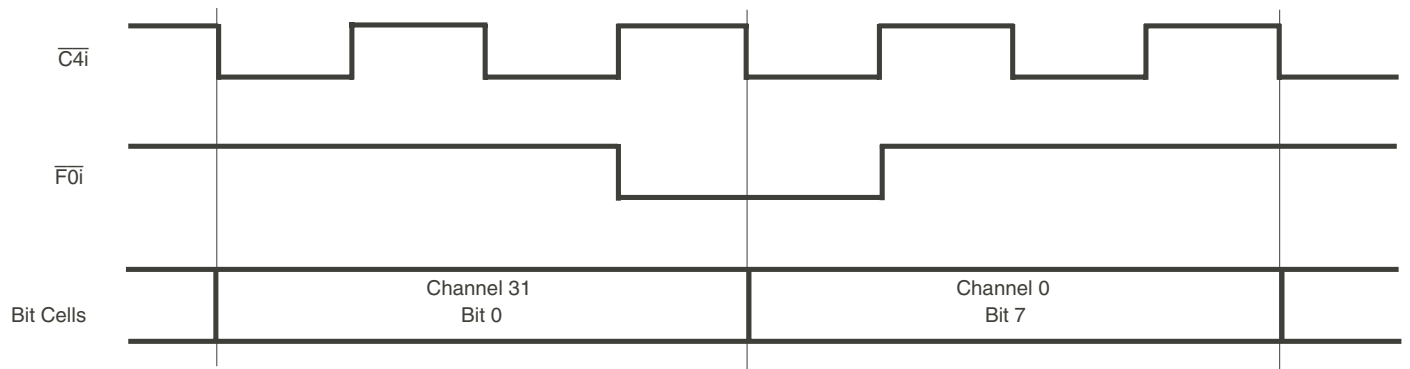
5702 drw08

*Figure 4. Output Load*

# AC ELECTRICAL CHARACTERISTICS [1]— CLOCK TIMING

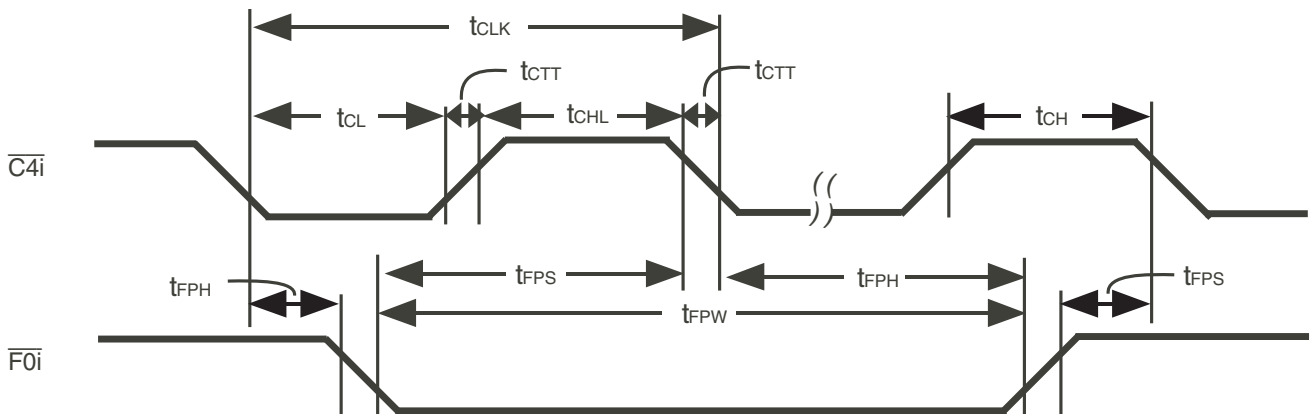| Symbol | Characteristics | Min. | Typ.[2] | Max. | Unit |
|--------|-----------------|------|---------|------|------|
| $t_{CLK}$ | Clock Period[3] | — | 244 | — | ns |
| $t_{CH}$ | Clock Width High | — | 122 | — | ns |
| $t_{CL}$ | Clock Width Low | 110 | 122 | 150 | ns |
| $t_{CTT}$ | Clock Transition Time | — | 20 | — | ns |
| $t_{FPS}$ | Frame Pulse Setup Time | 5 | 20 | 190 | ns |
| $t_{FPH}$ | Frame Pulse Hold Time | 5 | 20 | 190 | ns |
| $t_{FPW}$ | Frame Pulse Width | — | 244 | — | ns |

**NOTE:**
1. Timing is over recommended temperature and power supply voltages.
2. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
3. Contents of Connection Memory are not lost if the clock stops, however, TX output go into the high impedance state.



5702 drw09

*Figure 5. Frame Alignment*



5702 drw10

*Figure 6.  Clock Timing*

## AC ELECTRICAL CHARACTERISTICS [1] — SERIAL STREAM TIMING

| Symbol | Characteristics | Min. | Typ.[2] | Max. | Unit | Test Conditions |
|--------|-----------------|------|---------|------|------|-----------------|
| $t_{TAZ}$ | TX0-3 Delay - Active to High Z | — | 30 | 45 | ns | $R_L = 1K\Omega^{(3)}$, $C_L = 150pF$ |
| $t_{TZA}$ | TX0-3 Delay - High Z to Active | — | 45 | 60 | ns | $C_L = 150pF$ |
| $t_{TAA}$ | TX0-3 Delay - Active to Active | — | 40 | 60 | ns | $C_L = 150pF$ |
| $t_{TOH}$ | TX0-3 Hold Time | 20 | 45 | — | ns | $C_L = 150pF$ |
| $t_{OED}$ | Output Driver Enable Delay | — | 45 | 60 | ns | $R_L = 1K\Omega^{(3)}$, $C_L = 150pF$ |
| $t_{SIS}$ | Serial Input Setup Time | 10 | 20 | — | ns | |
| $t_{SIH}$ | Serial Input Hold Time | 10 | 20 | — | ns | |
| $t_{ZDO}$ | High Z to Valid Data | — | 32 | — | cycles | $\overline{C4i}$ cycles |

NOTE:
1. Timing is over recommended temperature and power supply voltages.
2. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
3. High Impedance is measured by pulling to the appropriate rail with $R_L$, with timing corrected to cancel time taken to discharge $C_L$.
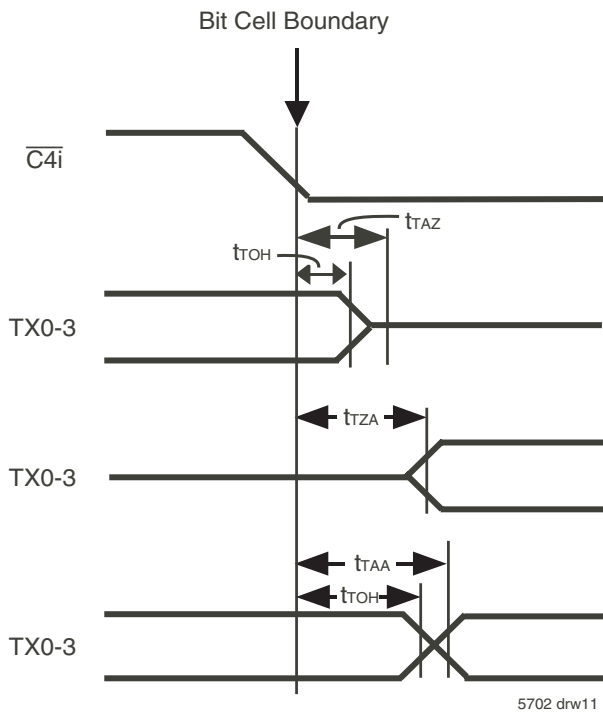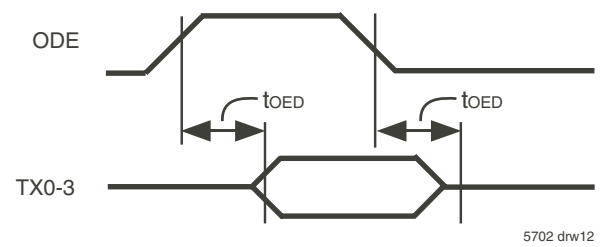


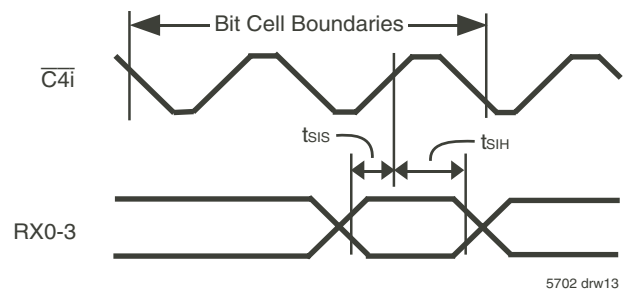Figure 7. *Serial Outputs and External Control*
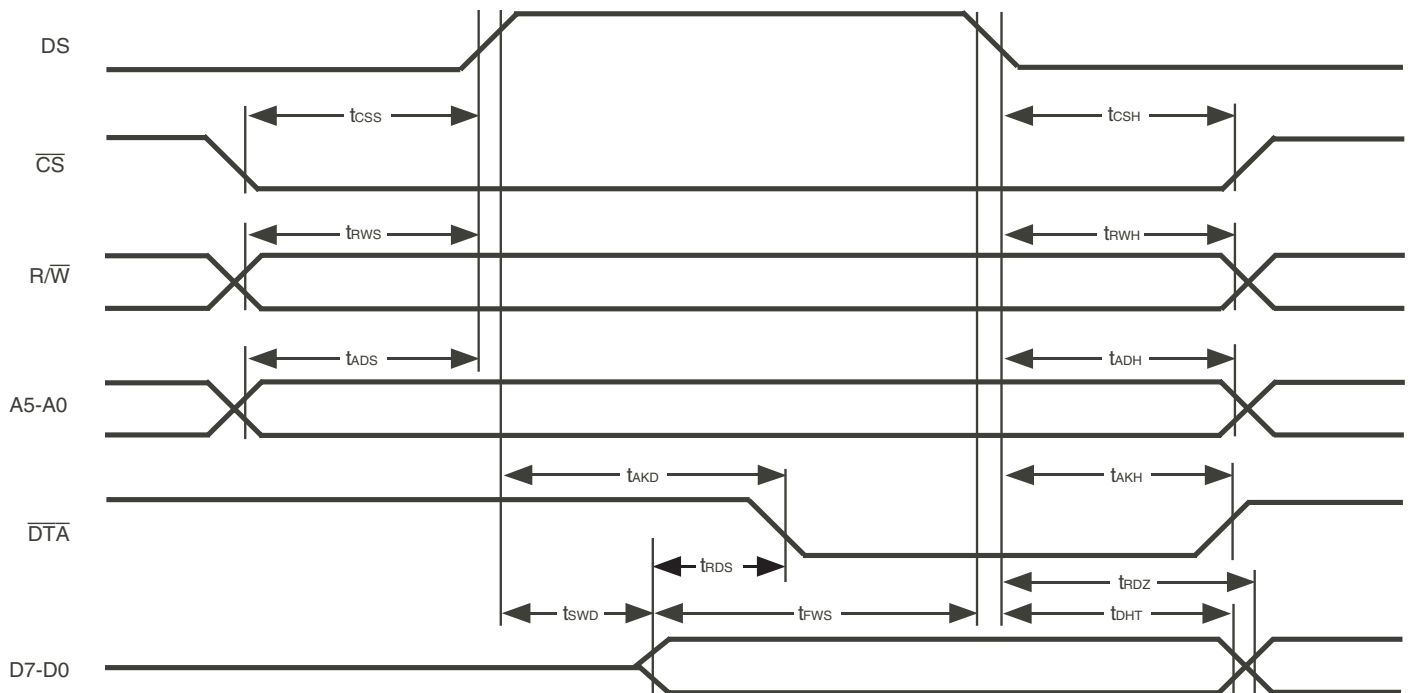


Figure 8. *Output Driver Enable*



Figure 9. *Serial Inputs*

## AC ELECTRICAL CHARACTERISTICS [(1)] — PROCESSOR BUS

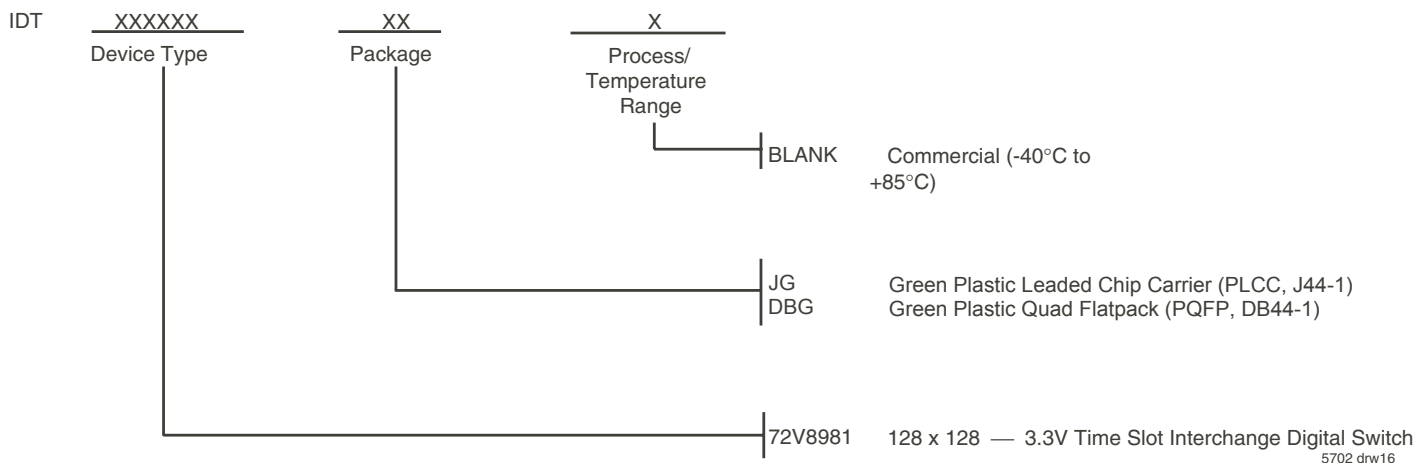| Symbol | Characteristics | Min. | Typ.[(2)] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{CSS}$ | Chip Select Setup Time | 0 | — | — | ns | |
| $t_{RWS}$ | Read/Write Setup Time | 5 | — | — | ns | |
| $t_{ADS}$ | Address Setup Time | 5 | — | — | ns | |
| $t_{AKD}$ | Acknowledgment Delay Fast | — | 40 | 60 | ns | $C_L = 150pF$ |
| $t_{AKD}$ | Acknowledgment Delay Slow | — | — | 4.5 | cycles | $\overline{C4i}$ cycles[(4)] |
| $t_{FWS}$ | Fast Write Data Setup Time | 10 | 20 | — | ns | |
| $t_{SWD}$ | Slow Write Data Delay | — | 2.0 | 1.7 | cycles | $\overline{C4i}$ cycles |
| $t_{RDS}$ | Read Data Setup Time | — | — | 0.5 | cycles | $\overline{C4i}$ cycles, $C_L = 150pF$ |
| $t_{DHT}$ | Data Hold Time Read | 20 | 50 | 75 | ns | $R_L = 1K\Omega^{(3)}$, $C_L = 150pF$ |
| $t_{DHT}$ | Data Hold Time Write | 10 | — | — | ns | |
| $t_{RDZ}$ | Read Data to High Impedance | 10 | 50 | — | ns | $R_L = 1K\Omega^{(3)}$, $C_L = 150pF$ |
| $t_{CSH}$ | Chip Select Hold Time | 0 | 5 | — | ns | |
| $t_{RWH}$ | Read/Write Hold Time | 0 | 5 | — | ns | |
| $t_{ADH}$ | Address Hold Time | 0 | 5 | — | ns | |
| $t_{AKH}$ | Acknowledgment Hold Time | — | 20 | 40 | ns | $R_L = 1K\Omega^{(3)}$, $C_L = 150pF$ |

**NOTE:**
1. Timing is over recommended temperature and power supply voltages.
2. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
3. High Impedance is measured by pulling to the appropriate rail with $R_L$, with timing corrected to cancel time taken to discharge $C_L$.
4. Processor accesses are dependent on the $\overline{C4i}$ clock, and so some things are expressed as multiples of the $\overline{C4i}$.



5702 drw15

*Figure 10. Processor Bus*

# ORDERING INFORMATION

```
IDT    XXXXXX          XX            X
     Device Type     Package    Process/
                                Temperature
                                Range
```

                                                    BLANK      Commercial (-40°C to
                                                               +85°C)

                                                    JG         Green Plastic Leaded Chip Carrier (PLCC, J44-1)
                                                    DBG        Green Plastic Quad Flatpack (PQFP, DB44-1)

                                                    72V8981    128 x 128 — 3.3V Time Slot Interchange Digital Switch

<span style="font-size:smaller">5702 drw16</span>

# DATASHEET DOCUMENT HISTORY