STF6N80K5, STFI6N80K5

N-channel 800 V, 1.3 Ω typ., 4.5 A MDmesh™ K5 Power MOSFETs in TO-220FP and I²PAKFP packages

Datasheet - production data

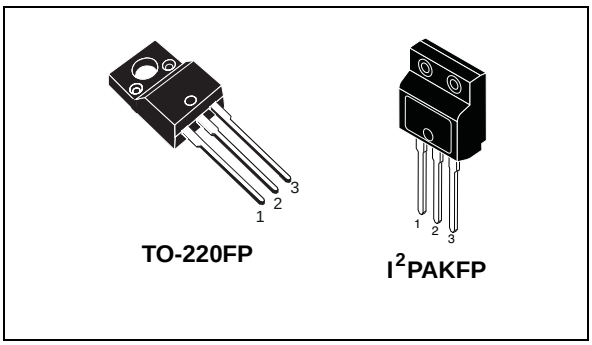
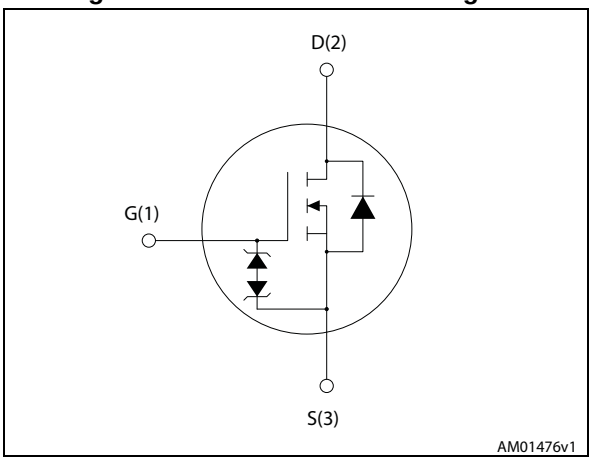


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$max	I_D	P_{TOT}
STF6N80K5	800 V	1.6 Ω	4.5 A	25 W
STFI6N80K5				

- Industry's lowest $R_{DS(on)}$
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

Order code	Marking	Package	Packing
STF6N80K5	6N80K5	TO-220FP	Tube
STFI6N80K5		I²PAKFP	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	30	V
I_D	Drain current (continuous) at T_C = 25 °C	4.5(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	2.8	A
I_{DM} (2)	Drain current (pulsed)	18	A
P_{TOT}	Total dissipation at T_C = 25 °C	25	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	1.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AS}, V_{DD} = 50 V)	85	mJ
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2500	V
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 4.5$ A, di/dt $\leq$ 100 A/µs, peak $V_{DS} \leq V_{(BR)DSS}$
4. $V_{DS} \leq 640$ V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb	62.5	

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 800 V			1	µA
		V_{DS} = 800 V, T_j = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2 A		1.3	1.6	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	270	-	pF
C_{oss}	Output capacitance		-	25	-	pF
C_{rss}	Reverse transfer capacitance		-	0.7	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = from 0 to 640 V	-	38	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	16	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0	-	7.5	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 4.5 A V_{GS} = 10 V (see *Figure 15: Gate charge test circuit*)	-	13	-	nC
Q_{gs}	Gate-source charge		-	2.1	-	nC
Q_{gd}	Gate-drain charge		-	9.6	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 2.25 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: Switching times test circuit for resistive load* and *Figure 19: Switching time waveform*)	-	16	-	ns
t_r	Rise time		-	7.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	28.5	-	ns
t_f	Fall time		-	16	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-		18	A
V_{SD}(2)	Forward on voltage	I_{SD} = 4.5 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A, V_{DD} = 60 V di/dt = 100 A/µs, (see *Figure 16: Test circuit for inductive load switching and diode recovery times*)	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.2		µC
I_{RRM}	Reverse recovery current		-	15.5		A
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A,V_{DD} = 60 V di/dt = 100 A/µs, Tj = 150 °C (see *Figure 16: Test circuit for inductive load switching and diode recovery times*)	-	450		ns
Q_{rr}	Reverse recovery charge		-	3.15		µC
I_{RRM}	Reverse recovery current		-	14		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1mA, I_D = 0	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection,thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

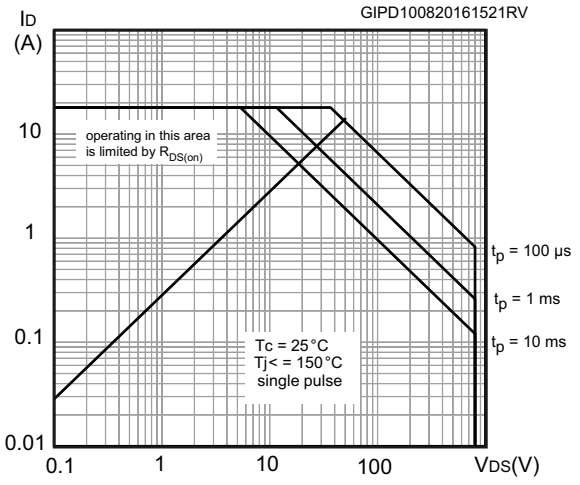


Figure 3. Thermal impedance

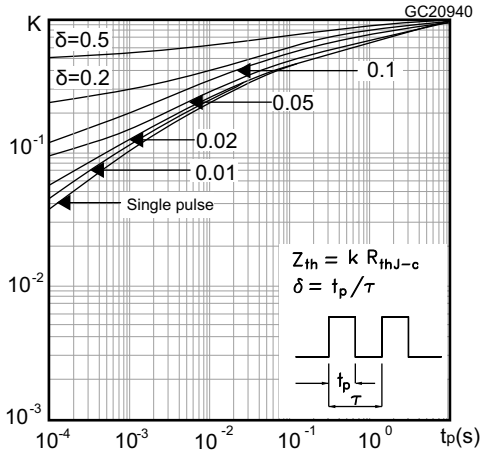


Figure 4. Output characteristics

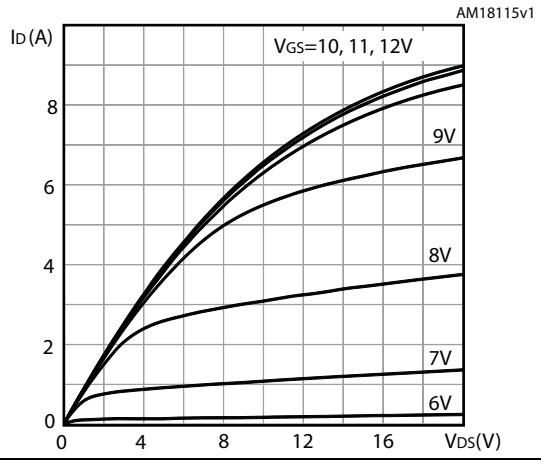


Figure 5. Transfer characteristics

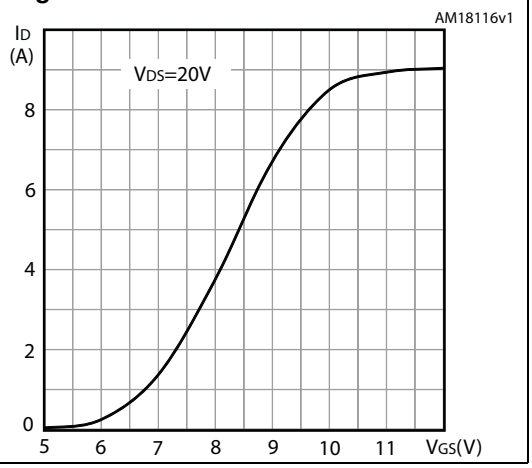


Figure 6. Gate charge vs gate-source voltage

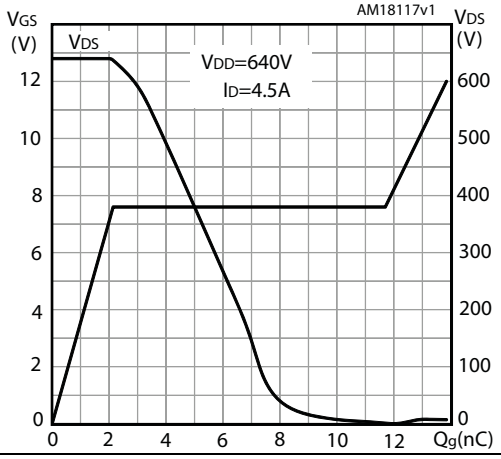


Figure 7. Static drain-source on-resistance

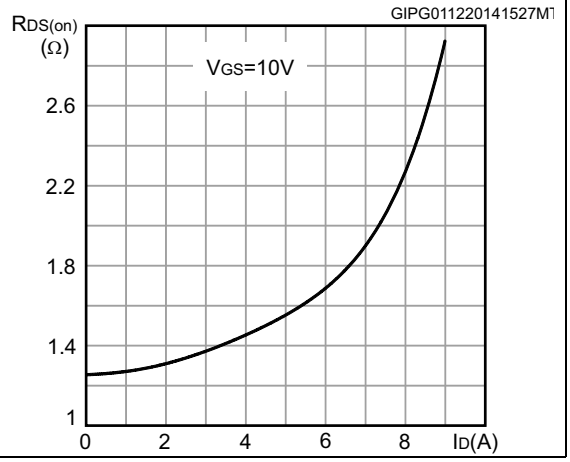


Figure 8. Capacitance variations

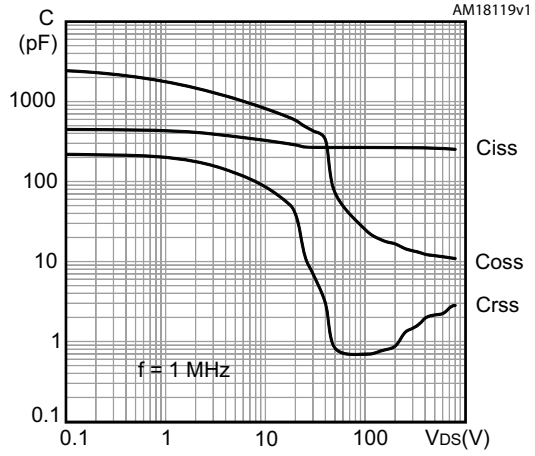


Figure 9. Output capacitance stored energy

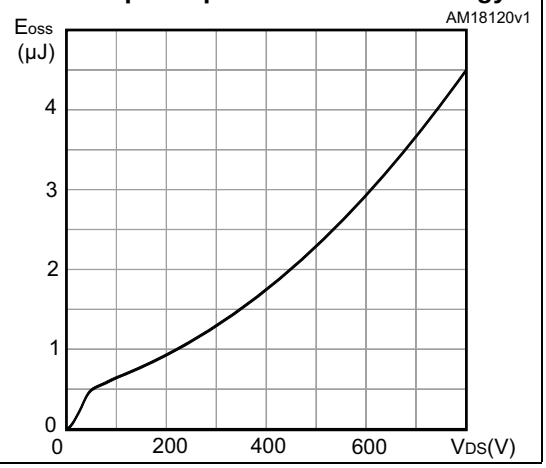


Figure 10. Normalized gate threshold voltage vs temperature

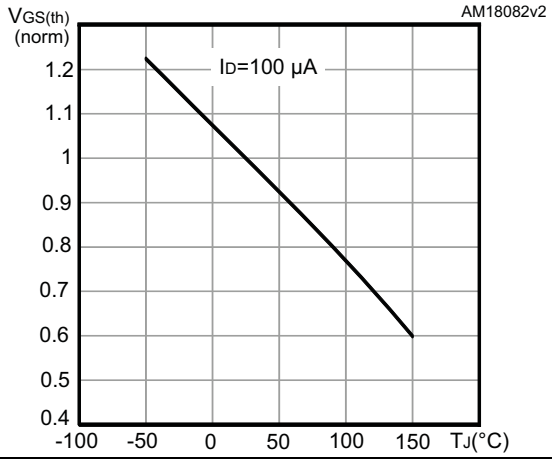


Figure 11. Normalized on-resistance vs temperature

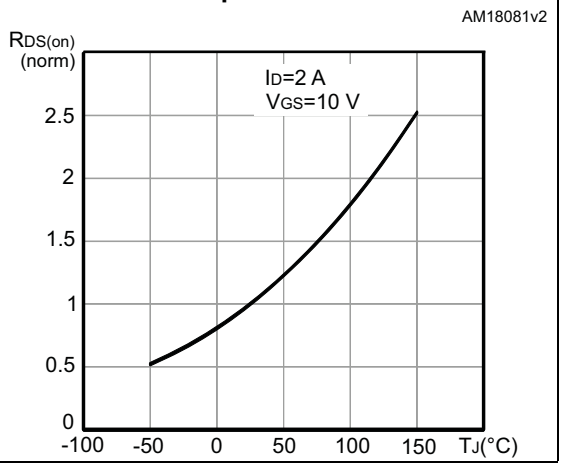


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

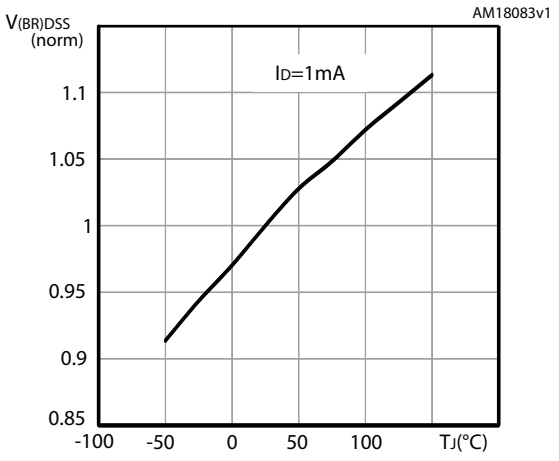
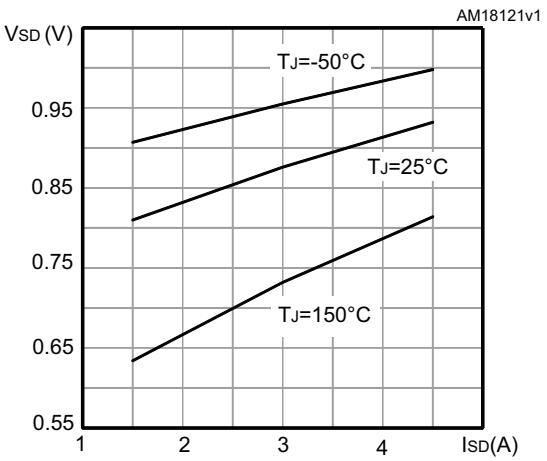


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

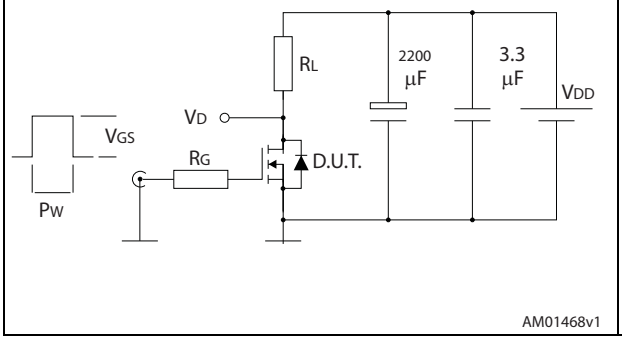


Figure 15. Gate charge test circuit

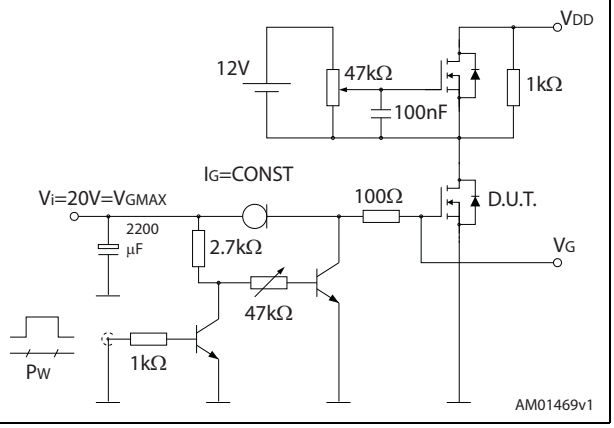


Figure 16. Test circuit for inductive load switching and diode recovery times

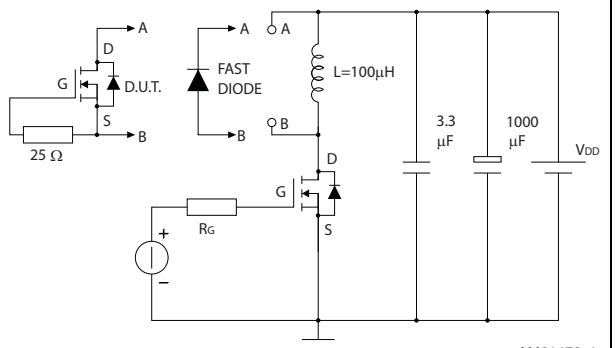


Figure 17. Unclamped inductive load test circuit

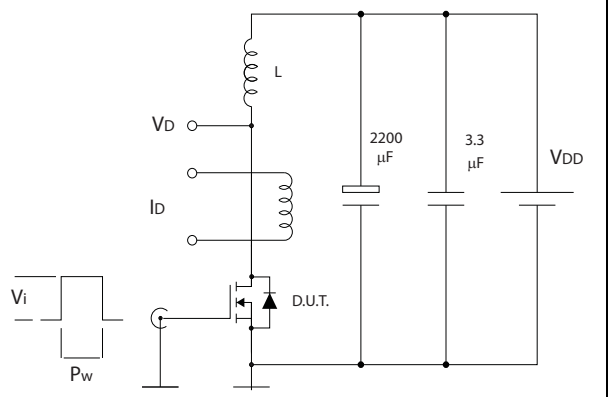


Figure 18. Unclamped inductive waveform

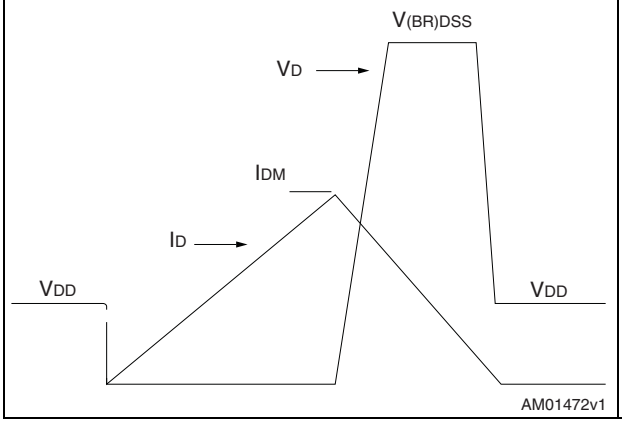
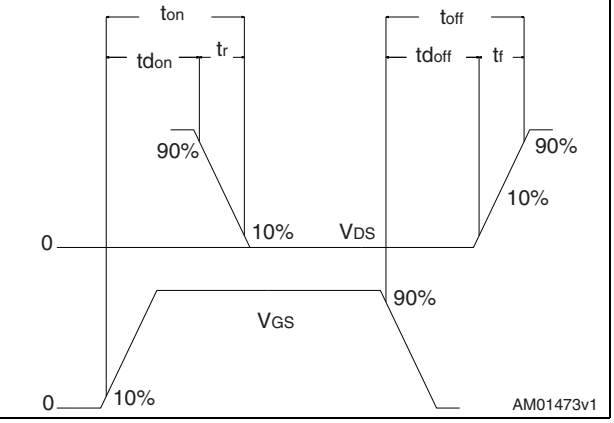


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 20. TO-220FP package outline

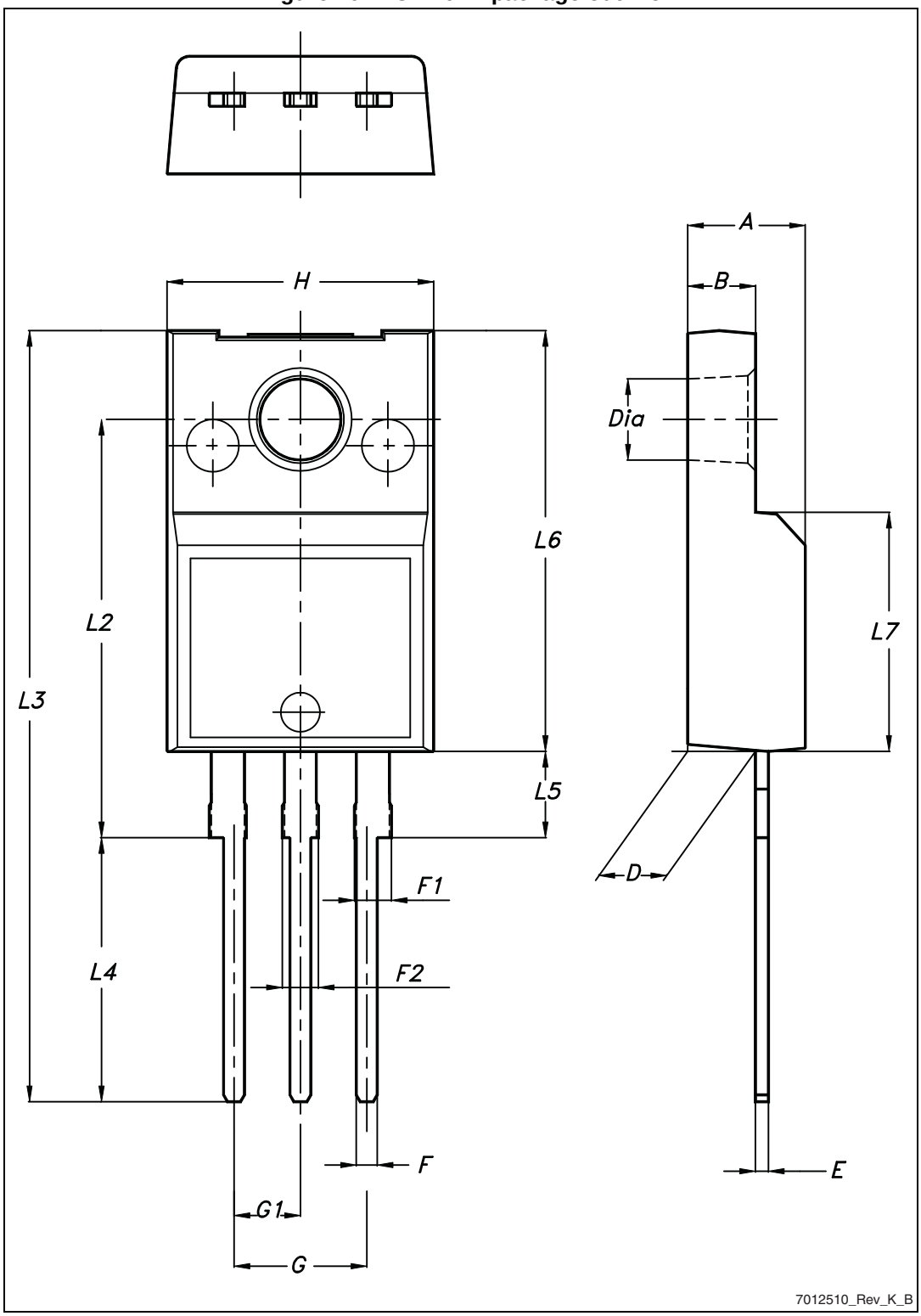


Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.2 I²PAKFP (TO-281) package information

Figure 21. I²PAKFP (TO-281) package outline

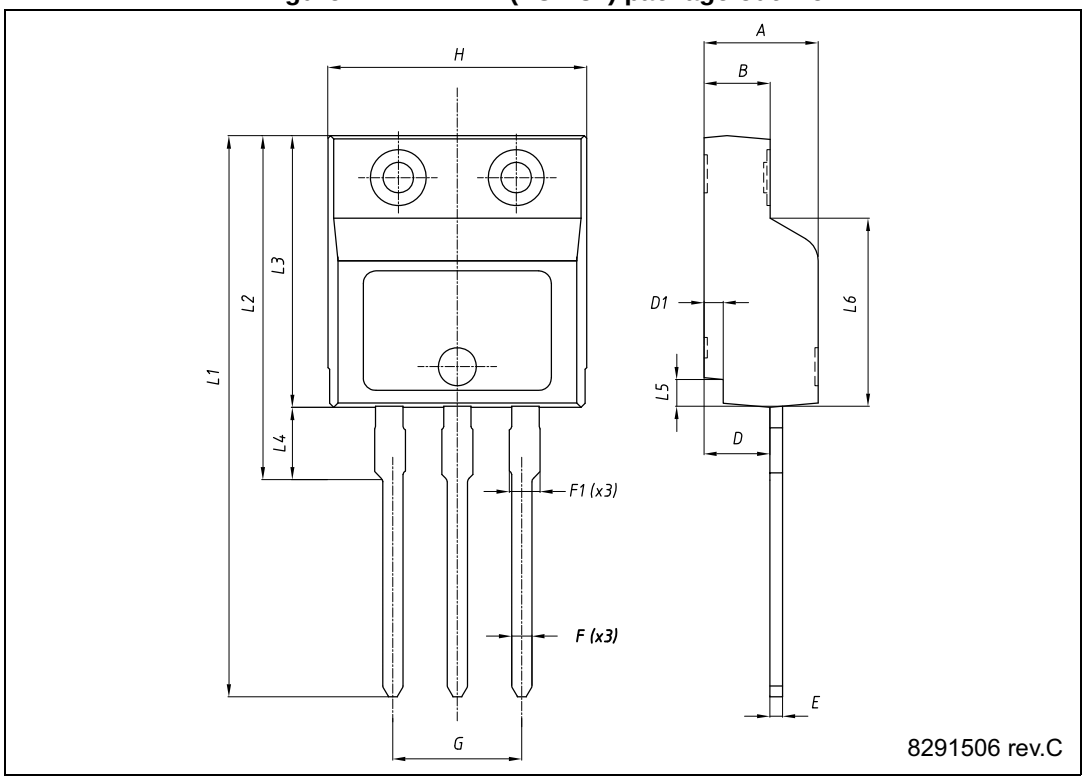


Table 10. I^2PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

5 Revision history

Table 11. Document revision history

Date	Revision	Changes
28-May-2013	1	First release.
05-Mar-2014	2	– Datasheet status promoted from preliminary data to production data – Added: I^2PAKFP package – Modified: E_{AS} value in *Table 2* – Added: MOSFET dv/dt ruggedness test condition and *note 4* in *Table 2* – Modified: R_G value in *Table 5* – Modified: the entire typical values in *Table 5, 6 and 7* – Added: *Section 2.1: Electrical characteristics (curves)* – Minor text changes
05-Dec-2014	3	Updated title, features and description in cover page. Updated *Section 2.1: Electrical characteristics (curves)* and *Section 4: Package information*. Minor text changes.
06-Sept-2016	4	Updated *Table 2: Absolute maximum ratings* ,*Table 4: On/off states*, *Table 5: Dynamic*, *Table 6: Switching times*, and *Table 7: Source drain diode*. Updated *Figure 2: Safe operating area* and *Figure 3: Thermal impedance*. Minor text changes.