

74HC4040-Q100; 74HCT4040-Q100

12-stage binary ripple counter

Rev. 1 — 24 March 2014

Product data sheet

1. General description

The 74HC4040-Q100; 74HCT4040-Q100 is a 12-stage binary ripple counter with a clock input (\overline{CP}), an overriding asynchronous master reset input (\overline{MR}) and twelve parallel outputs (Q_0 to Q_{11}). The counter advances on the HIGH-to-LOW transition of \overline{CP} . A HIGH on \overline{MR} clears all counter stages and forces all outputs LOW, independent of the state of \overline{CP} . Each counter stage is a static toggle flip-flop. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ For 74HC4040-Q100: CMOS level
 - ◆ For 74HCT4040-Q100: TTL level
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- Multiple package options

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4040D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4040D-Q100				
74HC4040DB-Q100	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4040DB-Q100				
74HC4040PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4040PW-Q100				
74HC4040BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4040BQ-Q100				

5. Functional diagram

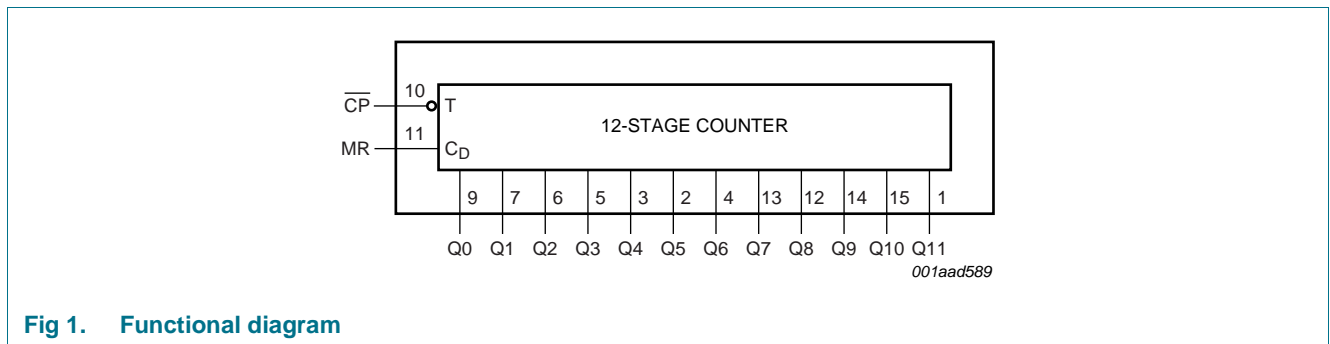


Fig 1. Functional diagram

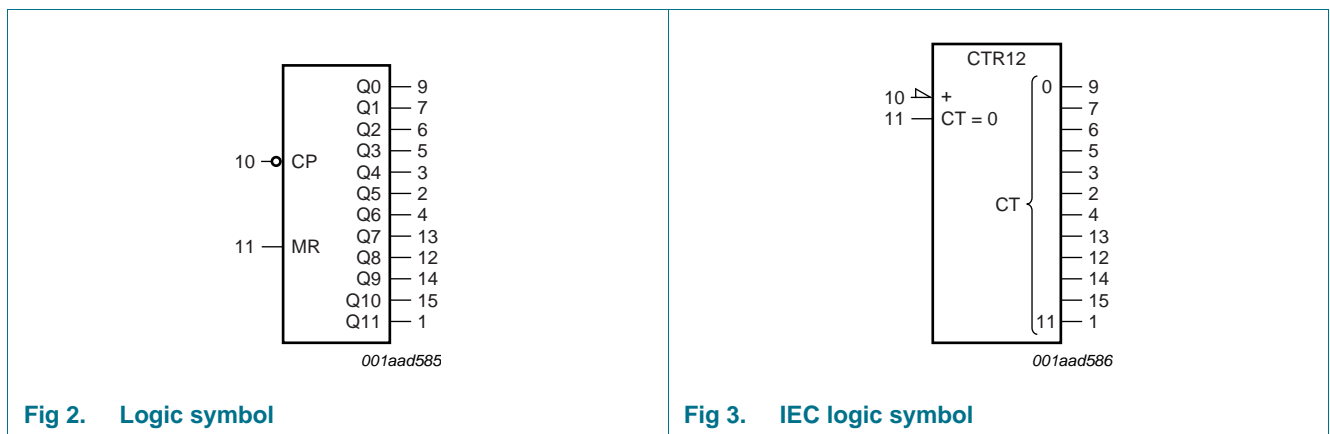


Fig 2. Logic symbol

Fig 3. IEC logic symbol

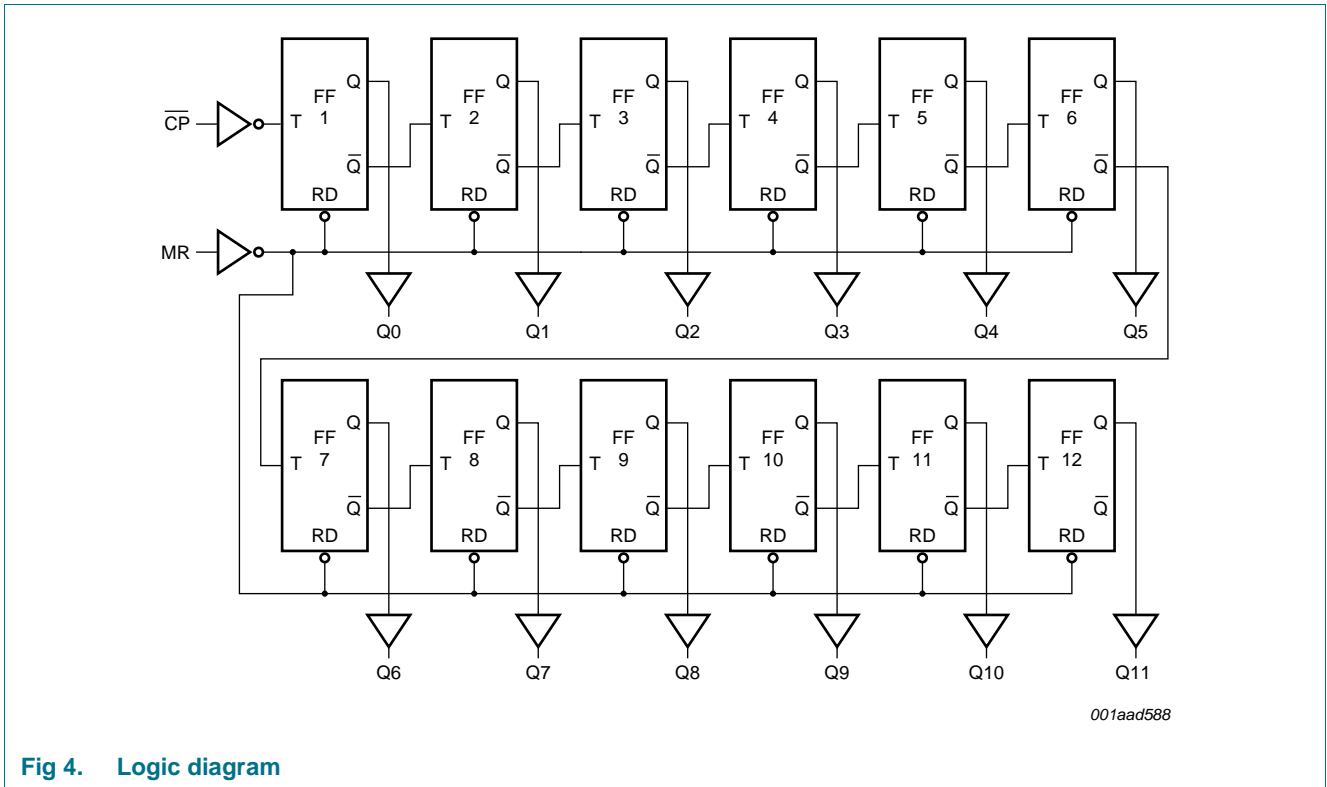
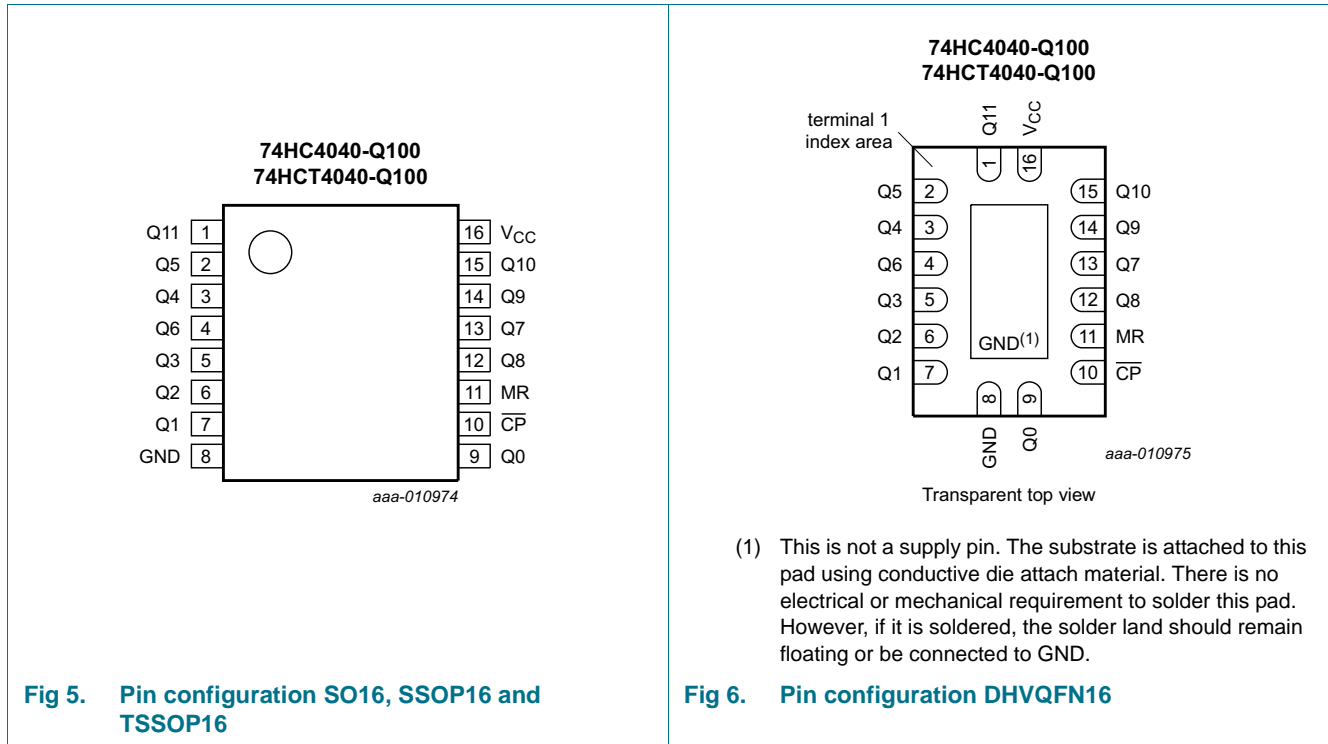


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11	1	output 11
Q5	2	output 5
Q4	3	output 4
Q6	4	output 6
Q3	5	output 3
Q2	6	output 2
Q1	7	output 1
GND	8	ground (0 V)
Q0	9	output 0
CP	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
Q8	12	output 8
Q7	13	output 7
Q9	14	output 9
Q10	15	output 10
V _{CC}	16	positive supply voltage

7. Functional description

7.1 Function table

Table 3. Function table

Input		Output
CP	MR	Q0 to Q11
↑	L	no change
↓	L	count
X	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

7.2 Timing diagram

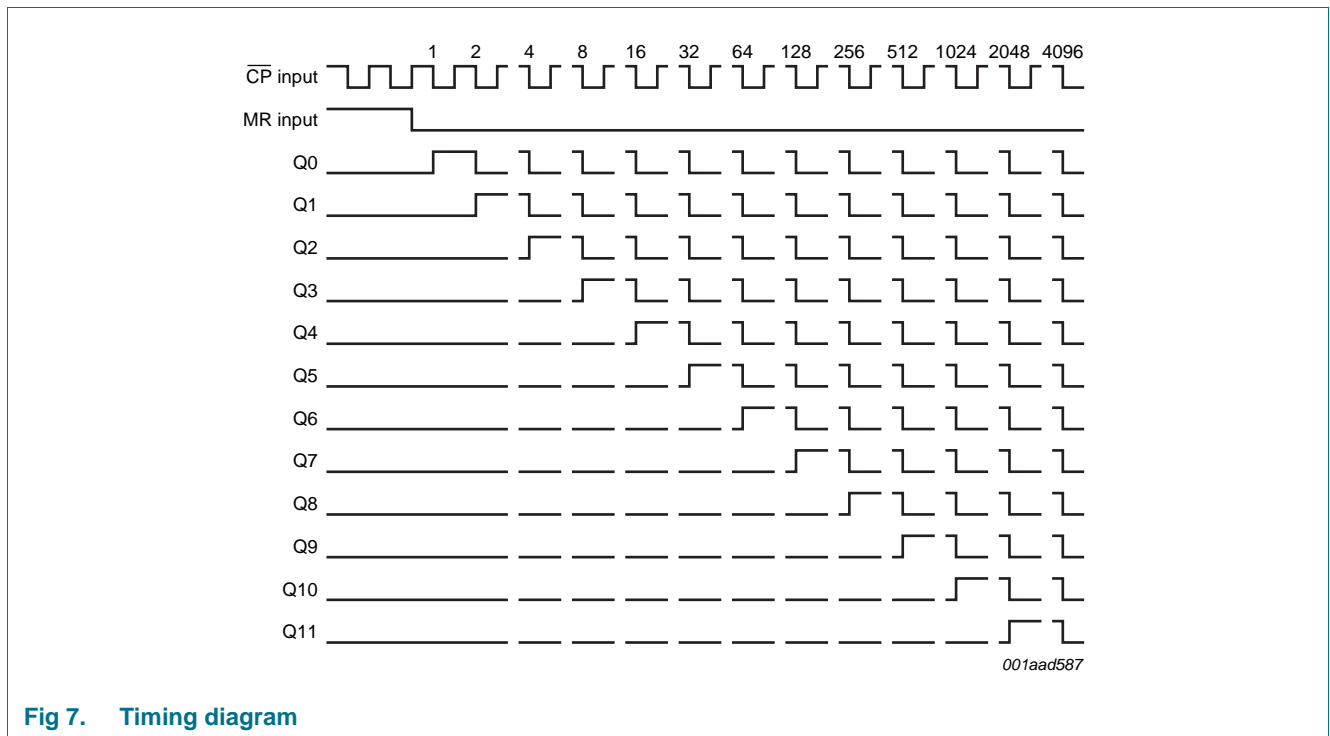


Fig 7. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	± 50	mA
I_{GND}	ground current		-	± 50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [1]	-	500	mW

[1] For SO16, SSOP16, TSSOP16 and DHVQFN16 packages, above 70 °C, P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4040-Q100			74HCT4040-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4040-Q100										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C _I	input capacitance		-	3.5	-					pF
74HCT4040-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		pin $\overline{\text{CP}}$	-	85	306	-	383	-	417	μA
		pin MR	-	110	396	-	495	-	539	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4040-Q100										
t_{pd}	propagation delay	CP to Q0; see Figure 8 ^[1]								
		$V_{CC} = 2.0$ V	-	47	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	17	30	-	38	-	45	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	26	-	33	-	38	ns
		Qn to Qn+1; see Figure 8								
		$V_{CC} = 2.0$ V	-	28	100	-	125	-	150	ns
		$V_{CC} = 4.5$ V	-	10	20	-	25	-	30	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	8	-	-	-	-	ns	
		$V_{CC} = 6.0$ V	-	8	17	-	21	-	26	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 8								
		$V_{CC} = 2.0$ V	-	61	185	-	230	-	280	ns
		$V_{CC} = 4.5$ V	-	22	37	-	46	-	56	ns
		$V_{CC} = 6.0$ V	-	18	31	-	39	-	48	ns
t_t	transition time	Qn; see Figure 8 ^[2]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns
t_w	pulse width	CP input, HIGH or LOW; see Figure 8								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns
		MR input, HIGH; see Figure 8								
		$V_{CC} = 2.0$ V	80	22	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	ns	
t_{rec}	recovery time	MR to CP; see Figure 8								
		$V_{CC} = 2.0$ V	50	8	-	65	-	75	-	ns
		$V_{CC} = 4.5$ V	10	3	-	13	-	15	-	ns
		$V_{CC} = 6.0$ V	9	2	-	11	-	13	-	ns
f_{max}	maximum frequency	CP input; see Figure 8								
		$V_{CC} = 2.0$ V	6	27	-	4.8	-	4	-	MHz
		$V_{CC} = 4.5$ V	30	82	-	24	-	20	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	90	-	-	-	-	-	MHz
		$V_{CC} = 6.0$ V	35	98	-	28	-	24	-	MHz

Table 7. Dynamic characteristics ...continuedGND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ [3]	-	20	-	-	-	-	-	pF
74HCT4040-Q100										
t_{pd}	propagation delay	$\overline{\text{CP}}$ to Q0; see Figure 8 [1]								
		$V_{CC} = 4.5$ V	-	19	40	-	50	-	60	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	16	-	-	-	-	-	ns
		Qn to Qn+1; see Figure 8								
		$V_{CC} = 4.5$ V	-	10	20	-	25	-	30	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	8	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 8								
		$V_{CC} = 4.5$ V	-	23	45	-	56	-	68	ns
t_t	transition time	Qn; see Figure 8 [2]								
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
t_W	pulse width	$\overline{\text{CP}}$ input, HIGH or LOW; see Figure 8								
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns
		MR input, HIGH; see Figure 8								
		$V_{CC} = 4.5$ V	16	6	-	20	-	24	-	ns
t_{rec}	recovery time	MR to $\overline{\text{CP}}$; see Figure 8								
		$V_{CC} = 4.5$ V	10	2	-	13	-	15	-	ns
f_{max}	maximum frequency	$\overline{\text{CP}}$ input; see Figure 8								
		$V_{CC} = 4.5$ V	30	72	-	24	-	20	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	79	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ [3]	-	20	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} , t_{PLH} .[2] t_t is the same as t_{THL} , t_{TLH} .[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

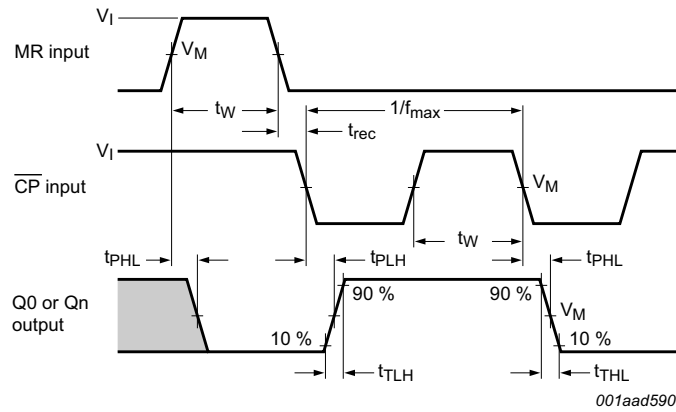
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{CC} = supply voltage in V;

N = number of inputs switching;

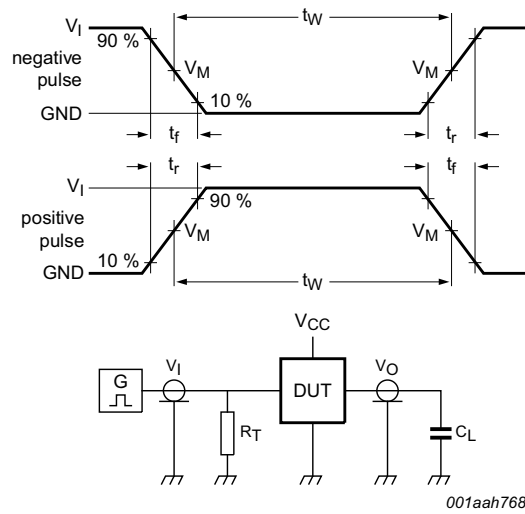
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveform and test circuit



74HC4040-Q100: $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 74HCT4040-Q100: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig 8. Clock propagation delays, pulse width, transition times, maximum pulse frequency and master resets



001aah768

Test data is given in [Table 8](#).

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig 9. Test circuit for measuring switching times

Table 8. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC4040-Q100	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT4040-Q100	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

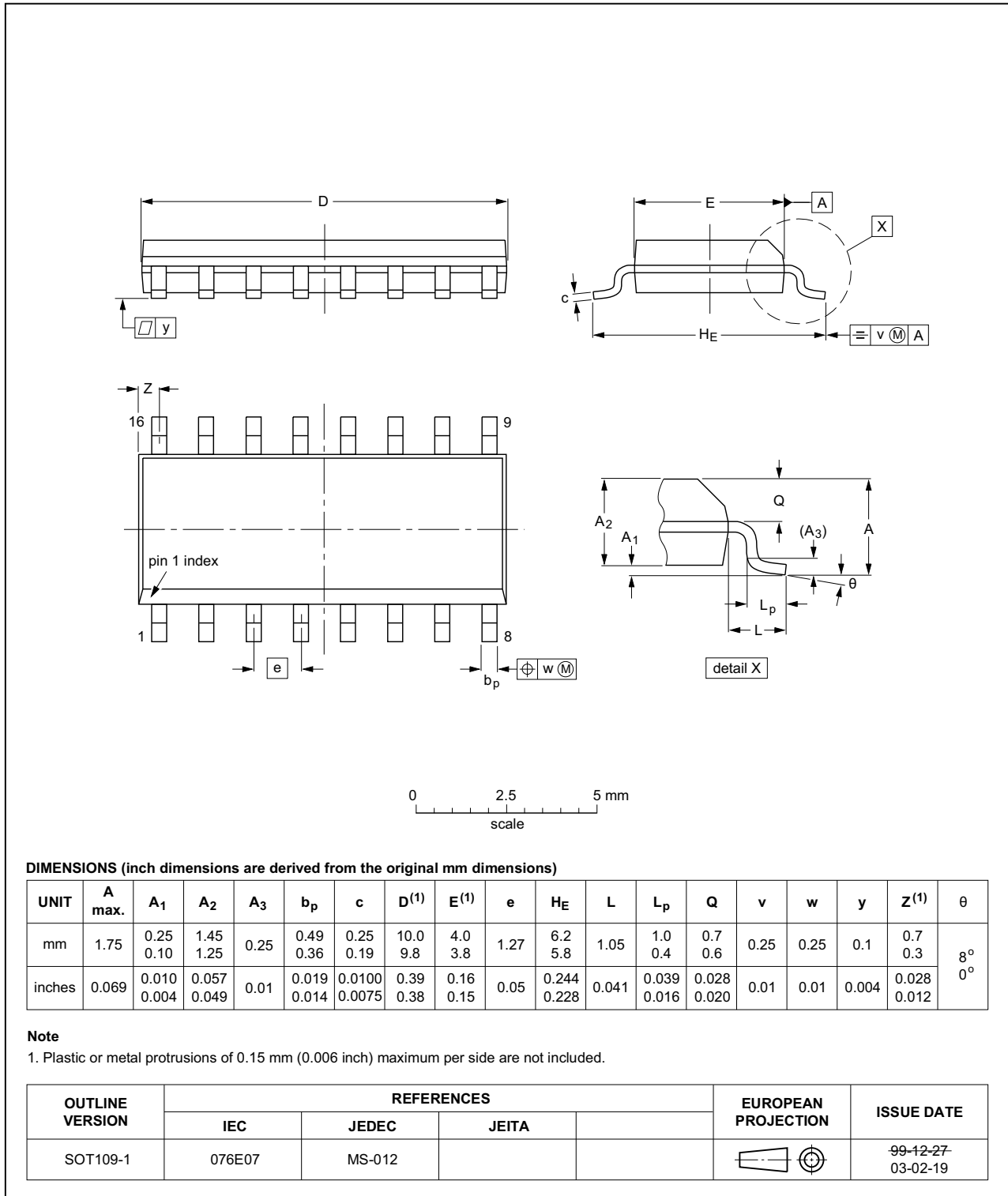


Fig 10. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

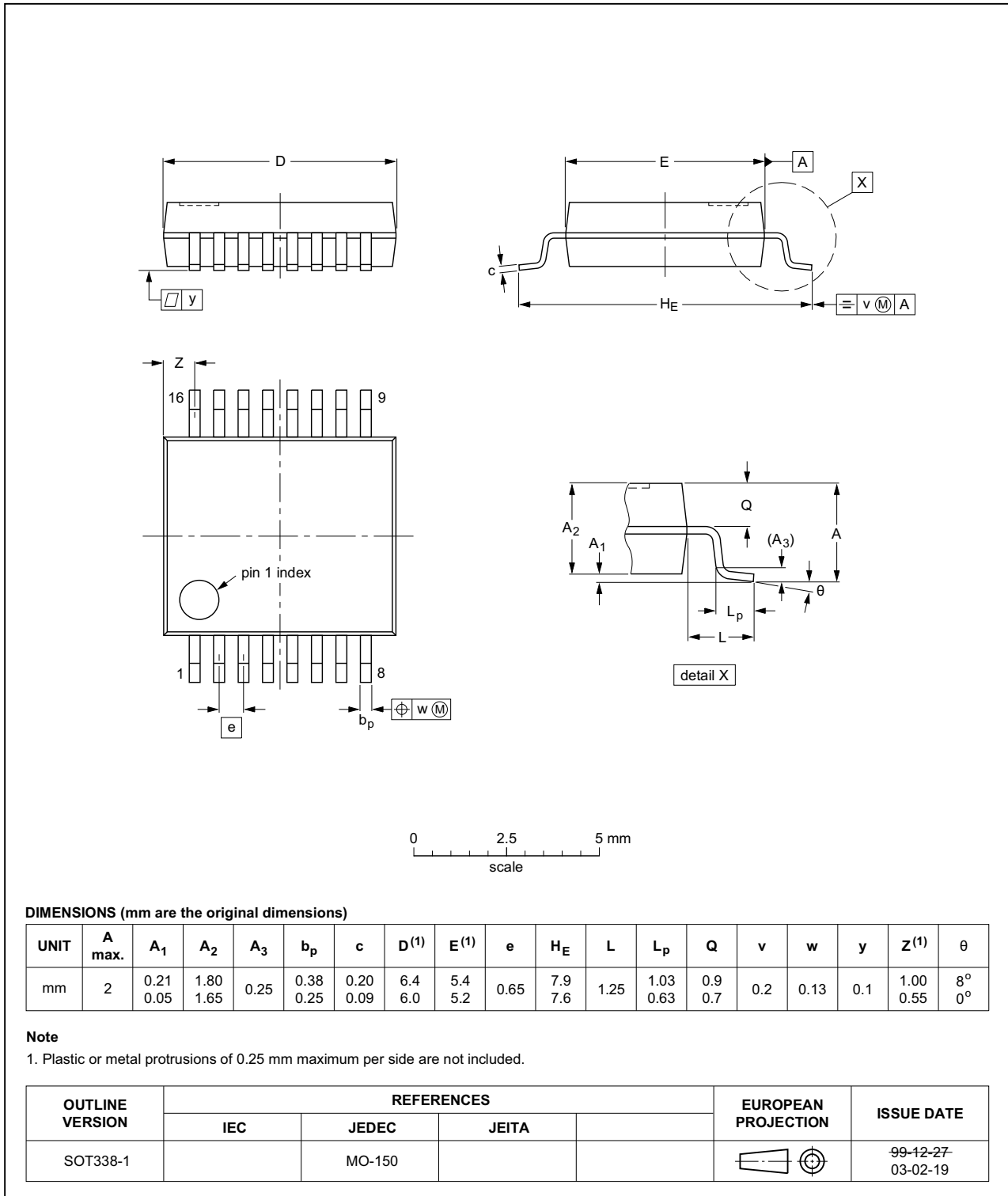


Fig 11. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

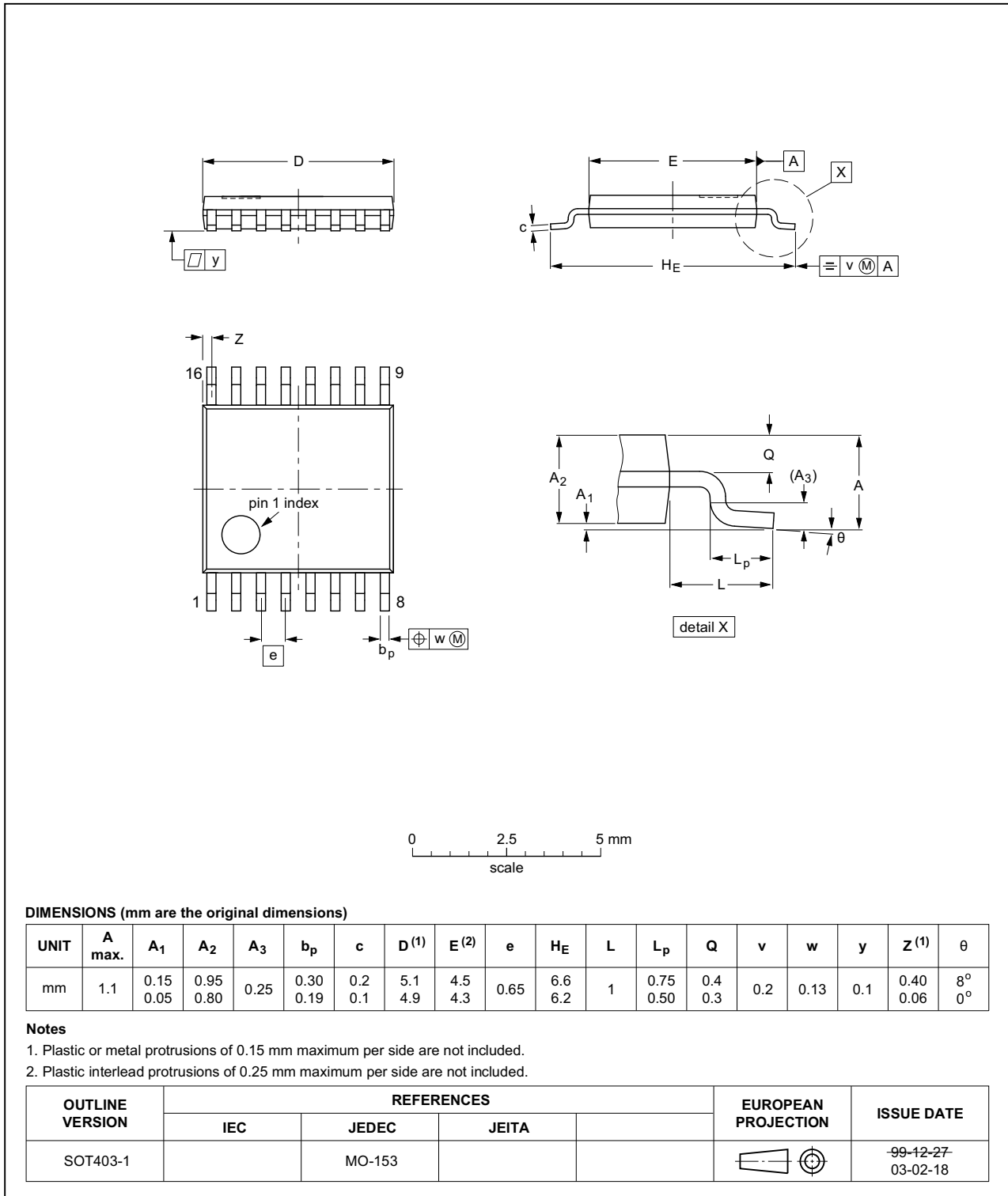


Fig 12. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

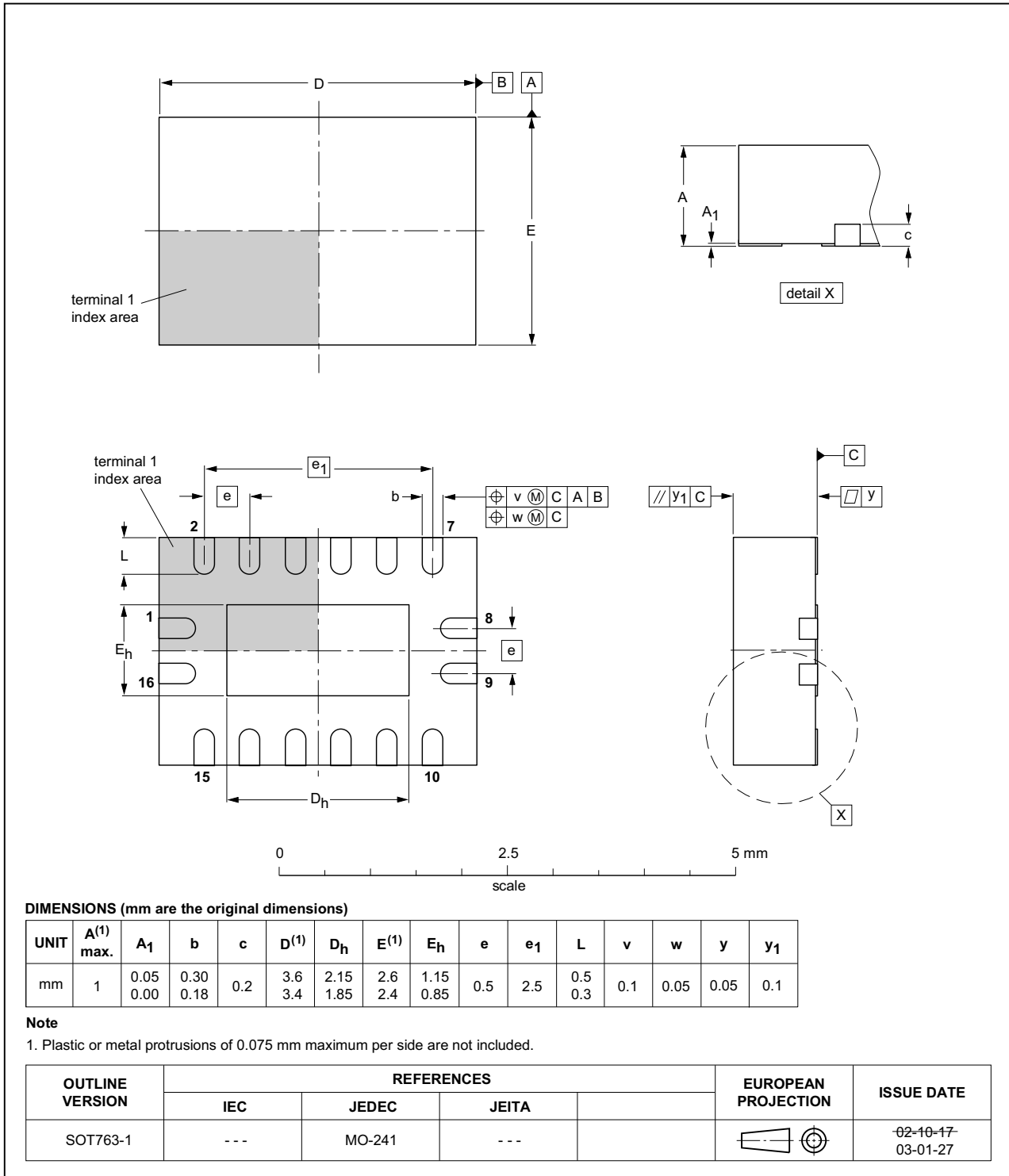


Fig 13. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
TTL	Transistor-Transistor Logic

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4040_Q100 v.1	20140324	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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17. Contact information

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

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