

ISL8215M

15A 42V Single-Channel DC/DC Step-Down Power Module

FN8878
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The [ISL8215M](#) power module is a single-channel, synchronous step-down, non-isolated complete power supply, capable of delivering up to 15A of continuous current. Operating from a single 7V to 42V wide input power rail and integrating the controller, power inductor, and MOSFETs, the ISL8215M requires only a few external components to operate and is optimized for space constrained applications.

Based on a valley current mode PWM control scheme, the ISL8215M provides fast transient response and excellent loop stability. It offers an adjustable output voltage range of 0.6V to 12V with better than 1.5% accuracy over line, load, and temperature. A 40ns typical minimum on time and an adjustable operating frequency allow it to support low duty cycle, single-step down conversions to point-of-load voltages and its operating frequency can also be synchronized with an external clock signal. The ISL8215M implements a selectable Pulse Skipping Mode (PSM) with Diode Emulation Mode (DEM) to improve light-load efficiency for battery related applications. A programmable soft-start reduces the inrush current from the input supply while a dedicated enable pin and power-good flag allow for easy system power rails sequencing with voltage tracking capability. Excellent efficiency and low thermal resistance permit full power operation without heatsinks.

Input Undervoltage Lockout (UVLO), over-temperature, programmable overcurrent, output overvoltage, and output prebias start-up protections ensure safe operations under abnormal operating conditions.

The ISL8215M is available in a compact RoHS compliant thermally-enhanced 19mm x 13mm x 5.3mm HDA package.

Features

- 15A single-channel complete power supply
 - Integrates controller, MOSFETs, and inductor
- 7V to 42V wide input voltage range
- Adjustable output voltage
 - 0.6V to 12V wide output voltage range
 - 40ns on-time low duty cycle conversion capable
 - ±1.5% accuracy over line, load, and temperature
 - Up to 96.5% efficiency
- 300kHz to 2MHz adjustable PWM operations
 - External synchronization up to 1MHz
 - Selectable light-load PSM/DEM efficiency mode
- Enable pin and power-good flag
- Programmable soft-start or voltage tracking
- Complete protection
 - UVLO, programmable overcurrent, overvoltage, and over-temperature
 - Prebias output start-up
- 19mm x 13mm x 5.3mm HDA package

Applications

- Industrial and medical equipment
- Aftermarket automotive
- Telecom and datacom equipment

Related Literature

- For a full list of related documents, visit our website
 - [ISL8215M](#) product page

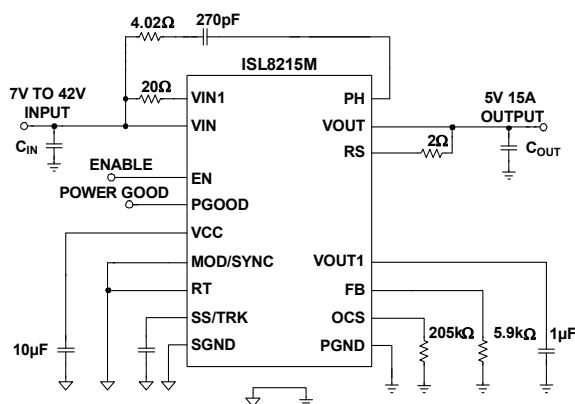


Figure 1. Typical Application Circuit

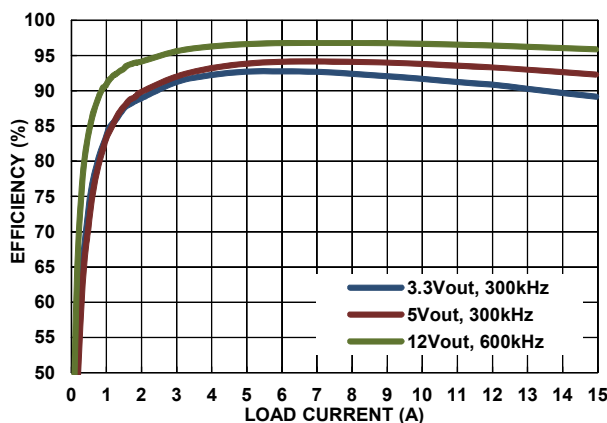


Figure 2. $V_{IN} = 24V$

Table of Contents

1.	Overview	4
1.1	Typical Application Circuits	4
1.2	Block Diagram	6
1.3	Ordering Information	6
1.4	Pin Configuration	7
1.5	Pin Descriptions	7
2.	Specifications	10
2.1	Absolute Maximum Ratings	10
2.2	Thermal Information	10
2.3	Recommended Operating Conditions	10
2.4	Electrical Specifications	11
3.	Typical Performance Curves	14
3.1	Efficiency Performance	14
3.2	Output Voltage Ripple	15
3.3	Load Transient Response Performance	16
3.4	Start-Up Waveforms	17
3.5	Derating	17
4.	Functional Description	19
4.1	Power-Good Indicator	19
4.2	Self-Enable Operation	19
4.3	Enable	19
4.4	Prebiased Power-Up	19
4.5	PWM/CCM Mode	20
4.6	PSM/DEM Light-Load Efficiency Mode	20
4.7	Internal 5V Linear Regulator (VCC)	20
4.8	Gate Control Logic Optimization	20
5.	Application Information	21
5.1	Output Voltage Programming	21
5.2	Switching Frequency Selection	21
5.3	External Frequency Synchronization	22
5.4	Soft-Start Operation	22
5.5	Tracking Operation	23
5.6	Input Voltage Range	24
5.7	Input Capacitor Selection	24
5.8	Output Capacitor Selection	25
6.	Protection Circuits	26
6.1	Undervoltage Lockout	26
6.2	Overcurrent Protection	26
6.3	Overvoltage Protection	27
6.4	Over-Temperature Protection	27

7.	Layout Guidelines	28
7.1	Layout Considerations	28
8.	Thermal Considerations	30
9.	Package Description	31
9.1	PCB Layout Pattern Design	31
9.2	Thermal Vias	31
9.3	Stencil Pattern Design	31
9.4	Reflow Parameters	32
10.	Revision History	33
11.	Package Outline Drawing	34
12.	About Intersil	41

1. Overview

1.1 Typical Application Circuits

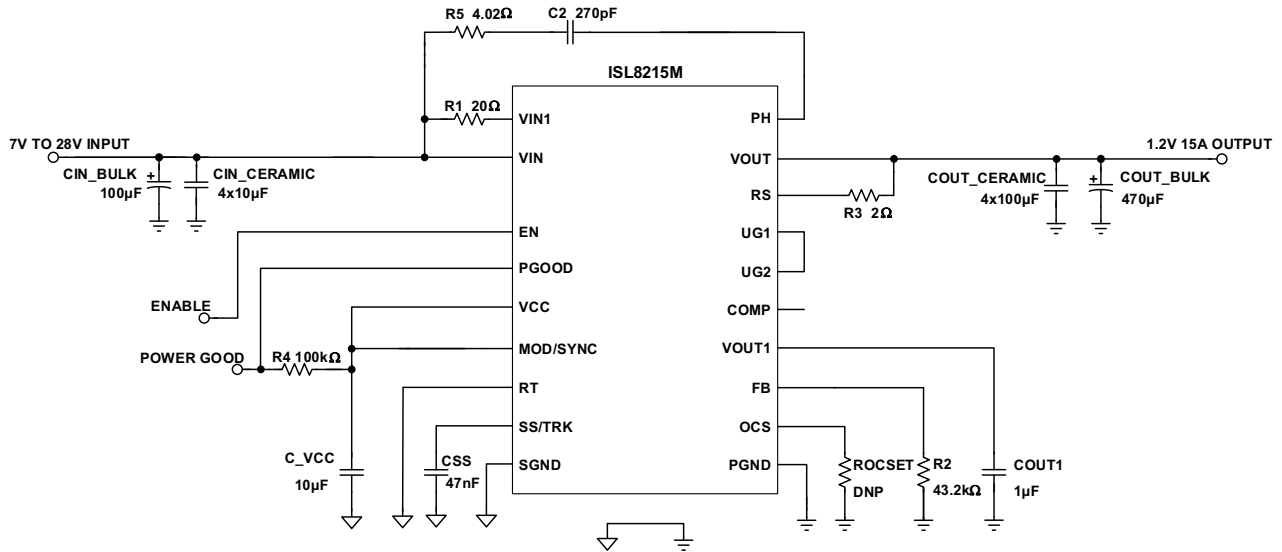


Figure 3. $V_{OUT} = 1.2V$, $f_{sw} = 300kHz$, Light-Load Mode, $t_{SS} = 15ms$

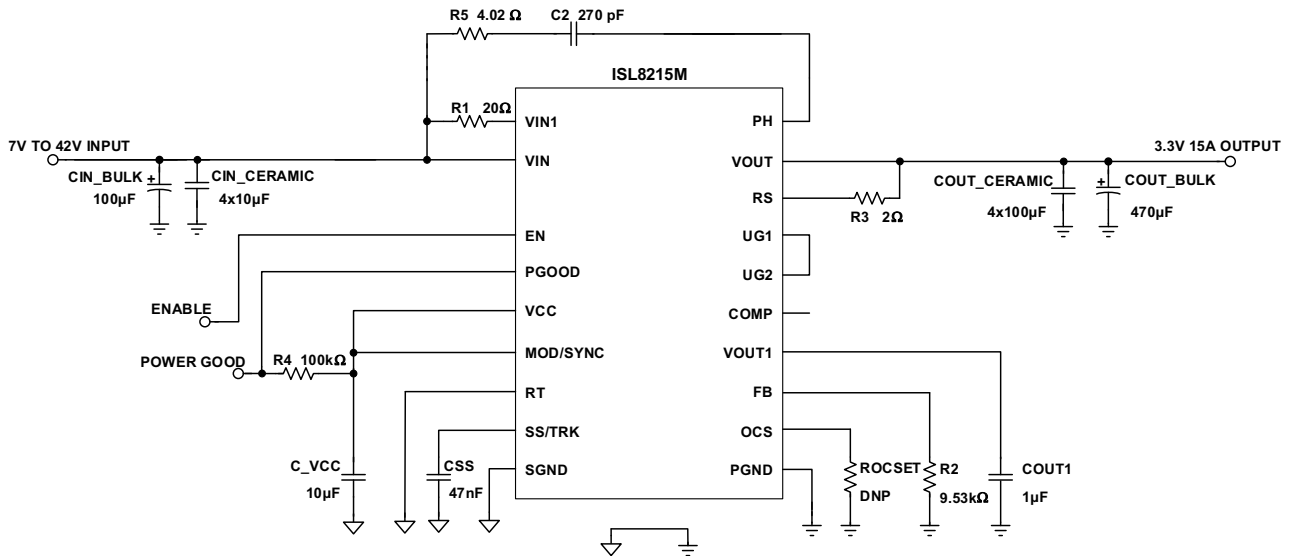


Figure 4. $V_{OUT} = 3.3V$, $f_{sw} = 300kHz$, Light-Load Mode, $t_{SS} = 15ms$

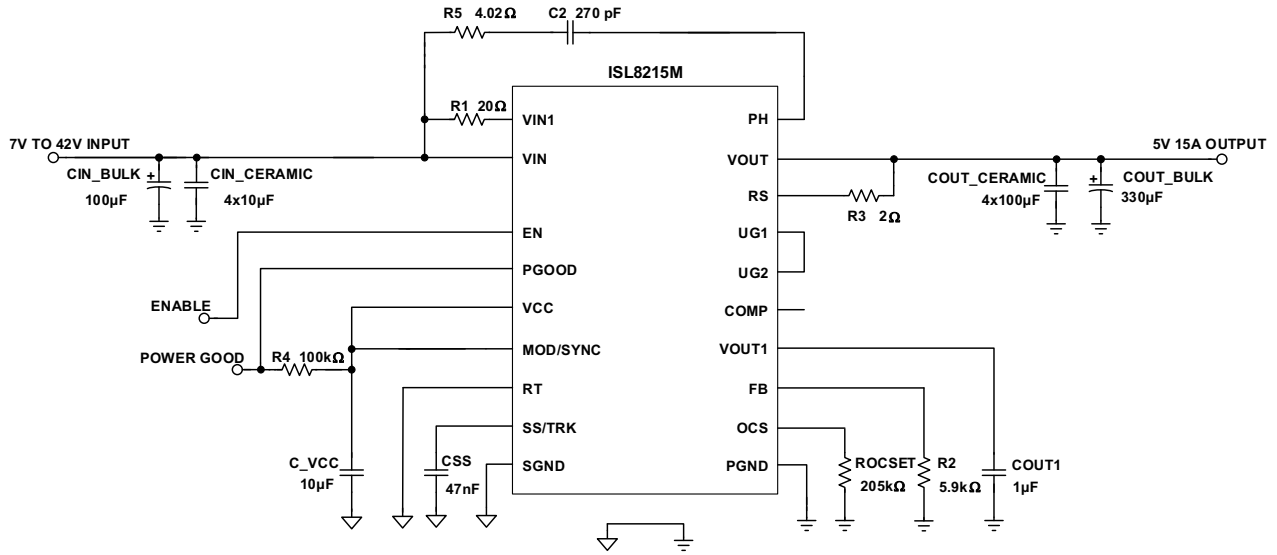


Figure 5. $V_{OUT} = 5V$, $f_{SW} = 300kHz$, Light-Load Mode, $t_{SS} = 15ms$

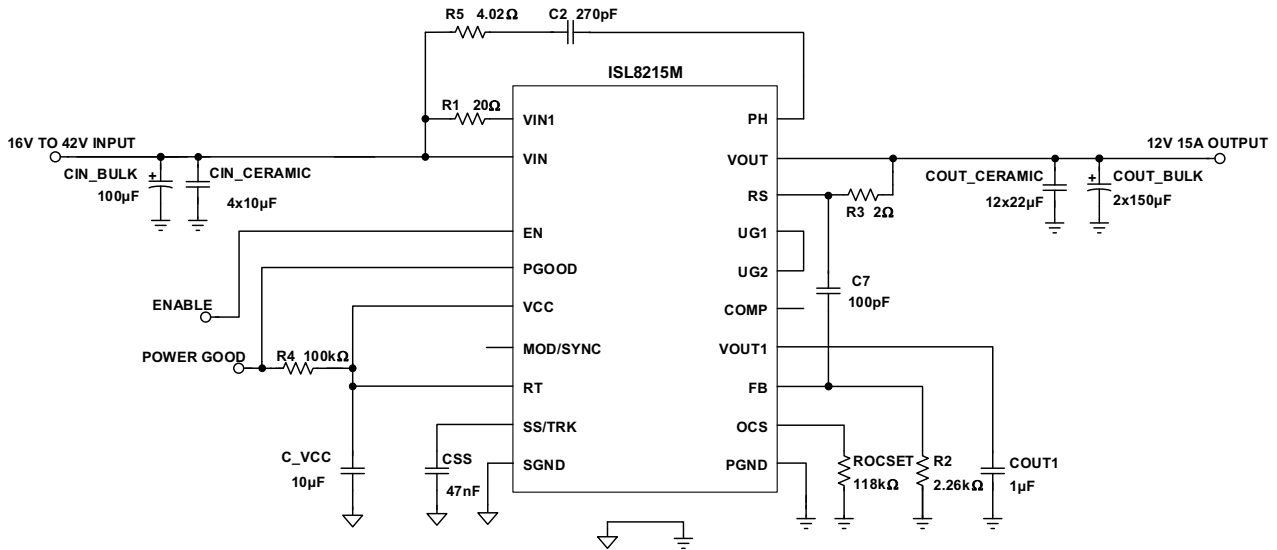


Figure 6. $V_{OUT} = 12V$, $f_{SW} = 600kHz$, PWM Only, $t_{SS} = 15ms$

1.2 Block Diagram

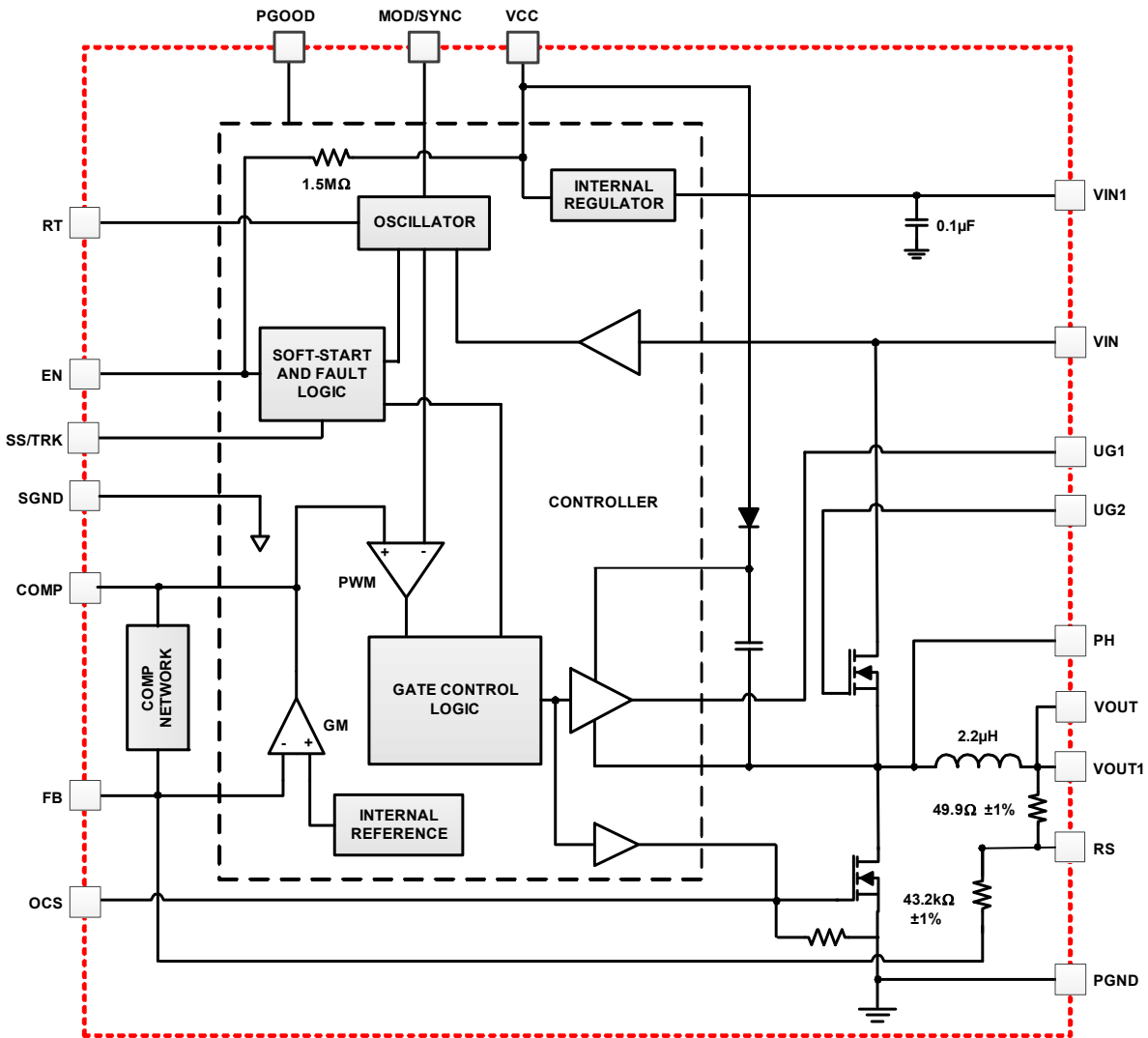


Figure 7. Block Diagram

1.3 Ordering Information

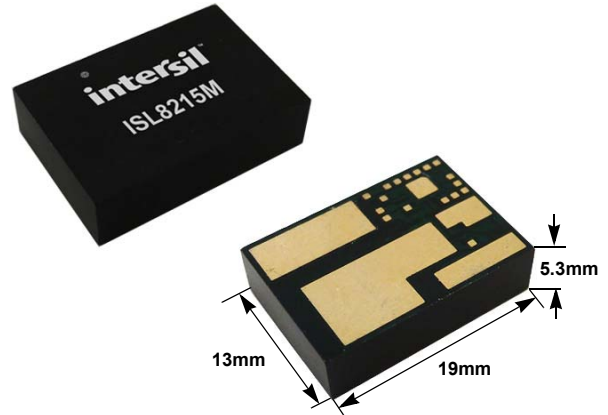
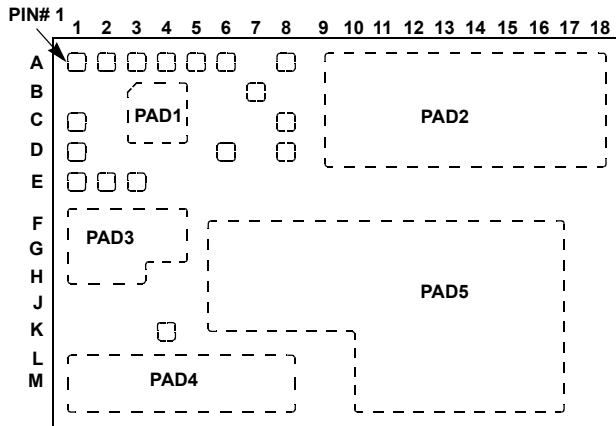
Part Number (Notes 1, 2, 3)	Part Marking	Temp. Range (°C)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL8215MIRZ	ISL8215M	-40 to +125	19x13 HDA	Y22.19x13
ISL8215MEVAL1Z	Evaluation Board			

Notes:

1. Add "-T" suffix for 350 unit or "-T1" suffix for 100 unit tape and reel options. Refer to [TB347](#) for details on reel specifications.
2. These Intersil plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish which is compatible with both SnPb and Pb-free soldering operations. Intersil RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see product information page for [ISL8215M](#). For information on Moisture Sensitivity Level (MSL), see [TB363](#).

1.4 Pin Configuration

ISL8215M
(22 Ld 19x13 HDA)
Top View



1.5 Pin Descriptions

Pin Number	Pin Name	Function
PAD1	SGND	Signal ground. The small-signal ground is common to all control circuitry and all voltage levels are measured with respect to this pin. SGND should be tied to a solid low noise GND plane. See "Layout Considerations" on page 28 and Figure 48 on page 29 for details.
PAD2	VOUT	Regulated power supply output. Output load should be applied between this pin and PGND. An external resistor on the FB pin sets the output voltage in a range of 0.6V to 12V. Refer to derating curves for maximum load current at various output voltage.
PAD3	PGND	Power ground. This pin is connected to the source of the lower MOSFET inside the module and should be connected to the (-) terminals of the external input capacitors and output capacitors.
PAD4	VIN	Power input. This pin should be connected directly to an input rail in a range of 7V to 42V. Input ceramic capacitors should be connected between this pin and PGND as close as possible to the device.
PAD5	PH	Phase node connection. This pin is connected to the junction of the high-side MOSFET's source, output filter inductor, and low-side MOSFET's drain. For a switching frequency of 300kHz and a 42V input, a 4.02Ω 1206 resistor and a 270pF X7R 100V 0603 capacitor in series from PH to VIN (see Figures 3 through 6) are required. Refer to "Layout Considerations" on page 28 for details.
A1	COMP	Voltage error amplifier output. Internal compensation networks are implemented to stabilize the system and achieve optimal transient response across the full range of input and output operating conditions. Leave this pin floating.
A2	SS/TRK	Soft-start/tracking pin. Connecting a capacitor from this pin to signal ground sets the soft-start output voltage ramp rate. For tracking control, an external supply rail applied to this pin via a resistor divider will be tracked by the output voltage. Leave this pin floating to enable a soft-start time of 1.5ms. Refer to "Tracking Operation" on page 23 .
A3	RT	Switching frequency selection. Connect to SGND to set the operating frequency to 300kHz. Connect to VCC or float this pin to set the operating frequency to 600kHz. Connect a resistor from RT to SGND to program the switching frequency. Refer to the "Switching Frequency Selection" on page 21 .
A4	PGOOD	Open-drain, power-good output. PGOOD signal is asserted when the output voltage is within ±12.5% of the nominal set output voltage and de-asserted when the output voltage is outside of the stated range or the EN pin is pulled low.

Pin Number	Pin Name	Function
A5	MOD/SYNC	Light-load mode selection/synchronization input. Connect to VCC to enable light load PSM/DEM mode with pulse skipping at light loads. Connect to SGND or leave floating to enable constant frequency PWM only mode. Connect to external clock to synchronize the internal switching operations to an external clock; PWM mode only.
A6, A8	EN	Enable inputs. Connect to logic high level or left floating to enable the device. An internal pull-up resistor allows for self enable operations upon application of VIN. Connect to logic low level or SGND: Disables the device. These two pins should be connected together externally through a PCB trace.
B7	VIN1	This pin should be tied to the input rail through a 20Ω 0603 resistor. It provides power to the internal linear drive circuitry and is also used by the feed-forward controller to adjust the amplitude of the PWM sawtooth.
C1	FB	Feedback input. Connect a resistor between this pin and SGND to adjust the output voltage. Refer to “Output Voltage Programming” on page 21 .
D1	RS	Output voltage remote sense feedback. Connect to the positive output regulation point. To achieve best regulation performance, connect a 2Ω resistor between the RS pin and the point of load. An internal 49.9Ω resistor connected between the RS pin and the VOUT1 pin can be used for injecting a small signal for loop gain measurements.
D6	UG1	High-side MOSFET gate driver output. Connect this pin to UG2, externally through a PCB trace.
K4	UG2	Pin connected to the gate of high-side MOSFET. Connect this pin to UG1 externally through a PCB trace.
E1	VOUT1	Power supply output. Connect a 1μF ceramic decoupling capacitor between this pin and SGND.
E2	OCS	Low-side MOSFET gate driver output and OC set pin. Resistor between this pin and ground is used to set the overcurrent threshold. Inside the module, a 26.1k resistor is connected between this pin and SGND. An external resistor in parallel with the internal 26.1k resistor can be used to reduce the overcurrent threshold. Refer to “Overcurrent Protection” on page 26 for more details.
E3	VCC	5V internal linear regulator output. This output supplies bias for the IC, the low-side gate driver and the internal boot circuitry for the high-side gate driver. Decouple with a 10μF ceramic capacitor placed close to the pin to power ground. Do not allow the voltage at VCC to exceed VIN at any time.
C8	NC	No connection pin. Do not connect these pins.
D8	NC	

Table 1. ISL8215M Design Guide Matrix (Refer to [Figures 3 Through 6](#))

Case	V _{IN} (V)	V _{OUT} (V)	R2 (kΩ)	C _{IN} (Bulk) (μF)	C _{IN} (Ceramic) (μF)	C _{OUT} (Bulk) (μF)	C _{OUT} (Ceramic) (μF)	Freq (kHz)	RT Config	ROCSET (kΩ)	C ₇ (pF)	R5 (Package) (Note 4)
1	12	0.8	130	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0402
2	12	0.9	86.6	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0402
3	12	1	64.9	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0402
4	12	1.2	43.2	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0402
5	12	1.8	21.5	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0402
6	12	2.5	13.7	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0402
7	12	3.3	9.65	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0402
8	12	5	5.90	1x100	4x10	1x330	4x100	300	SGND	205	Open	0402
9	24	0.9	86.6	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0603
10	24	1	64.9	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0603
11	24	1.2	43.2	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0603
12	24	1.8	21.5	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0603
13	24	2.5	13.7	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0603
14	24	3.3	9.65	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	0603
19	24	5	5.90	1x100	4x10	1x330	4x100	300	SGND	205	Open	0603
20	7 to 42	1.5	28.7	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	1206
21	7 to 42	1.8	21.5	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	1206
22	7 to 42	2.5	13.7	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	1206
23	7 to 42	3.3	9.65	1x100	4x10	1x470	4x100	300	SGND	DNP	Open	1206
24	7 to 42	5	5.90	1x100	4x10	1x330	4x100	300	SGND	205	Open	1206
27	16 to 42	12	2.26	1x100	4x10	2x150	12x22	600	Open	118	100	1210

Note:

- Refer to ["Layout Considerations" on page 28](#) for more details about package selection size for R5.

Table 2. Recommended Input/Output Capacitor

Vendor	Value	Part Number
Murata, Output Ceramic	100μF, 10V, 1210	GRM32ER61A107ME20L
Murata, Output Ceramic	22μF, 16V, 1210	GRM32ER71C226KE18L
Murata, Input Ceramic	10μF, 50V, 1210	GRM32ER71H106KA12L
Panasonic, Output Bulk	470μF, 6.3V	6TPF470MAH
Panasonic, Output Bulk	330μF, 6.3V	6TPF330M9L
Panasonic, Output Bulk	150μF, 16V	16TQC150MYF
United Chemi-Con, Input Bulk	100μF, 50V	EMZA500ADA101MHA0G
Murata	270pF, 100V, X7R	GRM188R72A271KA01D

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VCC to SGND	-0.3	+5.9	V
VIN to PGND	-0.3	+45	V
VIN1 to PGND	-0.3	+45	V
EN, PGOOD, SS/TRK, FB, COMP to SGND	-0.3	$V_{CC} + 0.3$	V
VOUT to PGND	-0.3	16	V
VOUT1 to PGND	-0.3	16	V
RS to PGND	-0.3	16	V
UG1 to PHASE	-0.3	$V_{CC} + 0.3$	V
UG2 to PHASE	-20	+20	V
OCS to SGND	-0.3	$V_{CC} + 0.3$	V
RT, MOD/SYNC to SGND	-0.3	$V_{CC} + 0.3$	V
ESD Rating		Value	Unit
Human Body Model (Tested per JS-001-2014)		2	kV
Machine Model (Tested per JESD22-A115C)		200	V
Charged Device Model (Tested per JS-002-2014)		750	V
Latch-Up (Tested per JESD78E; Class II, Level A, +125°C)		100	mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
22 Ld HDA Package (Notes 5, 6)	11.7	1.9

Notes:

- θ_{JA} is measured in free air with the module mounted on a 4-layer thermal test board 4.5x3 inch in size with significant coverage of 2.8oz Cu on top and bottom and 2oz Cu on buried plane layers, with numerous vias.
- For θ_{JC} , the "case temp" location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	Refer to TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
V_{IN} to GND	7	42	V
Output Voltage, V_{OUT}	0.6	12	V
Junction Temperature Range, T_J	-40	+125	°C

2.4 Electrical Specifications

Unless otherwise noted, typical specifications are measured at $V_{IN} = 7V$ to $42V$, $V_{OUT} = 1.2V$, $C_{VCC} = 10\mu F$, $T_A = +25^\circ C$. **Boldface limits apply across the internal junction temperature range, $-40^\circ C$ to $+125^\circ C$.**

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
V_{IN} Supply						
Input Voltage Range	V_{IN}		7		42	V
Controller Input Current						
Shutdown Current (Note 7)	I_{VIN1Q}	EN = 0 PGOOD is floating $V_{IN1} = 12V$		5	10	μA
Operating Current (Note 8)	I_{VIN1OP}	PGOOD is floating $V_{IN1} = 12V$		2.5	4	mA
V_{CC} Supply (Note 7)						
Internal LDO Output Voltage	V_{CC}	$V_{IN} = 12V$, $I_L = 0mA$	4.85	5.10	5.40	V
		$V_{IN} > 7V$, $I_L = 75mA$	4.75	5.05		V
Maximum Supply Current of Internal LDO	I_{VCC_MAX}	$V_{VCC} = 0V$, $V_{IN} = 12V$		120		mA
Output Regulation						
Output Continuous Current Range	I_{OUT}		0		15	A
Output Voltage Range (Note 13)	V_{OUT_RANGE}		0.6		12.0	V
Output Voltage Set-Point Accuracy	V_{OUT_ACCY}	Total variation with line, load, and temperature ($-40^\circ C \leq T_J \leq +125^\circ C$)	-1.5		1.5	%
Line Regulation	$\Delta V_{OUT}/V_{OUT_SET}$	V_{IN} from 7V to 42V, $I_{OUT} = 0A$ to 15A		0.1		%
Load Regulation	$\Delta V_{OUT}/V_{OUT_SET}$	From 0A to 15A, $V_{IN} = 7V$ to 42V		0.3		%
Output Ripple Voltage	$V_{OUT(AC)}$	$V_{IN} = 24V$, $V_{OUT} = 1.2V$, $I_{OUT} = 15A$, 4x100 μF ceramic capacitor and 1x470 μF POSCAP		13		mV _{P-P}
Dynamic Characteristics						
Voltage Change of Positive Load Step	V_{OUT_DP}	Current slew rate = 2.5A/ μs , $V_{IN} = 24V$, 4x100 μF ceramic capacitor and 1x470 μF POSCAP $V_{OUT} = 1.2V$, $I_{OUT} = 0A$ to 7.5A		60		mV
Voltage Change of Negative Load Step	V_{OUT_DN}	Current slew rate = 2.5A/ μs , $V_{IN} = 24V$, 4x100 μF ceramic capacitor and 1x470 μF POSCAP $V_{OUT} = 1.2V$, $I_{OUT} = 7.5A$ to 0A		60		mV
Undervoltage Lockout						
Undervoltage Lockout, Rising	$V_{UVLOTHR}$	V_{IN} voltage, 0mA on V_{CC}	3.70	3.90	4.20	V
Undervoltage Lockout, Falling	$V_{UVLOTHF}$	V_{IN} voltage, 0mA on V_{CC}	3.35	3.50	3.85	V
EN Threshold						
EN Rise Threshold	V_{ENSS_THR}	$V_{IN} = 12V$	1.25	1.60	1.95	V
EN Fall Threshold	V_{ENSS_THF}	$V_{IN} = 12V$	1.05	1.25	1.55	V
EN Hysteresis	V_{ENSS_HYST}	$V_{IN} = 12V$	180	350	500	mV
Soft-Start Current						
SS/TRK Soft-Start Charge Current	I_{SS}	SS/TRK = 0V		2		μA
Default Internal Minimum Soft-starting						
Default Internal Output Ramping Time	t_{SS_MIN}	SS/TRK open		1.5		ms
Power-Good Monitors						

Unless otherwise noted, typical specifications are measured at $V_{IN} = 7V$ to $42V$, $V_{OUT} = 1.2V$, $C_{VCC} = 10\mu F$, $T_A = +25^\circ C$. **Boldface limits apply across the internal junction temperature range, $-40^\circ C$ to $+125^\circ C$.** (Continued)

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
PGOOD Upper Threshold	V_{PGOV}		109.0	112.5	115.0	%
PGOOD Lower Threshold	V_{PGUV}		85.0	87.5	92.0	%
PGOOD Low-Level Voltage	V_{PGLow}	$I_{SINK} = 2mA$			0.35	V
PGOOD Leakage Current	I_{PGLKG}	PGOOD = 5V		20	150	nA
PGOOD Timing						
V_{OUT} Rising Threshold to PGOOD Rising (Note 11)	t_{PGR}			1.1	5	ms
V_{OUT} Falling Threshold to PGOOD Falling	t_{PGF}			75		μs
Reference Section						
Internal Reference Voltage	V_{REF}			0.600		V
Reference Voltage Accuracy		$T_A = 0^\circ C$ to $+85^\circ C$	-0.75		+0.75	%
		$T_A = -40^\circ C$ to $+125^\circ C$	-1.00		+1.00	%
FB Bias Current	I_{FBLKG}		-40	0	40	nA
PWM Controller Error Amplifiers						
Input Common-Mode Range		$V_{IN} = 12V$	0		$V_{CC} - 2$	V
DC Gain		$V_{IN} = 12V$		88		dB
Gain-BW Product	GBW	$V_{IN} = 12V$		8		MHz
Slew Rate	SR	$V_{IN} = 12V$		2.0		V/ μs
COMP V_{OL}		$V_{IN} = 12V$		0.4		V
COMP V_{OH}		$V_{IN} = 12V$		2.6		V
COMP Sink Current (Note 12)		$V_{COMP} = 2.5V$			30	mA
COMP Source Current (Note 12)		$V_{COMP} = 2.5V$			30	mA
PWM Regulator						
Minimum Off-Time	t_{OFF_MIN}			308	412	ns
Minimum On-Time (Note 12)	t_{ON_MIN}			40	60	ns
Peak-to-Peak Sawtooth Amplitude	DV_{RAMP}	$V_{IN} = 20V$		1.0		V
		$V_{IN} = 12V$		0.6		V
Ramp Offset				1.0		V
Switching Frequency						
Switching Frequency	f_{SW}	RT PIN connect to SGND	250	300	350	kHz
Switching Frequency		RT PIN connect to VCC or FLOAT	515	600	645	kHz
Switching Frequency		$R_T = 36k\Omega$	890	1050	1195	kHz
Switching Frequency		$R_T = 16.5k\Omega$	1650	2000	2375	kHz
R_T Voltage	V_{RT}	$R_T = 36k\Omega$		770		mV
Synchronization						
SYNC Synchronization Range (Note 12)	F_{SYNC}	$R_T = 0\Omega$	354		1000	kHz
Diode Emulation Mode Detection						
MOD/SYNC Threshold High (Note 12)	$V_{MODETHH}$		1.1	1.6	2.1	V
MOD/SYNC Hysteresis (Note 12)	$V_{MODEHYST}$			200		mV
Diode Emulation Phase Threshold (Note 10)	V_{CROSS}	$V_{IN} = 12V$		-3		mV
Overvoltage Protection						

Unless otherwise noted, typical specifications are measured at $V_{IN} = 7V$ to $42V$, $V_{OUT} = 1.2V$, $C_{VCC} = 10\mu F$, $T_A = +25^\circ C$. **Boldface limits apply across the internal junction temperature range, $-40^\circ C$ to $+125^\circ C$.** (Continued)

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
OVP Threshold	V_{OVTH}		116	121	127	%
Overcurrent Protection						
OCP Threshold (Note 14)	I_{OCTH}	R_{OCSET} resistor open, at $+125^\circ C$ junction		19.4		A
Over-Temperature						
Over-Temperature Shutdown (Controller Junction Temperature)	T_{OT-TH}			150		$^\circ C$
Over-Temperature Hysteresis	T_{OT-HYS}			15		$^\circ C$

Notes:

7. In normal operation, where the device is supplied with voltage on the VIN pin, the VCC pin provides a 5V output capable of sourcing 75mA (minimum). This is the total shutdown current with $V_{IN} = 7V$ and $42V$.
8. Operating current is the supply current consumed when the device is active but not switching. It does not include gate drive current.
9. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested. Controller is independently tested prior to module assembly.
10. Threshold voltage at PHASE pin for turning off the bottom MOSFET during DEM.
11. When soft-start time is less than 4.5ms, t_{PGR} increases. With internal soft-start (the fastest soft-start time), t_{PGR} increases close to its maximum limit 5ms.
12. Compliance to limits is assured by characterization and design.
13. Maximum limit 100% production tested up to 5V.
14. $V_{IN} = 24V$, $V_{OUT} = 3.3V$ at $125^\circ C$ junction.

3. Typical Performance Curves

3.1 Efficiency Performance

Operating condition: $T_A = +25^\circ\text{C}$, no air flow. Device in PWM mode. Typical values are used unless otherwise noted.

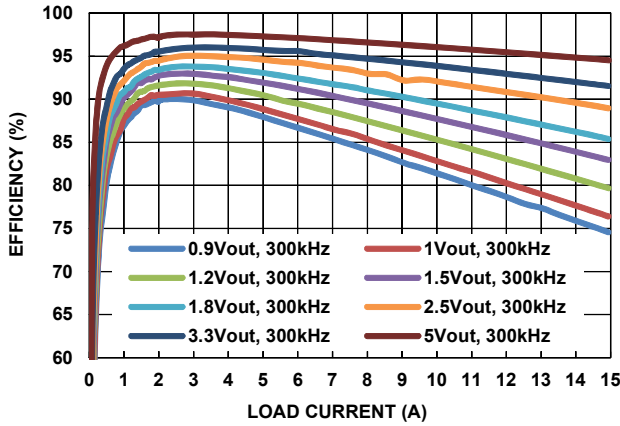


Figure 8. $V_{IN} = 7\text{V}$

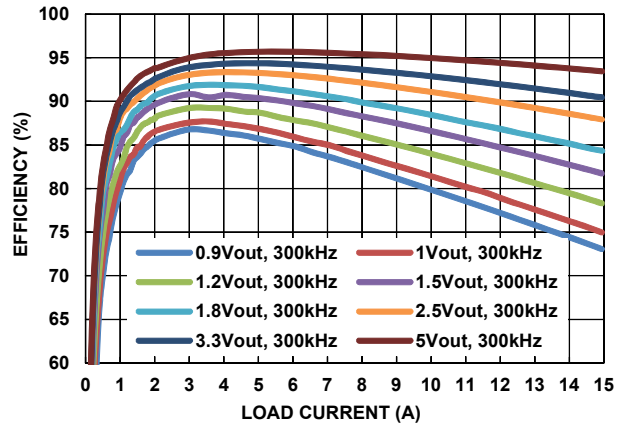


Figure 9. $V_{IN} = 12\text{V}$

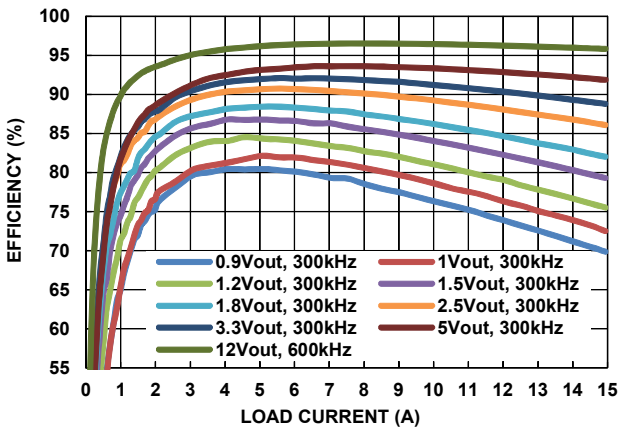


Figure 10. $V_{IN} = 24\text{V}$

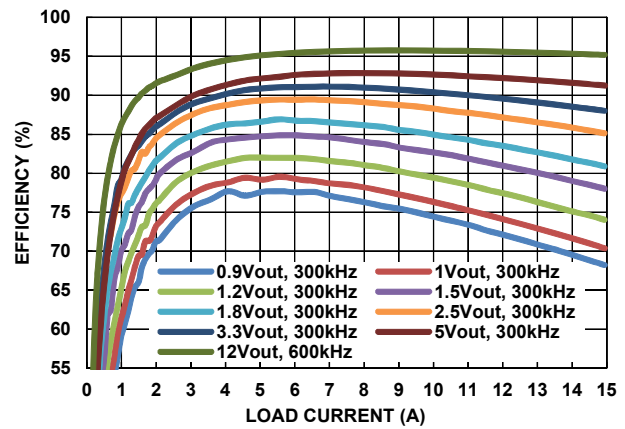


Figure 11. $V_{IN} = 30\text{V}$

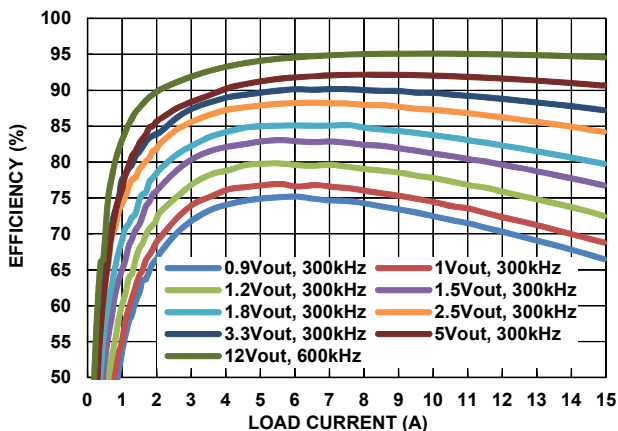


Figure 12. $V_{IN} = 36\text{V}$

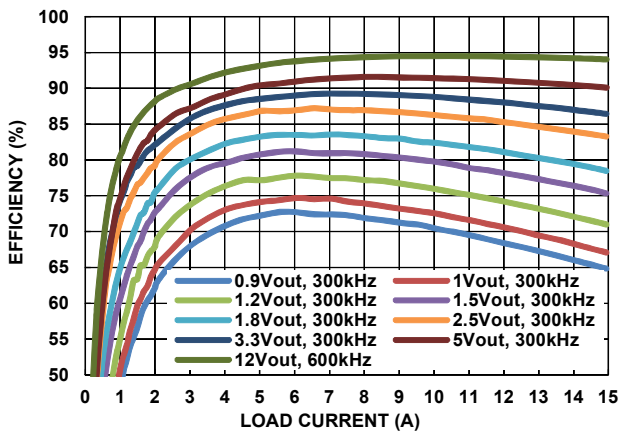


Figure 13. $V_{IN} = 42\text{V}$

3.2 Output Voltage Ripple

Operating condition: $T_A = +25^\circ\text{C}$, no air flow. $V_{IN} = 24\text{V}$, CCM mode. Typical values are used unless otherwise noted.

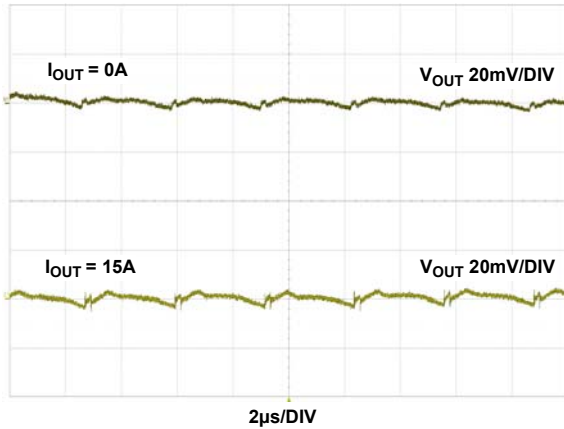


Figure 14. Output Ripple, $V_{OUT} = 1.2\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F}$ Ceramic + $1 \times 470\mu\text{F}$ POSCAP

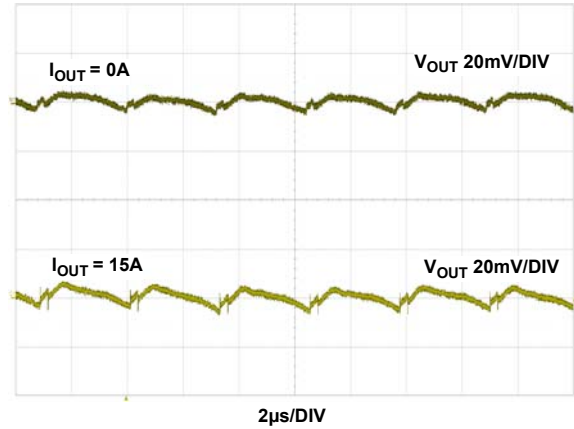


Figure 15. Output Ripple, $V_{OUT} = 1.8\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F}$ Ceramic + $1 \times 470\mu\text{F}$ POSCAP

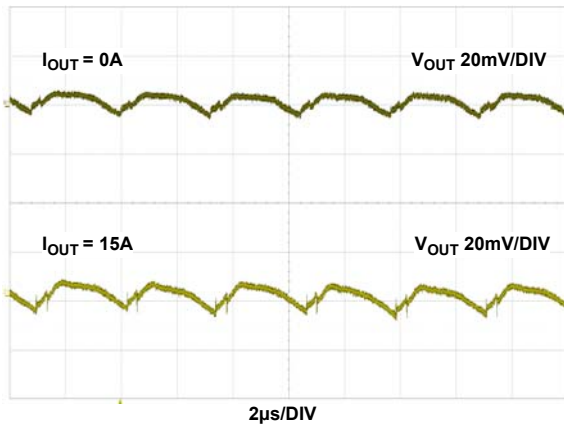


Figure 16. Output Ripple, $V_{OUT} = 2.5\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F}$ Ceramic + $1 \times 470\mu\text{F}$ POSCAP

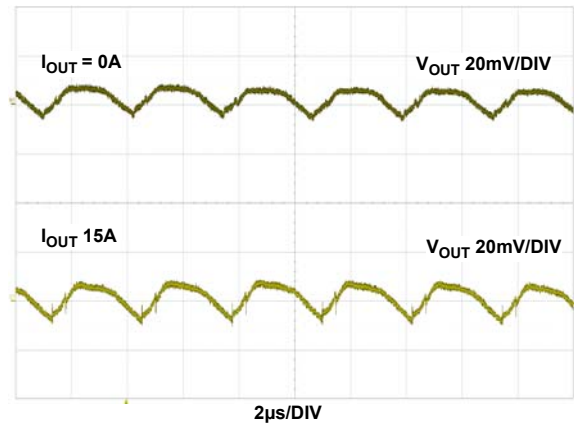


Figure 17. Output Ripple, $V_{OUT} = 3.3\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F}$ Ceramic + $1 \times 470\mu\text{F}$ POSCAP

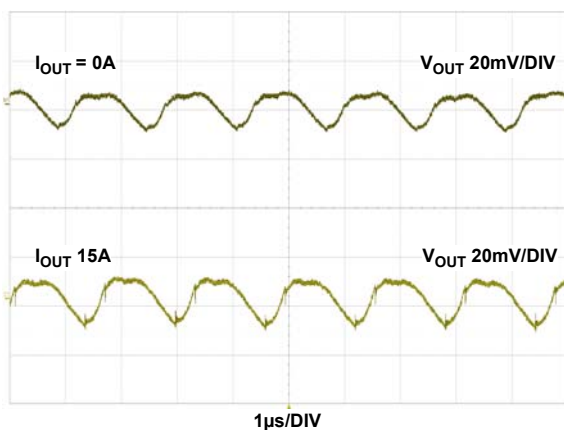


Figure 18. Output Ripple, $V_{OUT} = 5\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F}$ Ceramic + $1 \times 330\mu\text{F}$ POSCAP

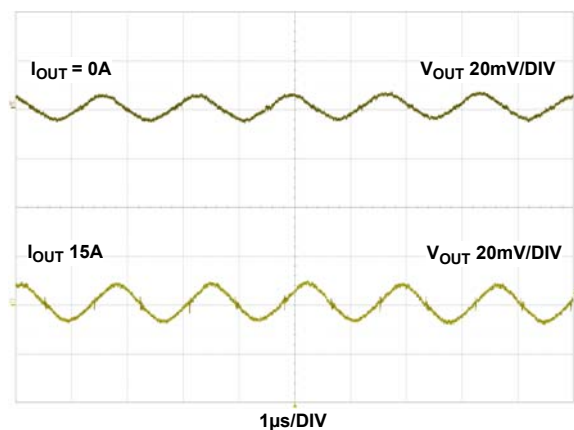


Figure 19. Output Ripple, $V_{OUT} = 12\text{V}$, $f_{SW} = 600\text{kHz}$, $C_{OUT} = 12 \times 22\mu\text{F}$ Ceramic + $2 \times 150\mu\text{F}$ POSCAP

3.3 Load Transient Response Performance

Operating condition: $T_A = +25^\circ\text{C}$, no air flow. $V_{IN} = 24\text{V}$, CCM mode, 0A - 7.5A, 2.5A/ μs step load. Typical values are used unless otherwise noted.

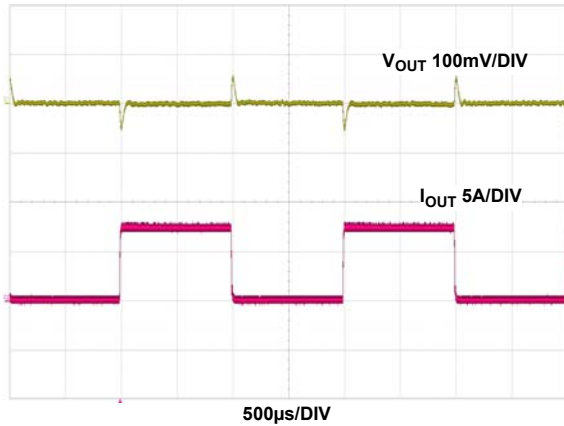


Figure 20. $V_{OUT} = 1.2\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F}$ Ceramic + 1x470 μF POSCAP

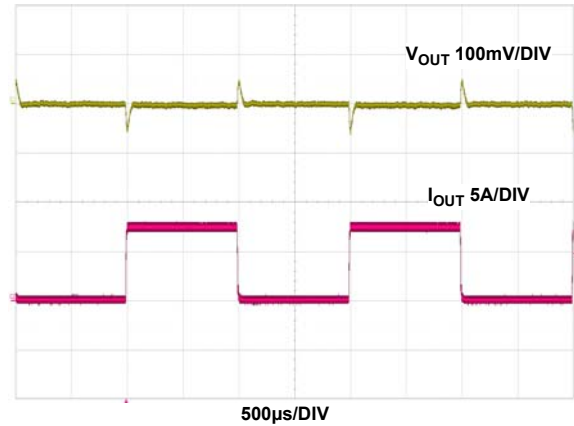


Figure 21. $V_{OUT} = 1.8\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F}$ Ceramic + 1x470 μF POSCAP

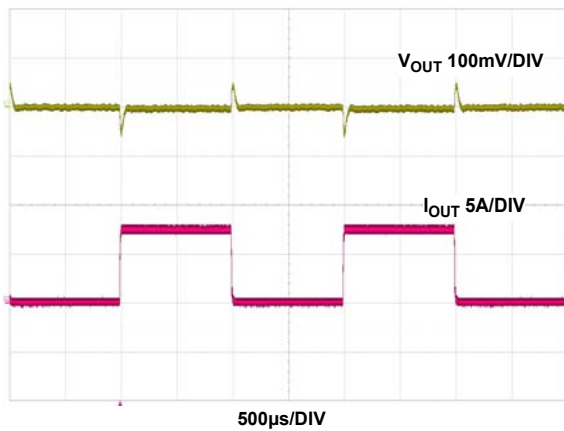


Figure 22. $V_{OUT} = 2.5\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F}$ Ceramic + 1x470 μF POSCAP

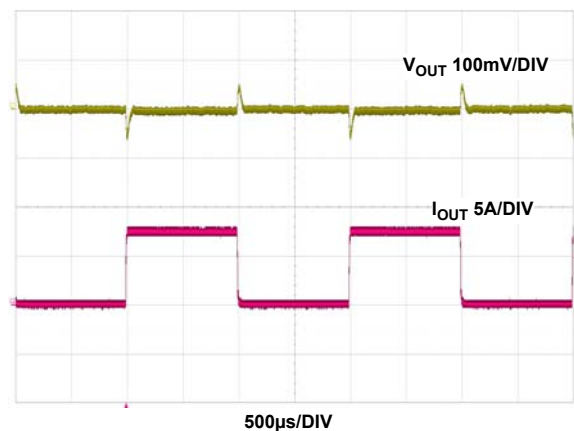


Figure 23. $V_{OUT} = 3.3\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F}$ Ceramic + 1x470 μF POSCAP

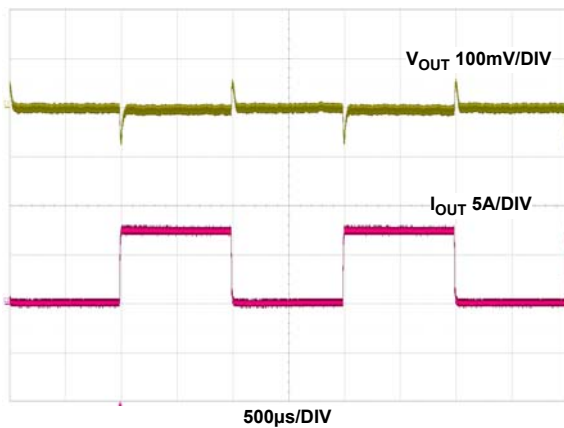


Figure 24. $V_{OUT} = 5\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F}$ Ceramic + 1x330 μF POSCAP

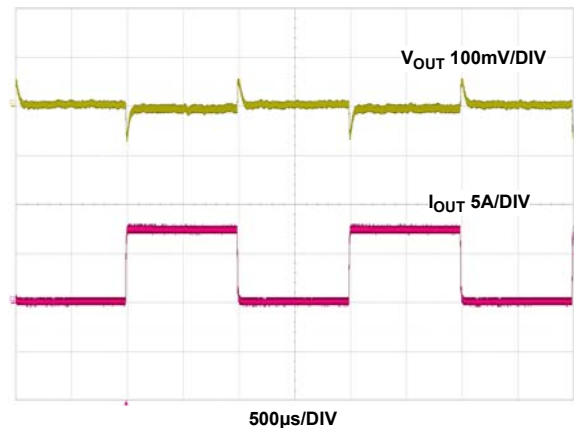


Figure 25. $V_{OUT} = 12\text{V}$, $f_{SW} = 600\text{kHz}$, $C_{OUT} = 12 \times 22\mu\text{F}$ Ceramic + 2x150 μF POSCAP

3.4 Start-Up Waveforms

Operating condition: $T_A = +25^\circ\text{C}$, no air flow. $V_{IN} = 24\text{V}$, $f_{SW} = 300\text{kHz}$, $C_{OUT} = 4 \times 100\mu\text{F CERAMIC} + 1 \times 330\mu\text{F POSCAP}$, CCM mode. Typical values are used unless otherwise noted.

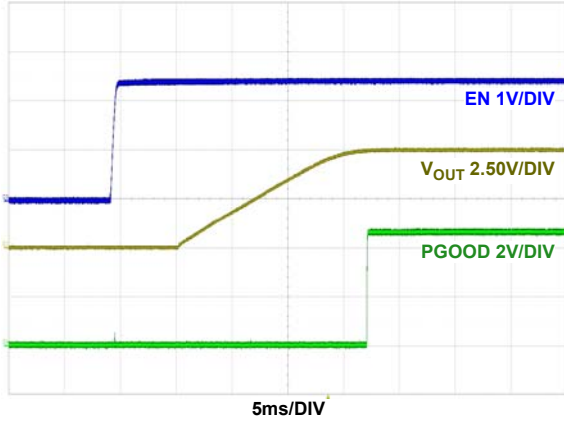


Figure 26. Start-Up Waveforms; $V_{OUT} = 5\text{V}$, $I_{OUT} = 0\text{A}$,

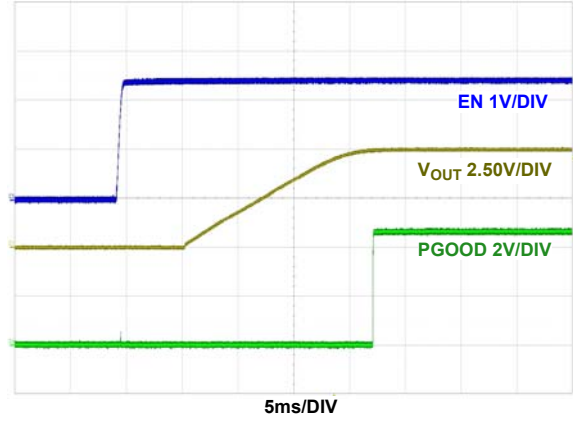


Figure 27. Start-Up Waveforms; $V_{OUT} = 5\text{V}$, $I_{OUT} = 15\text{A}$

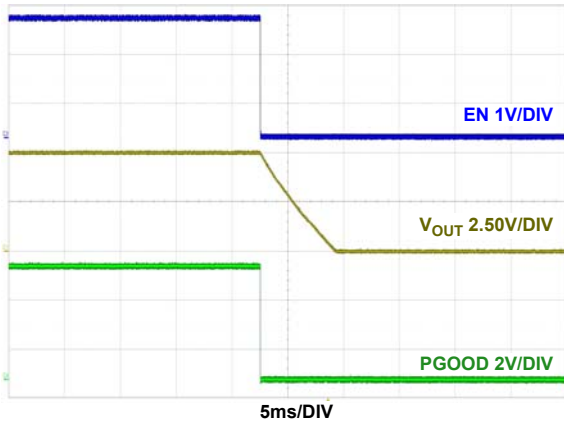


Figure 28. Shutdown Waveforms; $V_{OUT} = 5\text{V}$, $I_{OUT} = 0.5\text{A}$

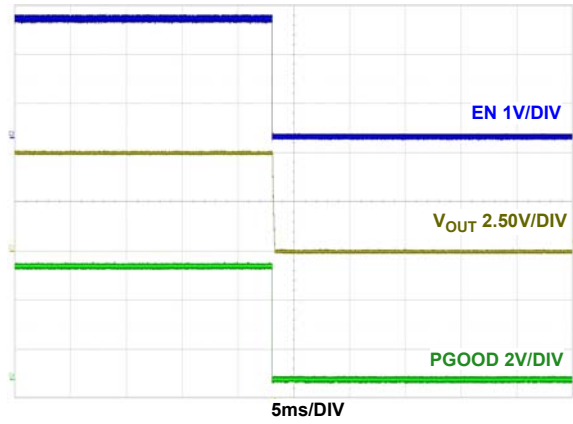


Figure 29. Shutdown Waveforms; $V_{OUT} = 5\text{V}$, $I_{OUT} = 15\text{A}$

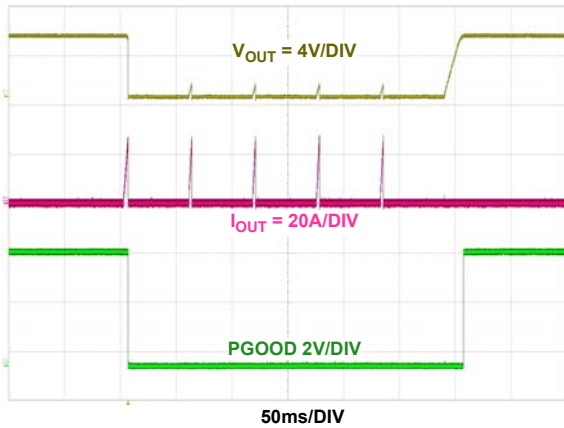


Figure 30. OCP Response; Output Short-Circuited from No Load to Ground and Released, $V_{OUT} = 5\text{V}$, $I_{OUT} = 0\text{A}$

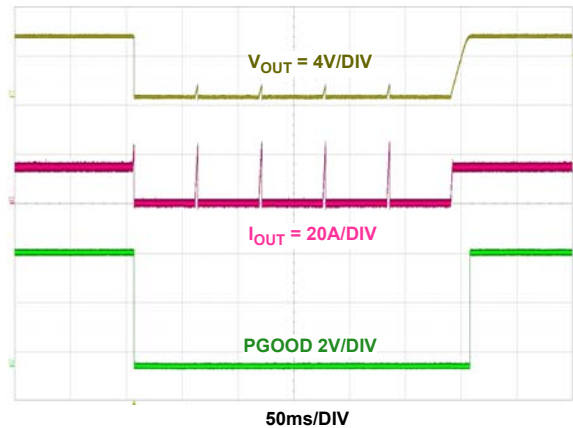


Figure 31. OCP Response; Output Short-Circuited from 15A to Ground and Released, $V_{OUT} = 5\text{V}$, $I_{OUT} = 15\text{A}$

3.5 Derating

Operating condition: $V_{IN} = 24V$. All of the following curves were plotted at $T_J = +120^{\circ}C$.

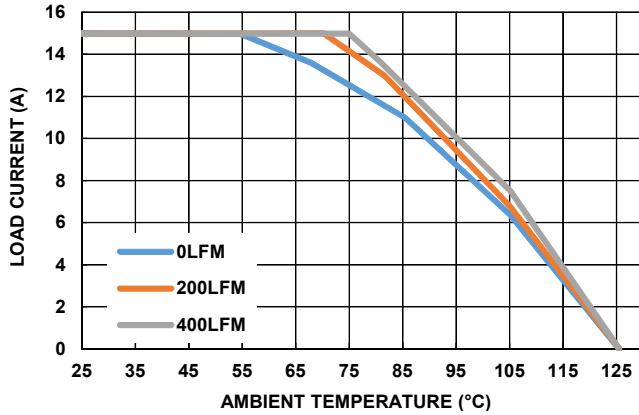


Figure 32. PWM/CCM Mode, $V_{OUT} = 1.2V$, $f_{SW} = 300kHz$

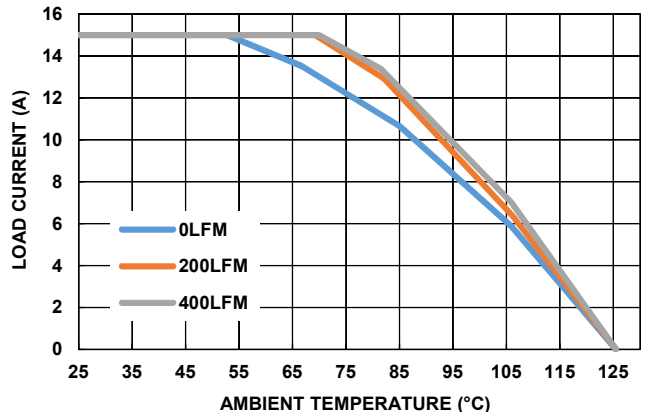


Figure 33. PWM/CCM Mode, $V_{OUT} = 1.8V$, $f_{SW} = 300kHz$

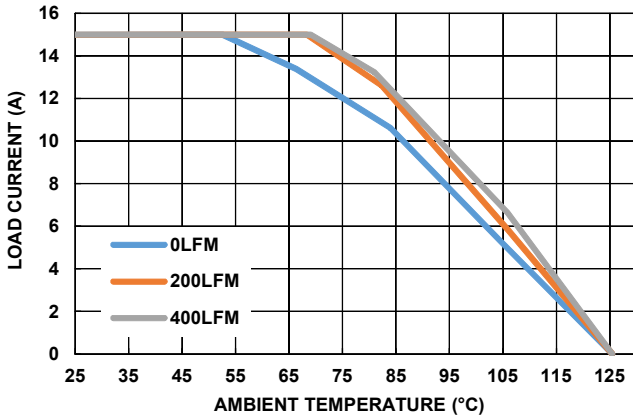


Figure 34. PWM/CCM Mode, $V_{OUT} = 2.5V$, $f_{SW} = 300kHz$

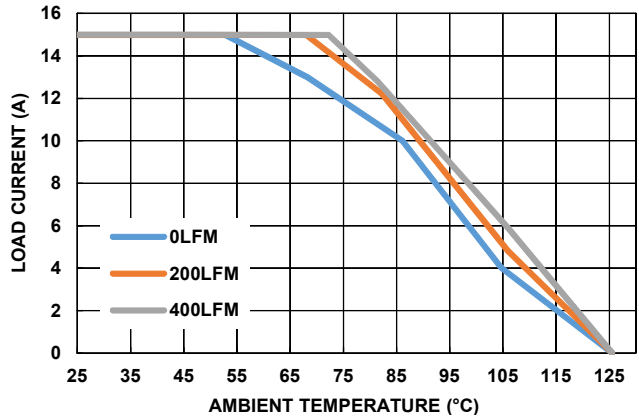


Figure 35. PWM/CCM Mode, $V_{OUT} = 3.3V$, $f_{SW} = 300kHz$

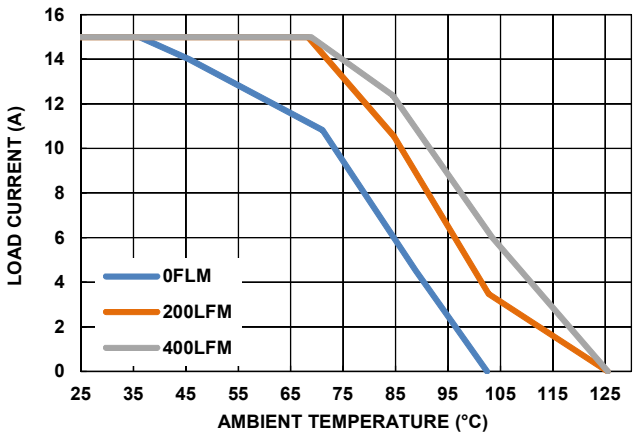


Figure 36. PWM/CCM Mode, $V_{OUT} = 5V$, $f_{SW} = 300kHz$

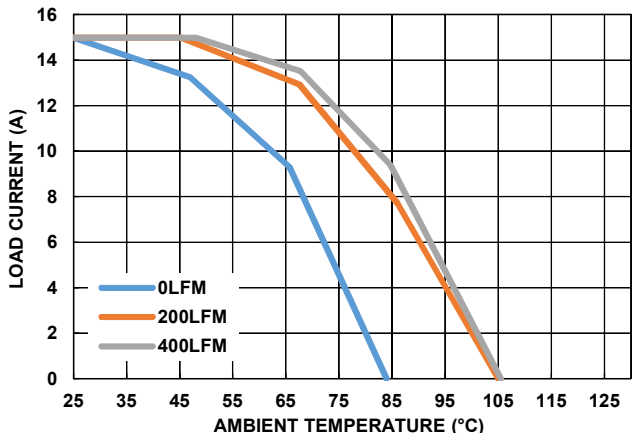


Figure 37. PWM/CCM Mode, $V_{OUT} = 12V$, $f_{SW} = 600kHz$

4. Functional Description

4.1 Power-Good Indicator

The power-good signal can be used to monitor the status of the output voltage for undervoltage and overvoltage conditions. This open-drain, PGOOD output is asserted whenever the output voltage is within $\pm 12.5\%$ of the selected target value. This voltage is measured through the feedback resistive divider hence referenced to the internal 0.6V reference. The PGOOD assertion occurs after a 1.1ms blanking delay upon the output voltage reaching the regulation window. PGOOD is deasserted without any delay when an output undervoltage or overvoltage is detected or when EN is pulled LOW.

4.2 Self-Enable Operation

An internal pull-up resistor from EN to VCC allows for self-enabling operation. Leaving the EN pin floating enables the ISL8215M as soon as VIN reaches the UVLO threshold, at which point the soft-start circuitry is activated.

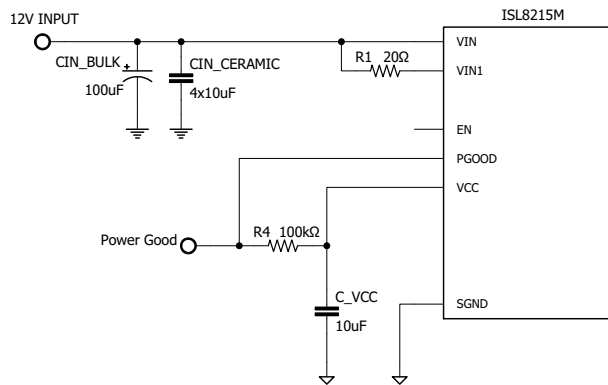


Figure 38. Self-Enable Operation

For operations in which the ISL8215M is required to turn on at a specific input voltage level, external circuitry must be implemented to control the voltage applied on the EN pin through a resistor divider. An optional zener (D1 as shown in [Figure 39](#)) may also be required to maintain the EN voltage within the recommended operating conditions.

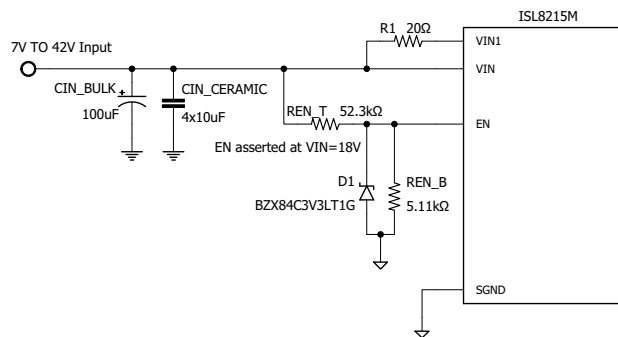


Figure 39. 18V_{IN} Minimum Self-Enable Operation

4.3 Enable

Driving the EN pin high or low respectively enables or disables operations of the ISL8215M. When the EN pin voltage reaches 1.6V, an initialization of the ISL8215M internal circuit is performed. Pulling the EN low disables all internal circuitry to achieve a low standby current and discharges the SS/TRK pin to GND by an internal MOSFET with 70Ω $r_{DS(ON)}$.

4.4 Prebiased Power-Up

The ISL8215M has the ability to soft-start with a prebiased output. The output voltage will not be pulled down during prebiased startup. PWM operations will initiate only when the soft-start ramp reaches the prebiased voltage times the resistive divider ratio. Overvoltage protection is active during soft-start operations.

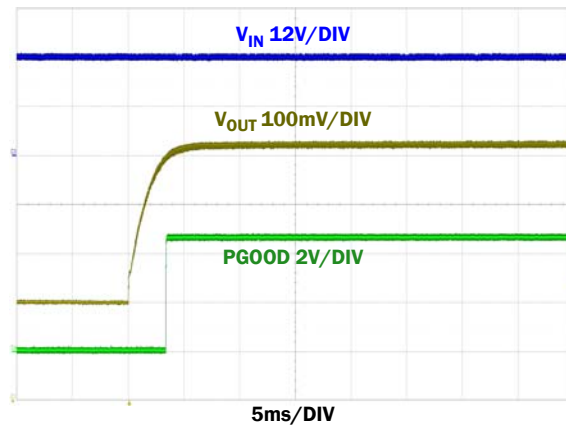


Figure 40. Prebiased Power-Up Waveform, Prebiased Voltage = 3.0V, V_{OUT} = 3.3V, I_{OUT} = No Load

4.5 PWM/CCM Mode

Tying the MOD/SYNC pin to signal ground or leaving it floating selects the PWM only mode of operation. In this mode, the ISL8215M operates at a constant frequency at all load currents. While this mode provides lower conversion efficiency at light current load, it may be sometimes required for applications sensitive to electromagnetic interferences.

4.6 PSM/DEM Light-Load Efficiency Mode

Tying the MOD/SYNC pin to VCC selects the PSM/DEM enhanced light-load efficiency mode of operation. In this mode, the ISL8215M operates in high-efficiency Diode Emulation Mode (DEM) and Pulse Skipping Mode (PSM) at light-load conditions. The inductor current is not allowed to reverse (discontinuous operation) while at very light loads, and the ISL8215M enters the pulse skipping function. Although this mode provides increased conversion efficiency at light load, it also increases the output ripple voltage and operates at a non-constant frequency.

4.7 Internal 5V Linear Regulator (V_{CC})

An internal low dropout regulator powers all ISL8215M internal circuitry allowing the device to operate from a single, wide-input voltage rail from 7V to 42V. For proper operation, the output of this internal LDO, V_{CC} , should be decoupled to power ground with a 10 μ F capacitor positioned as close as possible to the pin. No other circuitry should be connected to V_{CC} .

4.8 Gate Control Logic Optimization

The ISL8215M implements a specific proprietary MOSFET gates control logic that optimizes the performance over a wide range of operating conditions. This circuitry provides adaptive dead time control by monitoring the real gate waveforms of both the high-side and low-side MOSFETs. A shoot-through control logic provides a 16ns dead time to ensure that both the upper and lower MOSFETs will not turn on simultaneously and cause a shoot-through condition.

5. Application Information

5.1 Output Voltage Programming

The ISL8215M supports an adjustable output voltage range of 0.6V to 12V. A single resistor, R_2 , placed from FB to SGND sets the output voltage according to [\(EQ. 1\)](#).

$$(EQ. 1) \quad R_2 = \frac{(R_1 \times 0.6)}{(V_{OUT} - 0.6)}$$

where R_1 = Fixed high-side resistor value of $43.2k\Omega \pm 1\%$ tolerance inside the module and R_2 = Resistor connected from FB to SGND in $k\Omega$.

[Table 3](#) assists in selecting the value of resistor R_2 for typical output voltages. For maximum output voltage accuracy, R_2 should be selected with a tolerance of 0.1% or better.

Table 3. Output Voltage Resistor Settings

V_{OUT} (V)	R_2 E192 Series
0.6	Open
0.8	130k Ω
0.85	104k Ω
0.90	86.6k Ω
0.95	74.1k Ω
1.0	64.9k Ω
1.1	51.7k Ω
1.2	43.2k Ω
1.5	28.7k Ω
1.8	21.5k Ω
2.5	13.7k Ω
3.3	9.53k Ω
5	5.90k Ω
12	2.26k Ω

5.2 Switching Frequency Selection

The switching frequency of the ISL8215M is programmable from 300kHz to 2MHz typical and is set by a resistor connected from the RT pin to SGND according to [\(EQ. 2\)](#):

$$(EQ. 2) \quad R_T = \left(\frac{39.2}{f_{SW}} - 1.96 \right) k\Omega$$

where f_{SW} is the switching frequency in MHz.

The switching frequency can be set to 300kHz when the RT pin is tied to ground. The switching frequency can be increased to 600kHz if the RT pin is tied to VCC or left floating. Switching frequency selection is a trade-off between efficiency, output voltage ripple, and load transient response requirements. Typically, a low switching frequency improves efficiency by reducing MOSFET switching losses while a high switching frequency improves the output voltage ripple and transient response in conjunction with the value and type of the output capacitance. The frequency setting curve shown in [Figure 41](#) assists in selecting the correct value for the resistor R_T .

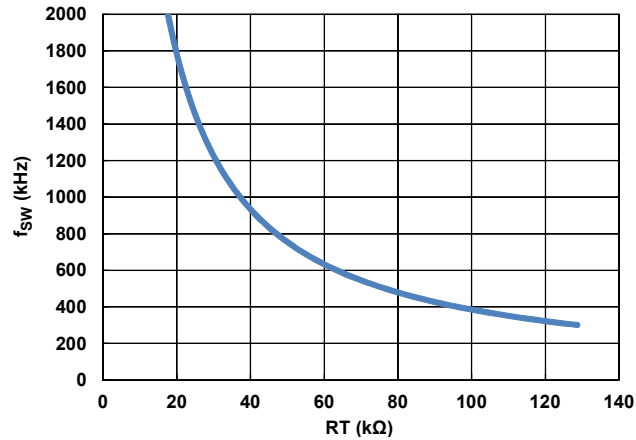


Figure 41. R_T vs Switching Frequency f_{SW}

When using the ISL8215M internal oscillator to control switching operations, the desired control scheme must be configured. In this mode, the MOD/SYNC pin selects the required configuration.

5.3 External Frequency Synchronization

The ISL8215M can be synchronized to an external clock applied on the MOD/SYNC pin. The external clock should be a square pulse waveform with a frequency in the range of 354kHz - 1MHz. The programmed frequency of the ISL8215M module, which is set by the resistor connected to the RT pin should be lower than the external clock frequency. The duty cycle of the external clock should be within 30% to 70% (typically 50%), while the amplitude should be in the range of 3V to 5V.

To ensure proper operation, the external clock frequency must be at least 18% higher than the programmed default frequency of the module. The module should be disabled before turning off the external clock. When frequency synchronization is in effect, the ISL8215M operates in forced PWM mode across all loads.

5.4 Soft-Start Operation

The ISL8215M provides soft-start operations for applications where inrush current during startup need be reduced.

A soft-start capacitor placed between the SS/TRK pin and signal ground adjusts the soft-start output voltage ramp rate. The typical soft-start time is based on the soft-start capacitor value and set according to [\(EQ. 3\)](#):

$$(EQ. 3) \quad t_{SS} = 0.6V \left(\frac{C_{SS}}{2} \right)$$

where C_{SS} is in nF and t_{SS} in ms.

The soft-start time setting curve shown in [Figure 42](#) assists in selecting the correct value for the capacitor C_{SS}. When the soft-start time set by external C_{SS} or tracking is less than 1.5ms, an internal soft-start circuitry of 1.5ms will take over the soft-start function. Furthermore, overvoltage protection is active during soft-starting operation.

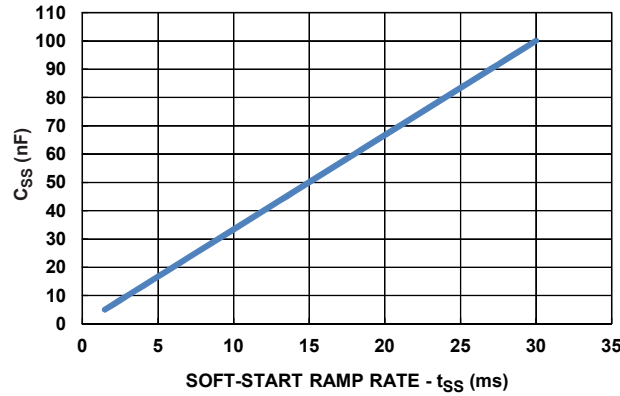


Figure 42. C_{SS} vs t_{SS}

5.5 Tracking Operation

The ISL8215M can be configured to track an external supply, either coincidentally or ratiometrically. To implement this functionality, a tracking resistor divider is connected between the external supply output (Master rail) and ground. The center point of this resistor divider is connected to the SS/TRK pin of ISL8215M.

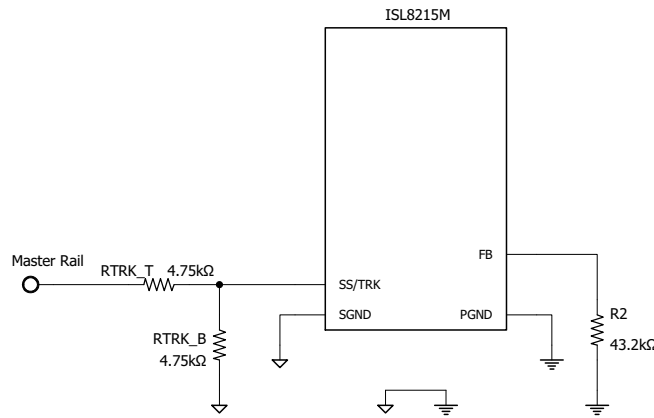


Figure 43. ISL8215M V_{OUT} = 1.2V - Coincidental Tracking of Master Rail - Divider Ratio of 1:1

Coincident tracking is achieved when both the master rail and ISL8215M output rail reach their respective regulation voltage levels with the same slope. As shown in Figure 44, the master rail and the ISL8215M output rail reach regulation at two different times. Coincidental tracking can be achieved by setting the external resistor divider ratio (RTRK_T/RTRK_B) equal to the feedback resistor divider ratio (R₁/R₂) of the ISL8215M. Table 3 on page 21 can assist in selecting the appropriate resistor value for different output voltages.

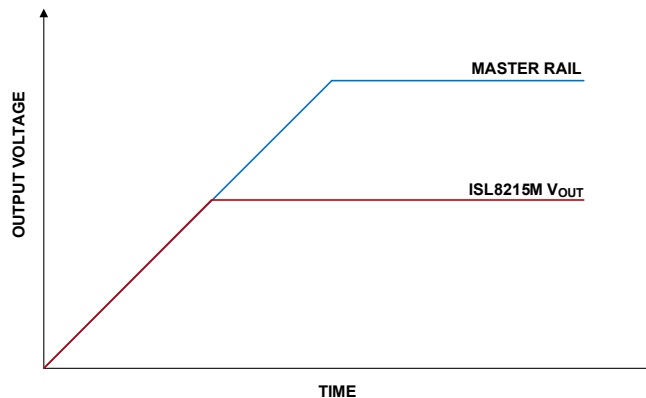


Figure 44. Coincidental Tracking of Master Rail

Ratiometric tracking is achieved when the master rail and the ISL8215M output rail both reach their final regulation value at the same time but with different slopes, as shown in [Figure 45](#). Use [\(EQ. 4\)](#) to calculate the resistor divider ratio (R_{TRK_T}/R_{TRK_B}) to implement ratiometric tracking.

$$(EQ. 4) \quad V_{\text{Master rail}} \times \frac{R_{TRK_B}}{R_{TRK_B} + R_{TRK_T}} = 0.6$$

Note that R1 is a fixed high-side resistor of value 43.2k Ω .

When the voltage at the SS/TRK pin reaches ~550mV, the output voltage is decided by the internal reference of the ISL8215M controller. In addition, the tracking resistor divider of the master rail should include resistors of values less than 10k Ω to minimize the impact of the 2 μ A soft-start current on the tracking function.

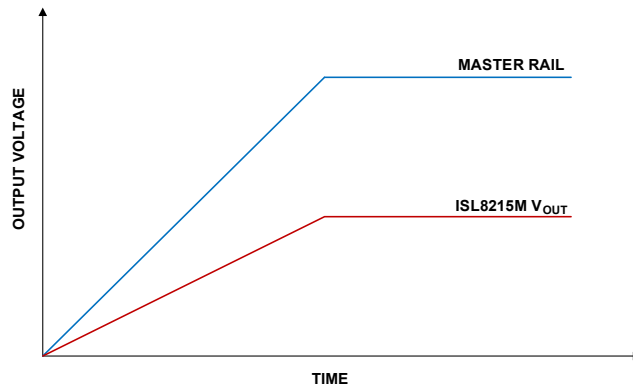


Figure 45. Ratiometric Tracking of Master Rail

5.6 Input Voltage Range

The ISL8215M is designed to operate from a single wide input supply ranging from 7V DC to 42V DC. Limitations on the minimum on-time and minimum off-time required by the ISL8215M limit the minimum and maximum conversion ratios, or duty cycles, supported. By extension, the supported input voltage range for a selected output voltage and selected operating frequency may be effectively reduced.

The maximum input voltage is limited by the minimum on-time ($t_{ON(min)}$) as shown in [\(EQ. 5\)](#).

$$(EQ. 5) \quad V_{IN(max)} \leq \left(\frac{V_{OUT}}{t_{ON(min)} \times f_{SW}} \right)$$

where $t_{ON(min)} = 60\text{ns}$ worst case and f_{SW} is the switching frequency in Hz.

The minimum input voltage is limited by the minimum off-time ($t_{OFF(min)}$), ON-resistance of the high-side FET, $r_{DS(ON)}$, series resistance of the inductor (R_L), and the load current (I_{OUT}) as shown in [\(EQ. 6\)](#). Because of the temperature coefficient of the MOSFET and inductor, note that the minimum value of V_{IN} will occur at the +125°C at $R_L = 9.7\text{m}\Omega$ and $r_{DS(ON)} = 18.75\text{m}\Omega$.

$$(EQ. 6) \quad V_{IN(min)} \geq \left(\frac{V_{OUT} + I_{OUT} \times (r_{DS(ON)} + R_L)}{1 - t_{OFF(min)} \times f_{SW}} \right)$$

where $t_{OFF(min)} = 412\text{ns}$ worst case.

5.7 Input Capacitor Selection

The important parameters for the input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline. The AC_{RMS} input current varies with the load given in [\(EQ. 7\)](#):

$$(EQ. 7) \quad I_{RMS} = \sqrt{D(1-D)} \cdot I_{OUT}$$

Where D is duty cycle of the PWM.

The maximum RMS current supplied by the input capacitance occurs at $V_{IN} = 2 \times V_{OUT}$, $D = 50\%$ as shown in [\(EQ. 8\)](#):

$$(EQ. 8) \quad I_{RMS} = \frac{1}{2} \cdot I_{OUT}$$

Refer to the capacitor vendor to check the RMS current rating. It should be noted that the current rating is decided by the ambient temperature or temperature rise. Each 1210 size 10 μ F low ESR capacitor is typically good for 2A to 3A RMS ripple current.

Use a mix of input bypass capacitors to control the voltage stress across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the MOSFETs to suppress the voltage induced in the parasitic circuit impedances.

Solid tantalum capacitors can be used, however, caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up.

5.8 Output Capacitor Selection

The ISL8215M is designed for low output voltage ripple. In general, output capacitors should be selected to meet the dynamic regulation requirements including ripple voltage and load transients, which can be met with bulk output capacitors that have adequately low ESR and ESL.

High frequency capacitors initially supply the transient current and slow the slew rate of load transient seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR and ESL and voltage rating requirements, as well as actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low ESR/ESL components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low ESR capacitors intended for switching regulator applications for the bulk capacitors. In most cases, multiple small case electrolytic capacitors perform better than a single large case capacitor.

In conclusion, the output capacitors must meet the following criteria:

- (1) They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.
- (2) The ESR must be sufficiently low to meet the desired output voltage ripple due to the output inductor current.

The recommended output capacitor value for the ISL8215M is between 400 μ F to 1000 μ F. See [Tables 1](#) and [2](#) on [page 9](#) for more capacitor information. All ceramic capacitors are possible with loop analysis to ensure stability.

6. Protection Circuits

6.1 Undervoltage Lockout

The ISL8215M includes UVLO protection, which keeps the device in a reset condition until a proper operating voltage is applied. It also shuts down the ISL8215M if the operating voltage drops below a predefined value. Upon assertion of the UVLO state, the controller is completely disabled. PGOOD is valid and will be deasserted.

6.2 Overcurrent Protection

The ISL8215M uses the lower MOSFET's ON-resistance, $r_{DS(ON)}$, to monitor the current in the converter. The sensed voltage drop across the MOSFET's drain-to-source is compared to a threshold voltage set by the resistor, R_{OCSET} , connected from the OCS pin to ground. Because $r_{DS(ON)}$ is higher at hot temperatures and lower at cold temperatures, the OCP setpoint at room and cold temperatures will be higher than the OCP setpoint at hot temperatures.

For applications involving less than 15A load, it is recommended to further reduce the OCP setpoint to improve the system reliability, and (EQ. 9) can be used to calculate the value of the OCP set resistor.

$$(EQ. 9) \quad R_{OCSET} = \frac{(26.1 \cdot R_{Nom} \cdot (I_O/15))}{(R_{Nom} \cdot (1 - (I_O/15)) + 26.1)} k\Omega$$

where,

I_O = Desired full load current (A).

R_{OCSET} = Resistor connected to the OCS pin (k Ω).

R_{Nom} = R_{OCSET} resistor to ensure 15A full load operation (k Ω).

R_{OCSET} values for ensuring 15A full load operation:

- 20M Ω for 3.3V output and below (simulating a “Do Not Populate” (DNP) condition).
- 205k Ω for 5V output
- 118k Ω for 12V output

In (EQ. 9) the typical load current to hit OCP at +120°C is set to around 20% higher than the desired full load current. The 20% margin is due to the controller OCP and the MOSFET $r_{DS(ON)}$ tolerance.

If an overcurrent is detected, the upper MOSFET remains off and the lower MOSFET remains on until the next cycle. As a result, the converter skips a pulse. When the overload condition is removed, the converter resumes normal operation. If an overcurrent is detected for two consecutive clock cycles, the module enters Hiccup mode by turning off the gate driver and entering soft-start. The ISL8215M stays off for 50ms before trying to restart and continues to cycle through soft-start until the overcurrent condition is removed. Hiccup mode is active during soft-start, so ensure that the peak inductor current does not exceed the overcurrent threshold during soft-start.

When OCP is triggered, the SS/TRK pin is pulled to ground by an internal MOSFET for hiccup restart. When configured to track another voltage rail, the SS/TRK pin rises up much faster than the internal minimum soft-start ramp. The voltage reference is then clamped to the internal minimum soft-start ramp. Thus, smooth soft-start hiccup is achieved even with the tracking function.

6.3 Overvoltage Protection

The overvoltage set point is set at 121% of the nominal output voltage set by the feedback resistors. In case of an overvoltage event, the module will attempt to bring the output voltage back into regulation by keeping the upper MOSFET turned off and the lower MOSFET turned on. If the overvoltage condition has been corrected and the output voltage returns to 110% of the nominal output voltage, both high-side and low-side MOSFETs will be turned off until the output voltage drops to the nominal voltage to start work in normal PWM switching.

6.4 Over-Temperature Protection

The IC incorporates an over-temperature protection circuit that shuts down the IC when a die temperature of +150°C is reached. Normal operation resumes when the die temperature drops below +145°C through the initiation of a full soft-start cycle. During OTP shutdown, the IC consumes only 100µA current. When the controller is disabled, thermal protection is inactive. This helps achieve a very low shutdown current of 5µA.

7. Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of an ISL8215M based DC/DC converter. The ISL8215M switches at a very high frequency and, therefore, the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. Also, the peak gate drive current rises significantly in an extremely short time. Transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device overvoltage stress and ringing. Careful component selection and proper PC board layout minimize the magnitude of these voltage spikes.

7.1 Layout Considerations

- (1) Place the input capacitors and high frequency decoupling ceramic capacitors between VIN and PGND, as close to the module as possible. The loop formed by the input capacitor, VIN pad, and PGND must be as small as possible to minimize the high frequency noise. The output capacitors should be placed close to the load. Use short, wide copper planes to connect the output capacitors to the load for avoiding any parasitic inductances and resistances. An illustrative layout example is shown in [Figures 46 and 47](#).
- (2) VIN, VOUT, and PGND should use large copper planes to minimize conduction loss and thermal stress. Use enough vias to connect the power planes in different layers.
- (3) Use full ground planes in the internal layers (underneath the module) with shared SGND and PGND to simplify the layout design. It is recommended to use slots, as shown in [Figure 48 on page 29](#) to ensure that the switching current avoids the SGND pad of the module. It is recommended to use as much GND plane as possible for the layer directly above the bottom layer (containing components like input caps, output caps, etc). Use the top and bottom layer to route EN, VCC, and PGOOD signals.
- (4) For a switching frequency of 300kHz and a 42V input, connect a 4.02Ω 1206 resistor and a 270pF 100V X7R 0603 capacitor in series from PH to VIN. De-rate the resistor size for switching frequencies higher than 300kHz. Calculate the power dissipated in resistor R5 (P_{cal}) by using the formula $C \cdot V^2 \cdot f$, where,
 - C = 270pF
 - V = Input voltage
 - f = Frequency of operation.
 For derating purposes, the nominal power handling capability of the resistor package size should be at least $P_{cal}/0.65$. The 65% derating is derived by looking at the resistor operation at +100°C ambient temperature. Use a standard thick film chip resistor datasheet to find the correct resistor package size for different switching frequencies and input voltage.
- (5) Make sure that UG1 and UG2 (D6 and K4) are connected externally through a PCB trace. A similar connection should be made for the two EN pins (A6 and A8). (Refer to the Pin Configuration on [page 7](#) and the Pin Description table on [page 8](#).)
- (6) Use a remote sensing trace to connect to the VOUT+ of load for achieving a tight output voltage regulation. Route the remote sense trace underneath the GND layer and avoid routing the sense lines near noisy planes such as PHASE node. Place a 2Ω resistor close to RS pin for damping the noise on the traces.
- (7) To avoid ground bouncing issues, place the V_{IN} return and the V_{OUT} return diagonally opposite to each other. This will also ensure that the switching noise generated by the power-train will have a minimal effect on the controller operation.
- (8) Do not unnecessarily oversize the copper islands for the PHASE node. Because the phase nodes are subjected to very high dv/dt voltages, the parasitic capacitor formed between these islands and the surrounding circuitry will tend to couple the switching noise. Caution must be taken to ensure that none of the sensitive signal traces are routed close to the PHASE node plane.
- (9) Place the VCC bypass capacitor underneath the VCC pin, and connect its ground to PGND pad. Connect the low side feedback resistor and the decoupling cap for VOUT1 to SGND pad.

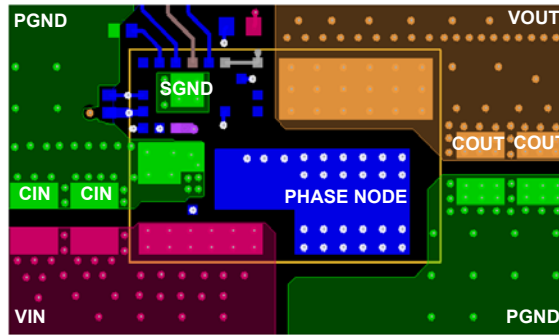


Figure 46. Layout Example - Top Layer

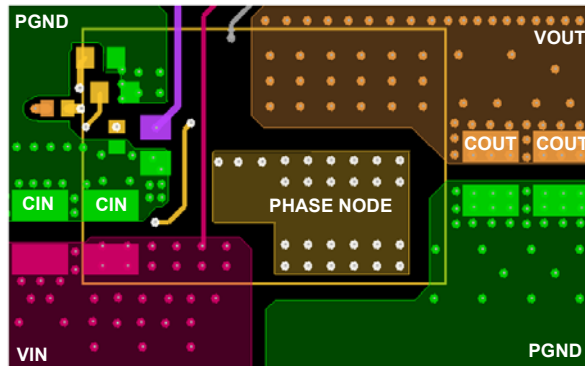


Figure 47. Layout Example - Bottom Layer

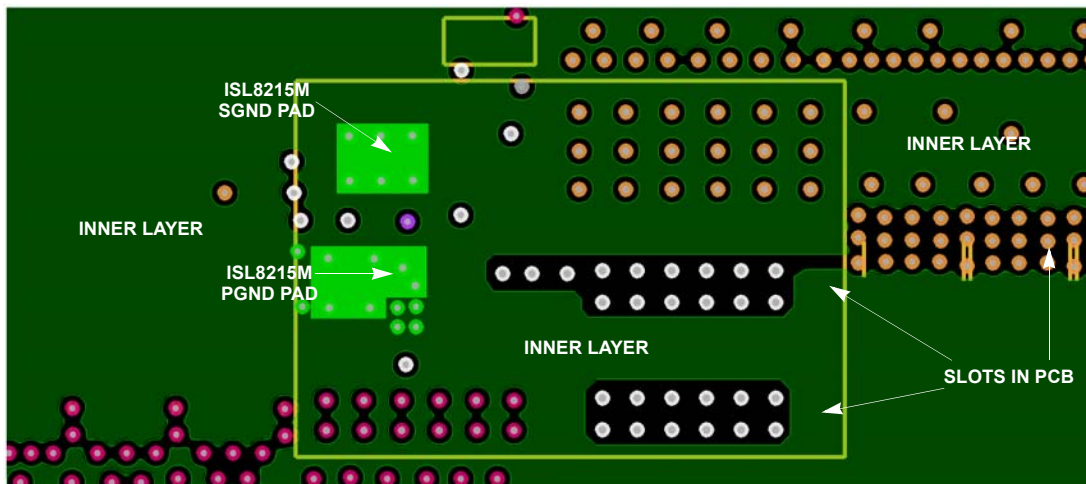


Figure 48. Layout Example - SGND is Connected to PGND Through Internal Layer

8. Thermal Considerations

Experimental power loss curves, along with θ_{JA} from thermal modeling analysis, can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining temperature below the maximum junction temperature of +120°C. In applications in which the system parameters and layout are different from the evaluation board, the customer can adjust the margin of safety. All derating curves are obtained from the tests on a 4-layer thermal test board 4.5x3 inches in size. Refer to [TB379](#) for more details. In the actual application, other heat sources and design margins should be considered.

9. Package Description

The structure of the ISL8215M belongs to the High Density Array No-lead package (HDA). This kind of package has advantages, such as good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The ISL8215M contains several types of devices, including resistors, capacitors, inductors, and control ICs. The ISL8215M is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multi-component assembly is overmolded with polymer mold compound to protect these devices.

The package outline, typical PCB layout pattern design, and typical stencil pattern design are shown in the [Package Outline Drawing](#) starting on [page 34](#). The module has a small size of 19mm x 13mm x 5.3mm.

9.1 PCB Layout Pattern Design

The bottom of the ISL8215M is a lead-frame footprint, which is attached to the PCB by a surface mounting process. The PCB layout pattern is shown on [page 37](#) and [page 38](#). The PCB layout pattern is an array of solder mask defined PCB lands that align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

9.2 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and your board design rules allow.

9.3 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2 mil to 3 mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. Stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown on [page 35](#) and [page 36](#). The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a “brick like” paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) HDA.

9.4 Reflow Parameters

Due to the low mount height of the HDA, “No Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in [Figure 49](#) is provided as a guideline, to be customized for varying manufacturing practices and applications.

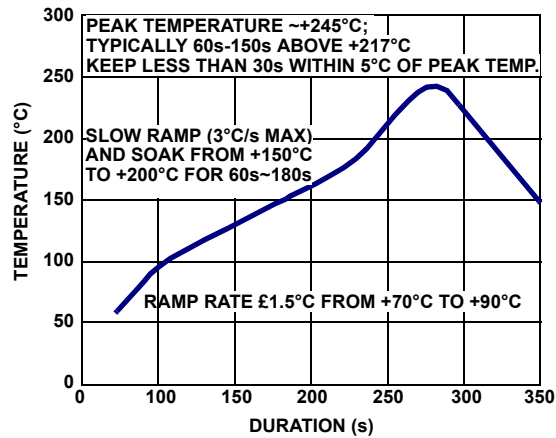


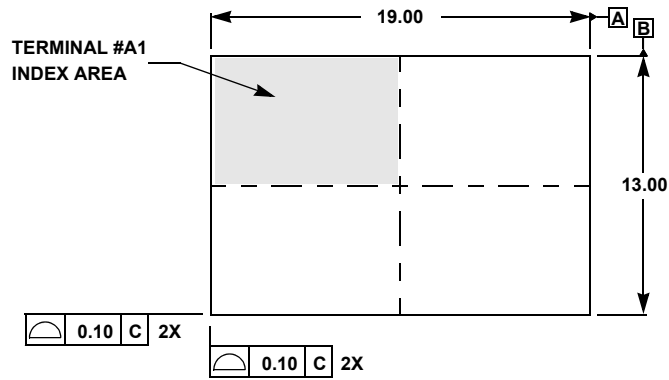
Figure 49. Typical Reflow Profile

10. Revision History

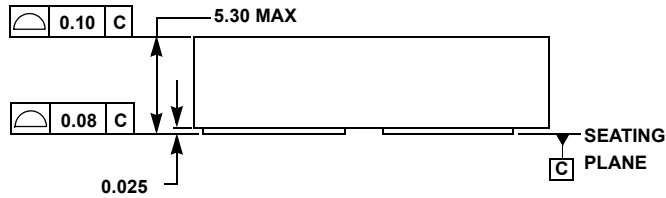
Rev.	Date	Description
1.00	Aug 30, 2017	Updated Figure 2 on page 1. Updated table in Section 1.5, Pin Descriptions. Added R5 (Package) column to Table 1 on page 9. Updated Over-Temperature Shutdown value on page 13. Updated requirements in Section 7.1, Layout Considerations.
0.00	Aug 1, 2017	Initial release

11. Package Outline Drawing

Y22.19x13
22 I/O 19mmx13mmx5.30mm HDA MODULE
Rev 1, 11/16



TOP VIEW

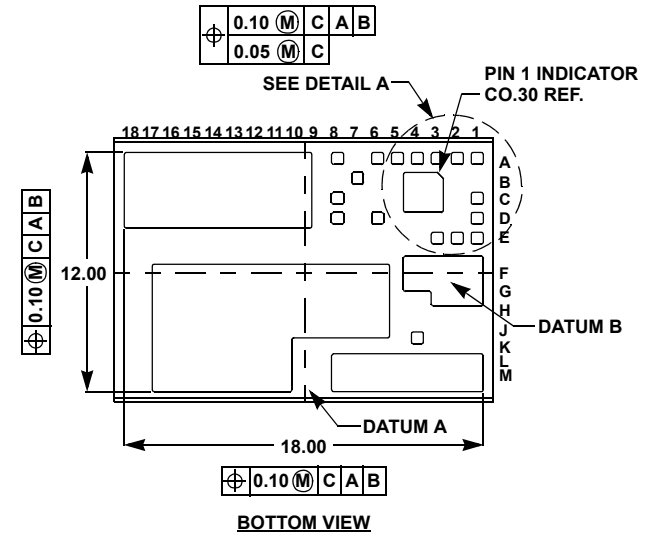


SIDE VIEW

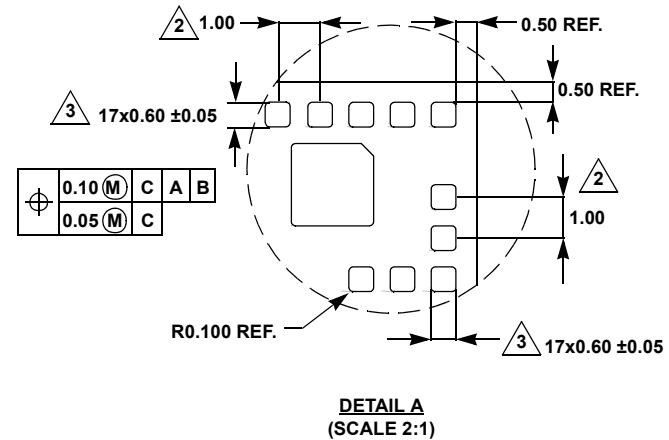
NOTES:

1. All dimensions are in millimeters.
2. Represents the basic land grid pitch.
3. These 17 I/Os are centered in a fixed row and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5-2009.
5. Tolerance for exposed PAD edge location dimension is ± 0.1 mm.

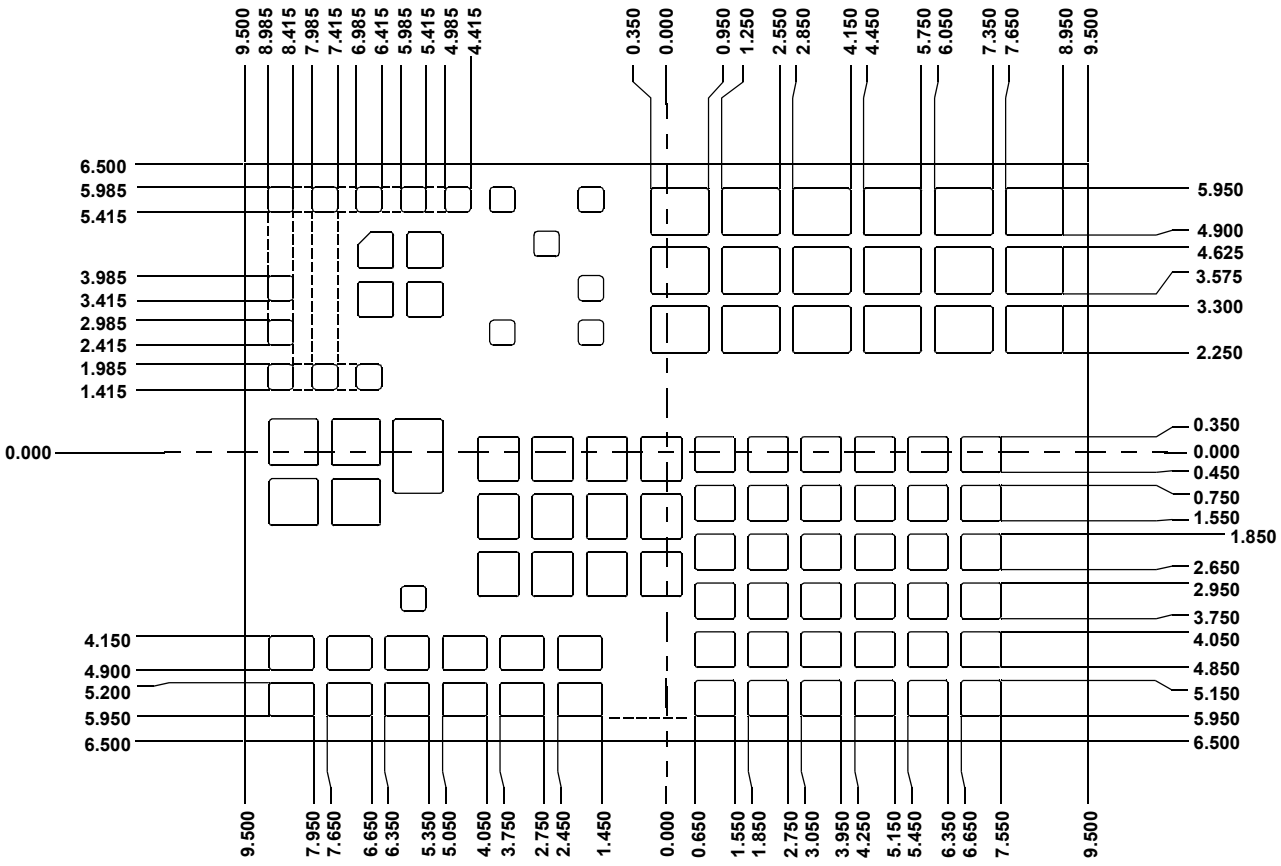
For the most recent package outline drawing, see [Y22.19x13](#).



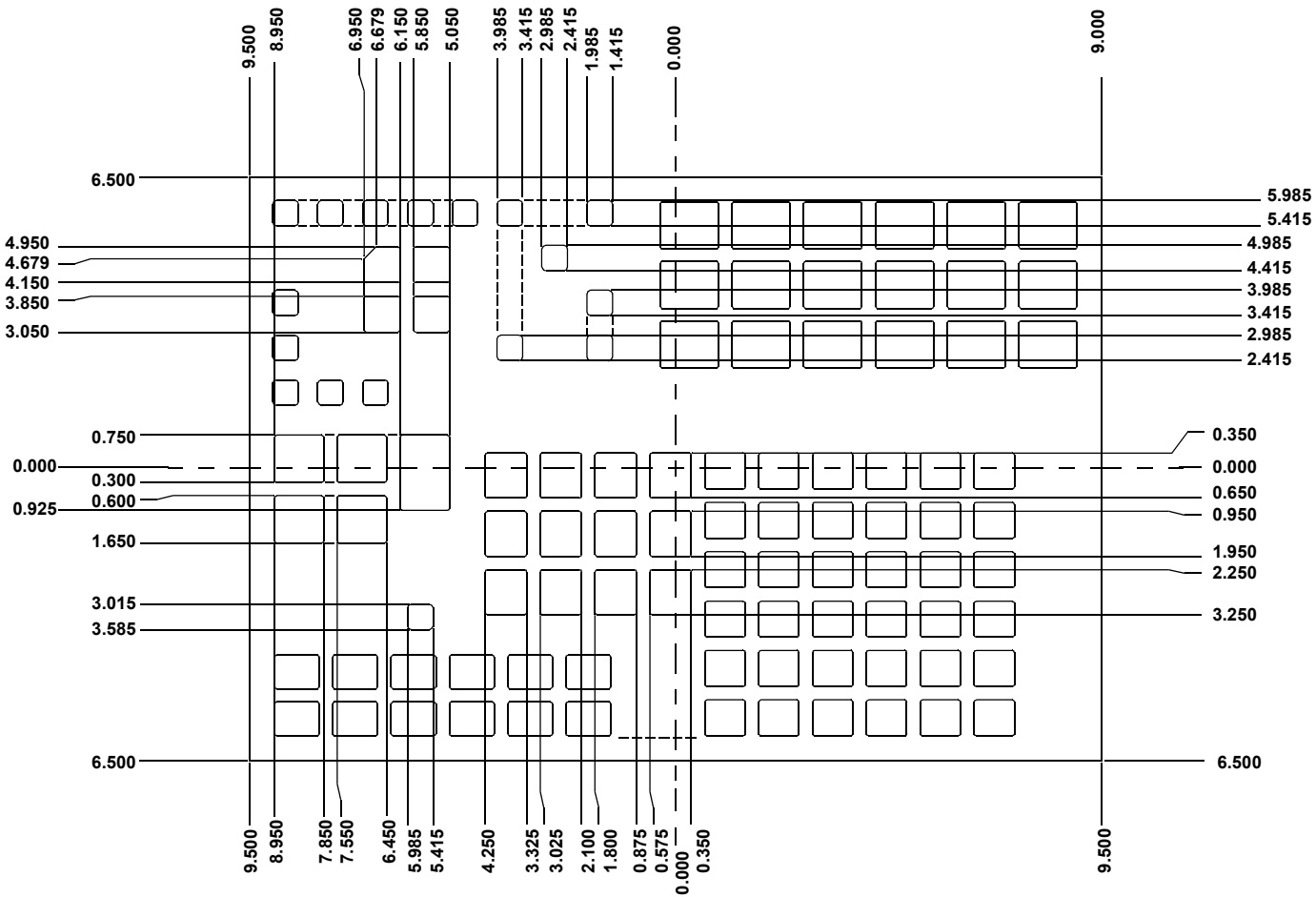
BOTTOM VIEW



DETAIL A
(SCALE 2:1)

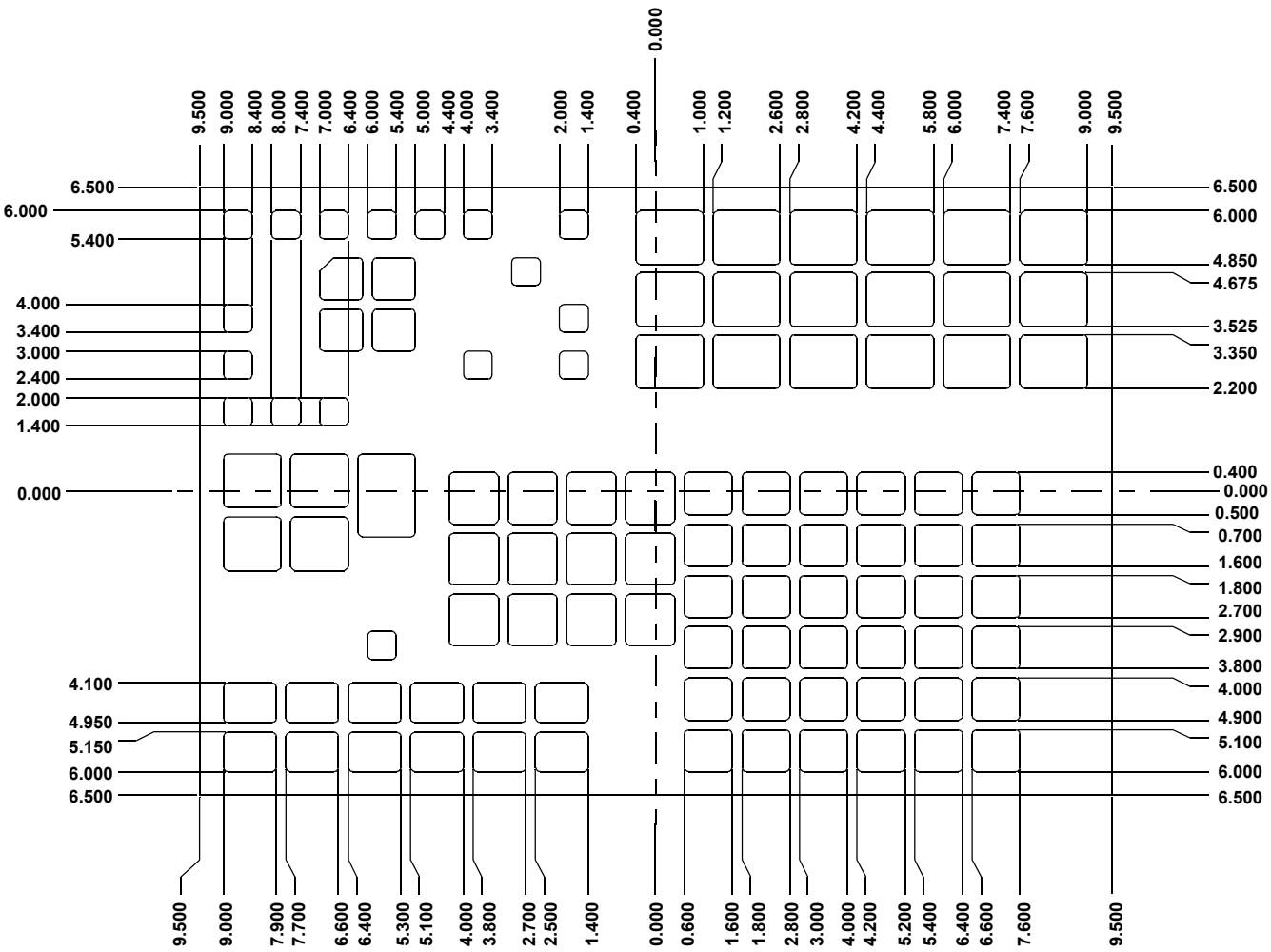


RECOMMENDED SOLDER STENCIL
TOP VIEW 1



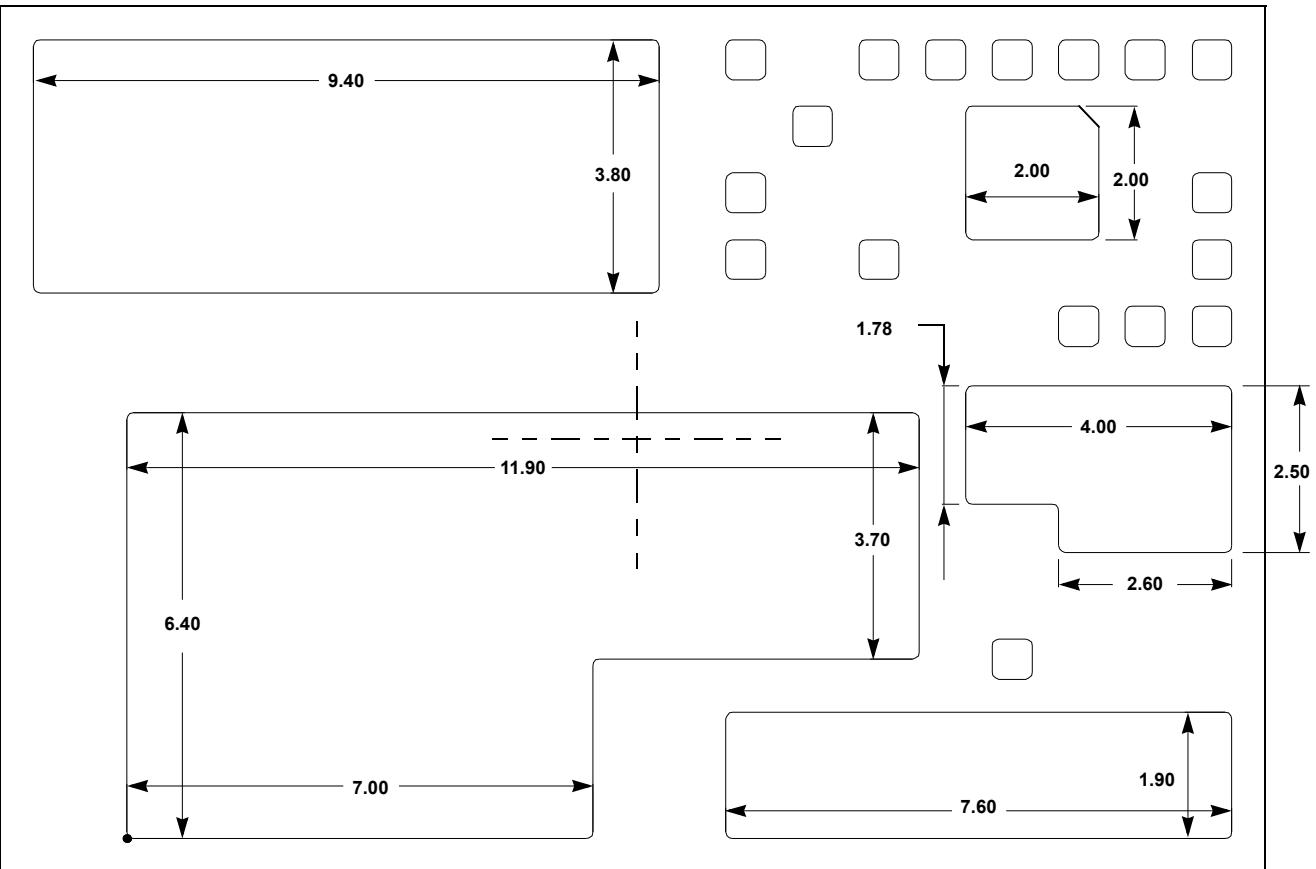
RECOMMENDED SOLDER STENCIL

TOP VIEW 2

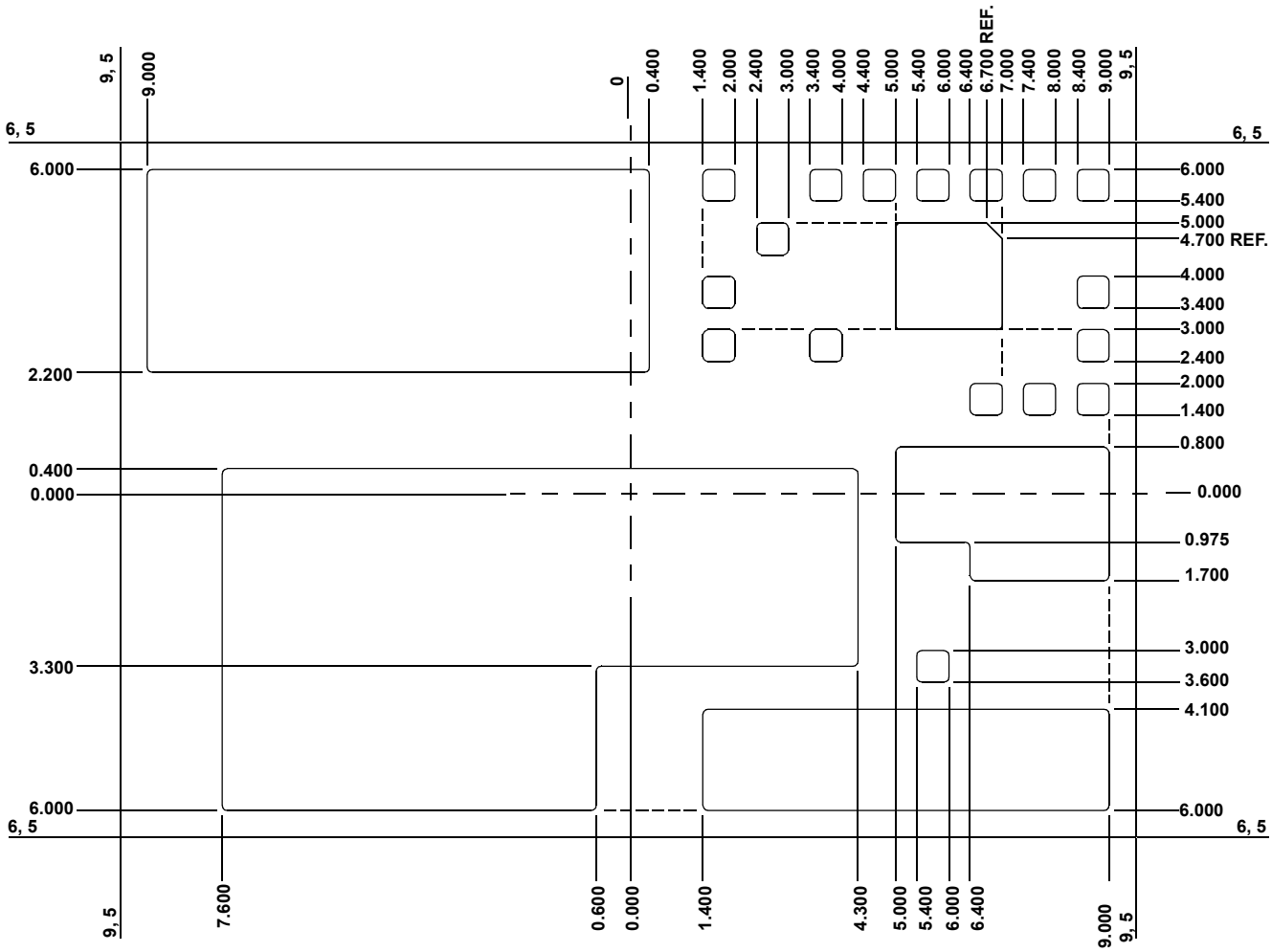


RECOMMENDED POSITIVE SOLDER MASK DEFINED PCB LAND PATTERN

TOP VIEW 1



SIZE DETAILS FOR THE 5 EXPOSED PADS



TERMINAL AND PAD EDGE DETAILS
(BOTTOM VIEW)

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