NCP5008, NCP5009

Backlight LED Boost Driver

The NCP5008/NCP5009 is a high efficiency boost converter operating in current loop control mode to drive Light Emitting Diode. The current mode regulation allows a uniform brightness of the LEDs.

Features

- 2.7 to 6.0 V Input Voltage Range
- Output Voltage from V_{bat} to 15 V
- 3.0 μA Quiescent Supply Current
- Automatically LEDs Current Matching
- No External Sense Resistor
- Includes Dimming Function
- Programmable or Automatic Current Output Mode
- LOCAL or REMOTE Control Facility
- Photo Transistor Sense Feedback Input
- Inductor Based Converter brings High Efficiency
- Low Noise DC/DC Converter
- All Pins are Fully ESD Protected
- Pb−Free Package is Available

Typical Applications

- LED Display Back Light Control
- High Efficiency Step Up Converter

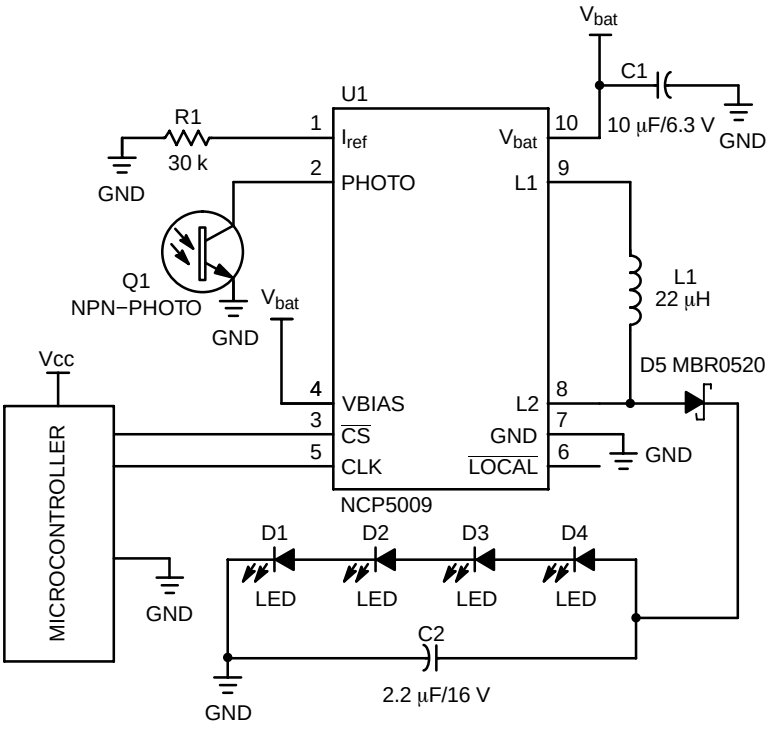
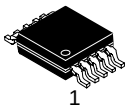


Figure 1. Typical Battery Powered LED Boost Driver

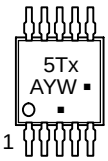
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

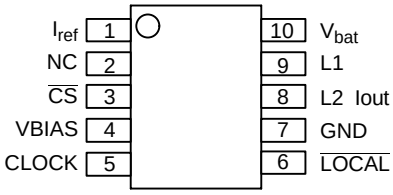


Micro 10
DM SUFFIX
CASE 846B

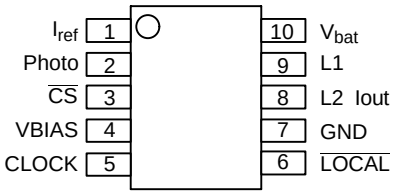


5Tx = Device Number
x = 8 or 9
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



NCP5008



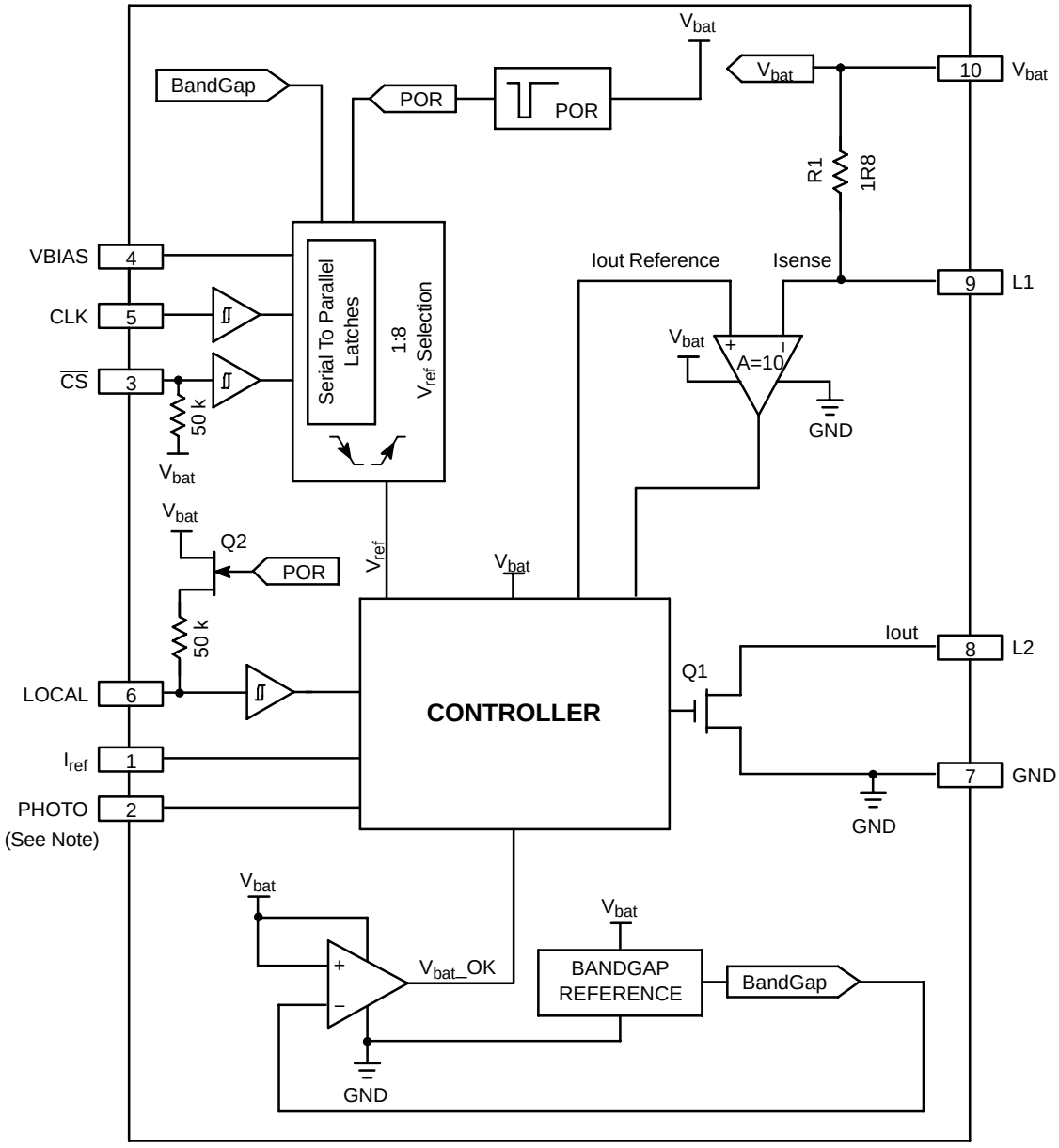
NCP5009

ORDERING INFORMATION

Device	Package	Shipping†
NCP5008DMR2	Micro 10	4000 / Tape & Reel
NCP5008DMR2G	Micro 10 (Pb−Free)	4000 / Tape & Reel
NCP5009DMR2	Micro 10	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BACK LIGHT WHITE LED CURRENT DRIVE CONTROLLER



NOTE: This functionality is NOT implemented on the NCP5008 type.

Figure 2. Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Description
1	I_{ref}	INPUT	This pin provides the output current range adjustment by means of a resistor connected to ground. The current output tolerance depends upon the accuracy of this resistor. Using a ±1% metal film resistor, or better, yields the best output current accuracy.
2	PHOTO	SIGNAL	This pin provides an access to the output current control loop for the NCP5009 version. The current sunk to ground from this pin is subtracted from the output current mirror. Primary use is the ambient light automatic adjustment by means of an external photo transistor connected across this pin and ground. The output current decreases as the ambient light increases. The internal circuit provides a 1/1 current ratio with the I_{ref} defined by the resistor connected from pin 1 to ground. This current shall be limited to 65 μA. This functionality is NOT implemented on the NCP5008 type.
3	$\overline{CS}$	INPUT	Negative going Chip Select logic input. This pin is used to select the NCP5008/ NCP5009 and validate the clock/data when $\overline{CS}$ = Low. The internal shift register is automatically clear to zero upon the falling edge, thanks to a 20 ns built−in one shoot. The built−in pull−up resistor disables the device when the $\overline{CS}$ pin is left open.
4	VBIAS	POWER	This pin should be connected to V_{bat}.
5	CLOCK	INPUT	The clock signal connected to this pin is used to serially shift right the internal preset high logic level. The clock is valid between the falling edge and until the rising edge of the $\overline{CS}$. There is neither a feedback nor an overflow control. If the clock count exceeds 8 bits, the internal register is clear, the output current is forced to zero and the device comes back to the shutdown mode.
6	$\overline{LOCAL}$	INPUT	This pin is used to select the mode of operation. • When $\overline{LOCAL}$ = High or Open, the chip is controlled by two digital lines:$\overline{CS}$ and CLOCK. The output current is programmed by the logic control of these pins, allowing a current adjustment within the range defined by the I_{ref} resistor. • When $\overline{LOCAL}$ = Low, the chip is turned ON /OFF by means of the $\overline{CS}$ line, the CLOCK pins being deactivated. The output current is constant, as defined by the I_{ref} resistor value. In order to minimize the standby current a dynamic pull−up resistor is activated when POR is High, this pull−up resistor being disconnected when $\overline{LOCAL}$ = Low.
7	GND	POWER	This pin is the system ground for the NCP5008/NCP5009 and carries both the Power and the Digital signals. High quality ground must be provided to avoid spikes and/or uncontrolled operation. Care must be observed to avoid high−density current flow in a limited PCB copper track.
8	L2	POWER	This pin is the power side of the external inductor and must be connected either to the external Schottky diode (see Figure 22) or directly to one external LED (see Figure 23). It provides the output current to the load. Since the boost converter operates in a current loop mode, the output voltage can range up to +15 V but shall not extend this limit. The user must make sure this voltage will not be exceeded during the normal operation of this part. An external low cost ceramic capacitor (2.2 μF/16 V, ESR < 100 mΩ) is recommended to smooth the current flowing into the diode(s), thus limiting the noise created by the fast transients present in this circuitry. Care must be observed to avoid EMI though the PCB copper tracks connected to this pin.
9	L1	POWER	The return side of the external inductor shall be connected to this pin. Typical application will use a 22 μH, size 1210, to handle the 2.8 to 364 mA max range. On the other hand, when the desired output current is above 20 mA, the inductor shall have an ESR < 1.0 Ω. The output current tolerance can be improved by using a larger inductor value.
10	V_{bat}	POWER	The external voltage supply is connected to this pin. A high quality reservoir capacitor must be connected across pin 10 and Ground to achieve the specified output voltage parameters. A 10 μF/6.3 V, low ESR capacitor must be connected as close as possible across pin 10 and ground pin 7. The X5R ceramic types are recommended.

Table 1. Shift Register Bits Assignment and Functions

SetReg shift register (Note: The register content is latched upon $\overline{CS}$ positive going).

	B7	B6	B5	B4	B3	B2	B1
Bn Value After POR	0	0	0	0	0	0	0
Iout Peak (mA)	I_{ref}*k*7.5	I_{ref}*k*6.5	I_{ref}*k*5.5	I_{ref}*k*4.5	I_{ref}*k*3.5	I_{ref}*k*2.5	I_{ref}*k*1.5

$\overline{LOCAL}$	CLOCK	$\overline{CS}$	B1−B7	Output Current
L	X	H	X	0
L	X	L	X	I_{ref} * k
H or Open	X	H	No Change	I_{ref} * k * (Bn + 0.5)
H or Open	↓	L	No Change	I_{ref} * k * (Bn + 0.5)
H or Open	↑	L	$Q_{data} \rightarrow$ Bn	I_{ref} * k * (Bn + 0.5)

The register is clear to 0 during the first 20 ns following the $\overline{CS}$ falling edge.

Note:

Coefficient Value (internal ratio): k = 746

Maximum output peak current @ B7 = 1 and Iphoto = 0 μA : Iout peak = I_{ref} * (7 + 0.5) * 746 = I_{ref} * 5595

$$I_{ref} = \frac{V_{ref}}{R1} = \frac{1.24\ V}{R1}$$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply	V_{bat}, V_{BIAS}	7.0	V
Output Power Supply Voltage Compliance	V_{L2}	16	V
Digital Input Voltage Digital Input Current	CLK, $\overline{CS}$	−0.3 < V < V_{bat} + 3.0 V 1.0	V mA
Human Body Model: R = 1500 Ω, C = 100 pF	ESD	±2.0	kV
Machine Model	ESD	±200	V
Micro 10 Package Power Dissipation @ T_A = +85°C Thermal Resistance, Junction−to−Air	 P_D R_{Thja}	 200 200	 mW °C/W
Operating Ambient Temperature Range	T_A	−25 to +85	°C
Operating Junction Temperature Range	T_J	−25 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

POWER SUPPLY SECTION (−25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
Power Supply	10	V_{bat}	2.7	−	6.0	V
Power Supply Threshold Startup Voltage	10	V_{batThr}	−	2.3	2.7	V
Output Load Voltage Compliance	8	V_{out}	−	−	15.0	V
Pulsed Current Regulation Range	8	I_{out}	0	−	400	mA
Continuous DC Current in the Load	8	I_{out}	−	−	75	mA
Output Pulsed Current Tolerance @ V_{bat} = 3.6 V, L1 = 22 μH/0.71 Ω, R_{ref} ±1%, I_{LED} = 20 mA (Note 1)	8	I_{out}	−	±5.0	−	%
Output Leakage @ LOCAL = 0, $\overline{CS}$ = H, Vout = 15 V, V_{bat} = 6.0 V	8	I_{out}	−	−	500	nA
Standby Current @ Iout = 0 mA, $\overline{CS}$ = H, CLK = H, V_{bat} = V_{BIAS} = 3.6 V	10	I_{stdb}	−	3.0	−	μA
Standby Current @ Iout = 0 mA, $\overline{CS}$ = H, CLK = H, V_{bat} = V_{BIAS} = 6.0 V	10	I_{stdb}	−	−	10	μA
Operating Current @ V_{bat} = V_{BIAS} = 3.6 V, I_{ref} = 30 μA, CLK = H, $\overline{CS}$ = L, LOCAL = Open	10	I_{ope}	−	600	−	μA
Boost Internal Oscillator Clock @ L1 = 22 μH, V_{bat} = V_{BIAS} = 3.6 V, Iout = 20 mA (Vout = 14 V)	−	F_{osc}	−	300	−	kHz

1. The tolerance refers to the 20 mA to 70 mA current range.

DIGITAL SECTION (−25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
High Level Input Voltage (Note 2) Low Level Input Voltage (Note 2) Input Capacitance	3, 5	V_{IH} V_{IL} C_{in}	0.7*V_{bat} − −	− − 10	V_{bat} 0.3*V_{bat} −	V V pF
High Level Input Voltage (Note 2) Low Level Input Voltage (Note 2) Input Capacitance	6	V_{IH} V_{IL} C_{in}	− − −	0.6*V_{bat} 0.4*V_{bat} 10	− − −	V V pF
LOCAL Pullup Resistor	6	R_{loc}	20	−	80	kΩ
LOCAL Leakage Current	9	I_{Loc}	−	−	100	nA
$\overline{CS}$ Pullup Resistor	3	R_{cs}	20	−	80	kΩ
Minimum $\overline{CS}$ Low Time	3	Tcs_{setup}	250	−	−	ns
Clock Frequency	5	F_{CLK}	−	−	5.0	MHz
CLOCK tr and tf	5	tr_{CLK}, tf_{CLK}	10	−	−	ns
Internal Register Clear	−	t_{clear}	10	30	−	ns
Internal Power on Reset Width	−	t_{POR}	−	100	−	μs

2. Digital inputs undershoot < − 0.30 V, Digital inputs overshoot < 0.30 V.

ANALOG SECTION (−25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
Output Voltage Range Reference @ 2.5 μA < I_{ref} < 65 μA (Note 3)	1	V_{ref}	1.20	1.24	1.28	V
Maximum Output Current Range Ratio	8	I_{out}	−	5595	−	−
Minimum Output Current Range Ratio	8	I_{out}	−	1119	−	−
Output Current Sense Resistor	10, 9	R_s	−	1.8	5.0	Ω
Output Voltage Range Reference @ 2.5 μA < Ipho < 65 μA	2	V_{pho}	1.20	1.24	1.28	V
Output Current Stabilization tdelay following a DC/DC startup	8	I_{outdly}	−	100	−	μs
Internal NMOS Resistor @ V_{bat} = 3.6 V	8	QR_{DSON}	−	2.2	3.0	Ω
Internal Comparator Delay Time	−	Td_{comp}	−	60	−	ns

3. The overall tolerance depends upon the accuracy of the external resistor. Using a 1%/low PPM metal film resistor is recommended to achieve ±5% output current tolerance.

TYPICAL OPERATING CHARACTERISTICS

Condition: Typical Application: L = 22 μH, Cin = 10 μF, Cout = 2.2 μF, R1 = 30 kΩ

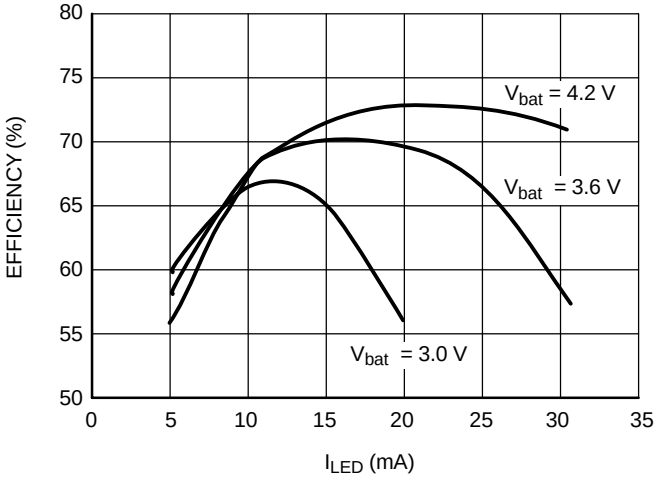


Figure 3. Efficiency vs. Load Current @ 4 LEDS (V_{load} = 4*Vf ⇒ 14.2 V)

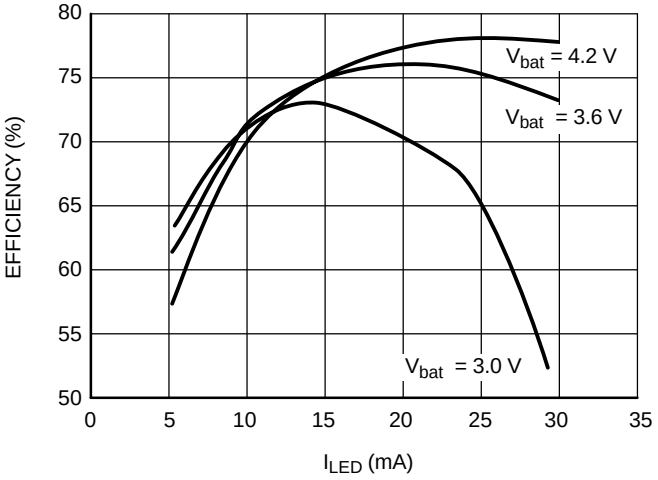


Figure 4. Efficiency vs. Load Current @ 3 LEDS (V_{load} = 3*Vf ⇒ 10.5 V)

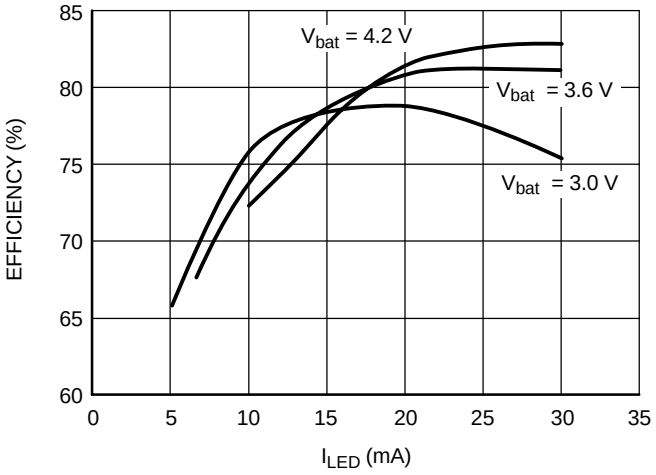


Figure 5. Efficiency vs. Load Current @ 2 LEDS (V_{load} = 2*Vf ⇒ 7.1 V)

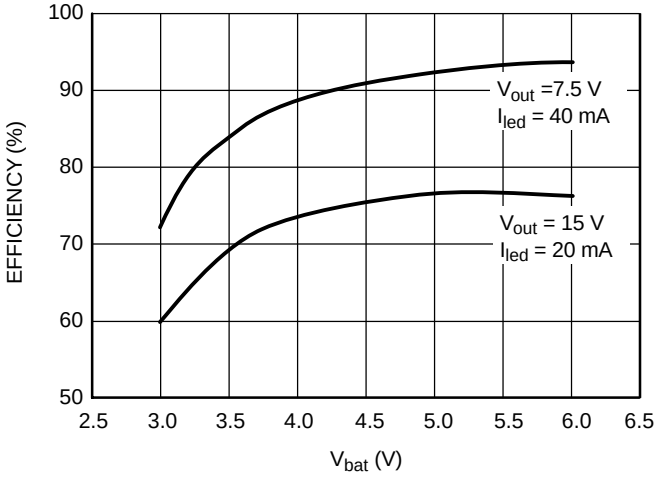


Figure 6. Efficiency vs. V_{bat} @ V_{out} = 15 V/I_{led} = 20mA and V_{out} = 7.5 V/I_{led} = 40 mA

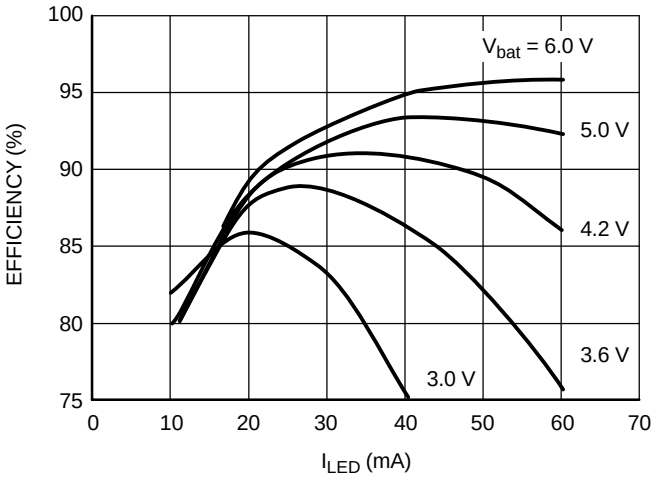


Figure 7. Efficiency vs. Load Current @ 4 LEDS (V_{load} = 2 strings of 2 LEDs in series = 7.1V)

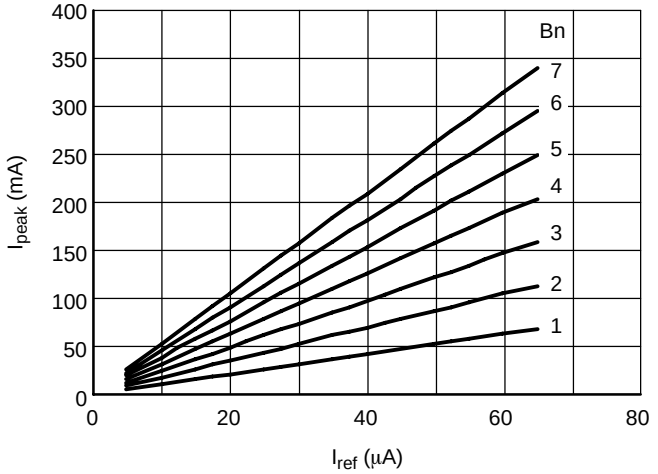


Figure 8. Inductor peak Current vs. I_{ref} @ Bn = {1, 2, 3, 4, 5, 6, 7}

TYPICAL OPERATING CHARACTERISTICS

Condition: Typical Application: L = 22 μH, Cin = 10 μF, Cout = 2.2 μF, R1 = 30 kΩ

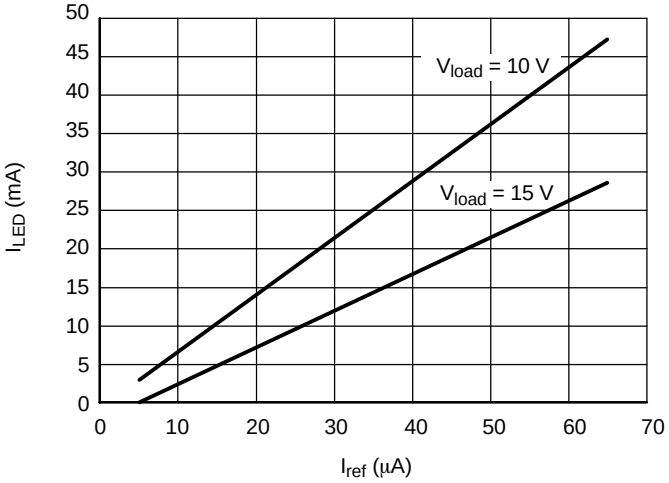


Figure 9. Load Current (I_{led}) vs. I_{ref} @ V_{bat} = 3.6 V, V_{load} = 15 V and 10 V

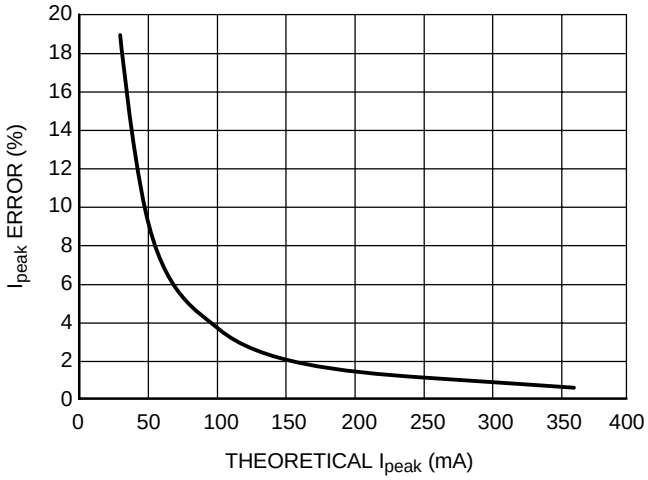


Figure 10. Inductor Peak Current Error vs. Theoretical Inductor Peak Current

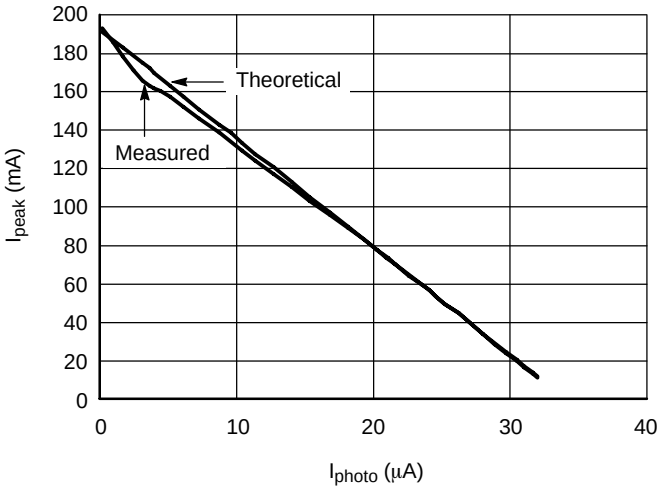


Figure 11. Inductor Peak Current vs. I_{photo} @ I_{ref} = 34 μA

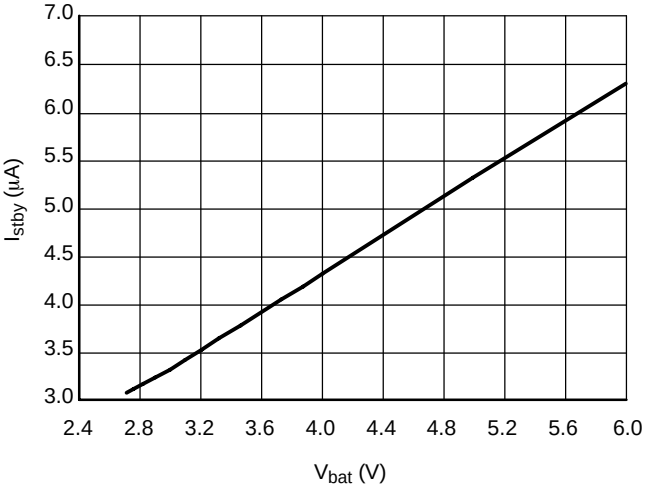


Figure 12. Stand by Current vs. V_{bat} @ T = 20°C

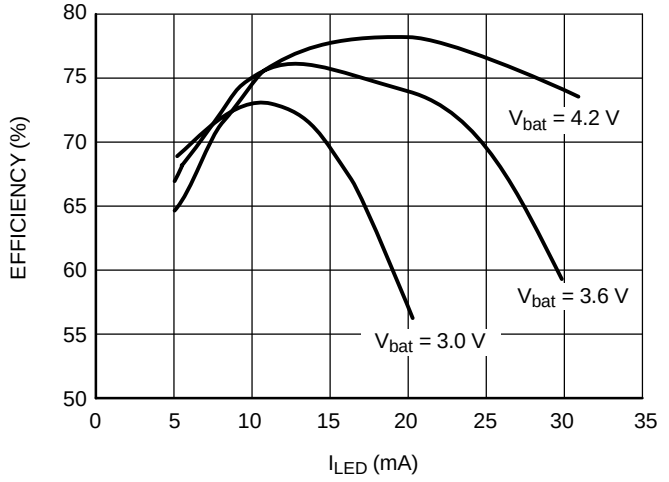


Figure 13. Efficiency vs. Load Current @ 4 LEDS (V_{load} = 4*Vf ⇒ 14.2 V)

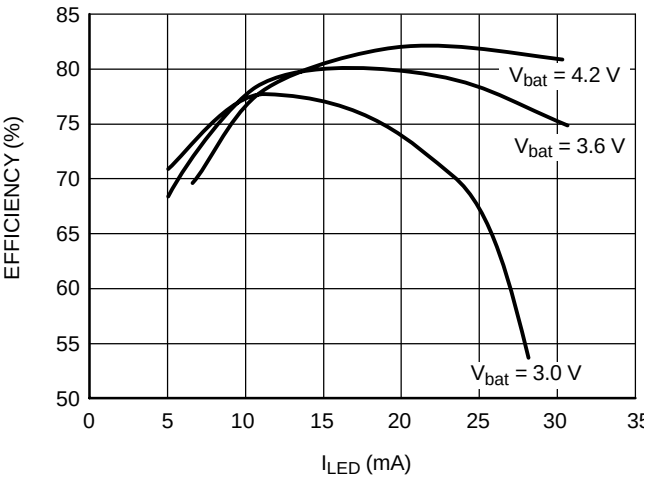


Figure 14. Efficiency vs. Load Current @ 3 LEDS (V_{load} = 3*Vf ⇒ 10.5 V)

TYPICAL OPERATING CHARACTERISTICS

Condition: Typical Application: L = 22 μH, Cin = 10 μF, Cout = 2.2 μF, R1 = 30 kΩ

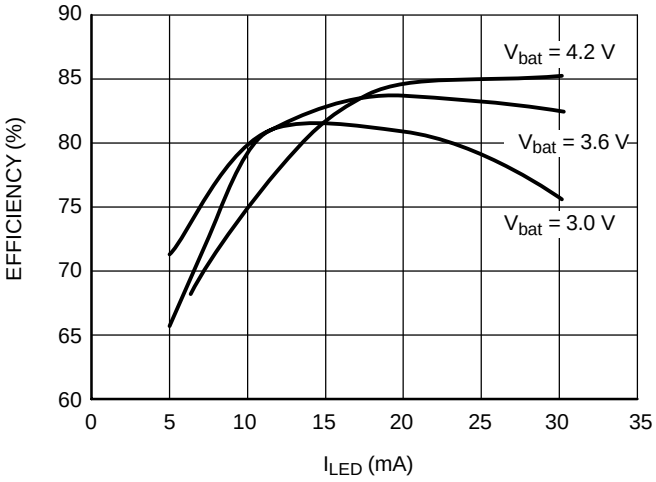


Figure 15. Efficiency vs Load Current @ 2 LEDS (V_{load} = 2*Vf ⇒ 7.1 V)

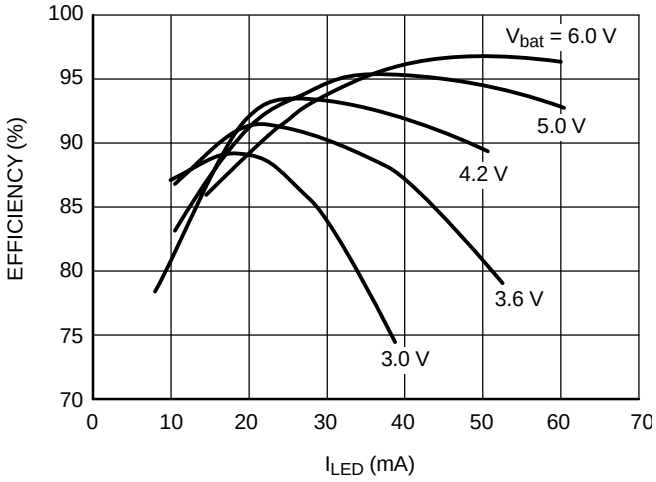


Figure 16. Efficiency vs Load Current @ 4 LEDS (V_{load} = 2 strings of 2 LEDs in series = 7.1 V)

Operating Description

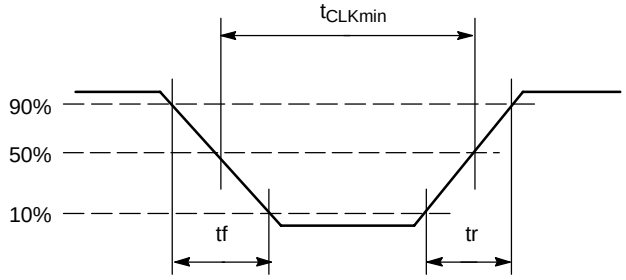


Figure 17. Digital Timing Definitions

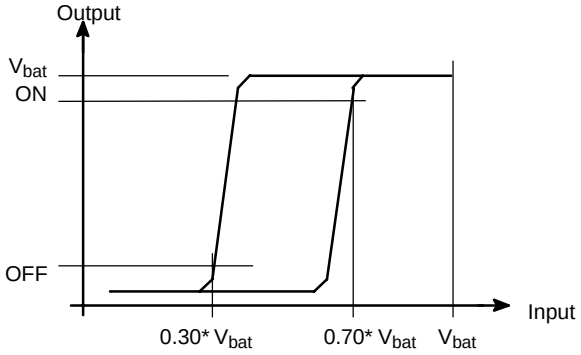


Figure 18. Typical Schmitt Trigger Characteristic

Input Schmitt Triggers

All the Logic Input pins have built−in Schmitt trigger circuits to prevent the NCP5008/NCP5009 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 18.

The output signal is guaranteed to go High when the input voltage is above 0.70*V_{bat}, and will go Low when the input voltage is below 0.30*V_{bat}.

Local Mode

When the system operate in a Local Mode (Pin 6, /LOCAL=Low), the output current depends solely upon the current drawn pin 1. The clock signal is irrelevant and the output current is derived by equation $I_{out} = I_{ref} * k$, the internal constant k being equal to 746.

ESD Protection

The NCP5008/NCP5009 includes silicon devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed in the applications, the built−in structures have been designed to handle ±2.0 kV in Human Body Model (HBM) and ±200 V in Machine Model (MM) and on each pin.

Remote Control Programming Sequence

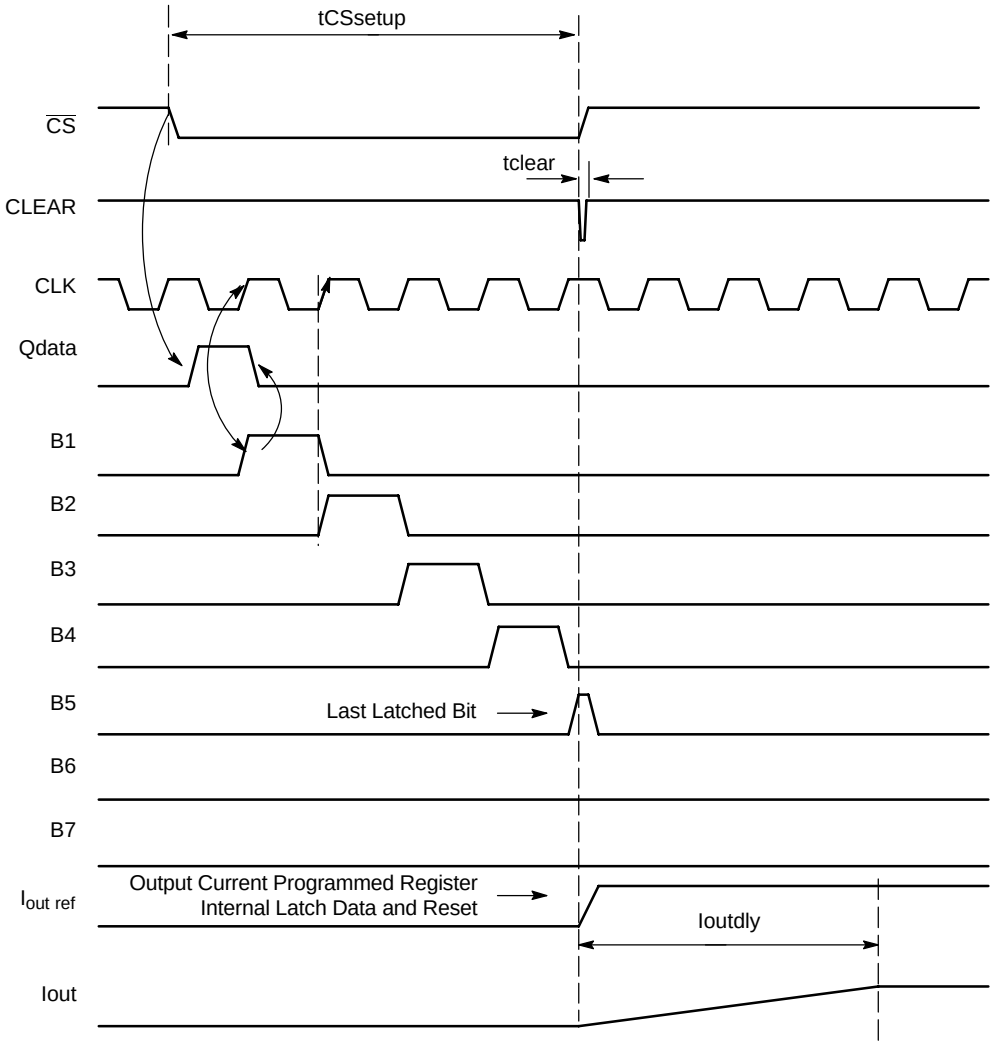


Figure 19. Programming Sequence

Upon $\overline{CS}$ transition from High to Low, the internal sequence will take place:

- Qdata is internally set to high level.
- Upon positive going transition of the next CLK signal, the Qdata is shifted to the next Bn stage.
- Clear the Qdata flip−flop upon the positive going of the SetReg[B1] transient.

The sequence keeps going until $\overline{CS}$ = High.

When the $\overline{CS}$ line returns to a High state, the programming output current flip−flop is set according to the previous state of the shift register and SetReg B[1−7] is cleared afterward.

Depending upon the $\overline{CS}$ width, for a given CLK period, the last SetReg bit will be latched and the output current will be adjusted accordingly. If the number of CLK pulses is higher than 7, the Qdata is lost and the SetReg register bits B[1−7] are in the Low state, yielding a zero output current.

The internal shift register can be clear by sending more than 7 pulses to the CLK pin when the pin $\overline{CS}$ is low. If the internal shift register is clear upon the $\overline{CS}$ transition from Low to High, the device will be placed or maintained in the shut down mode.

When the register content is higher than zero, the DC/DC is activated and a 100 μs delay (typical) is necessary to stabilize the output current to the programmed value.

Set Up Output Current Range

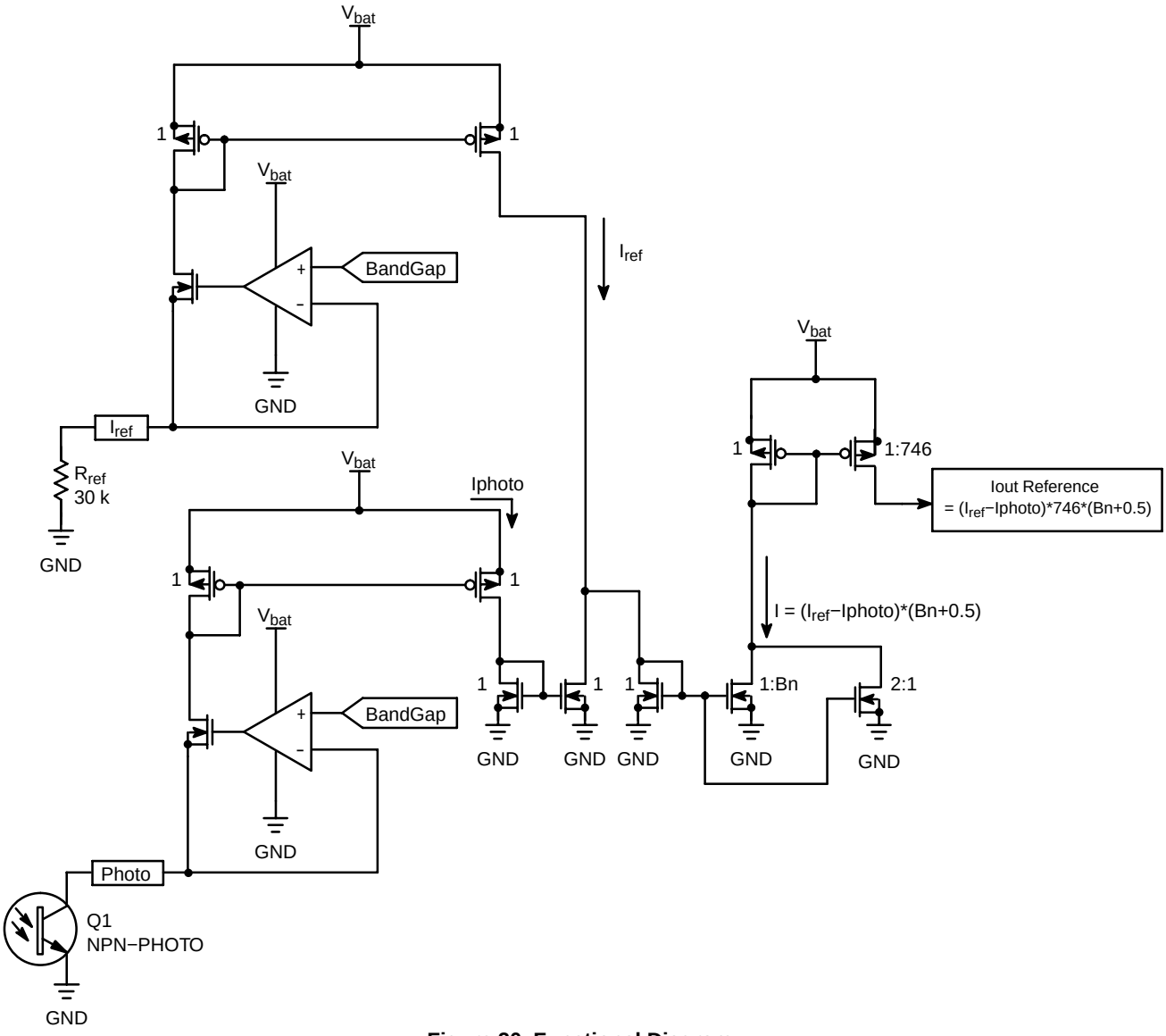


Figure 20. Functional Diagram

The current sunk to ground on PHOTO pin is subtracted from the current sunk to ground on I_{ref} pin. The result is multiplied by the programmed value (Bn) and then multiplied by the constant factor ratio (k = 746) in the current mirror.

The constant factor k is a ratio between the current on Iout sense and the Iout reference internally fixed.

The output current reference is:

Ipeak = Ivalley + (I_{ref} − Iphoto) * Bn * k.

Where k = 746, Bn represents the bit of the internal shift register, range from 1 to 7, and Ivalley = (I_{ref} − Iphoto) * 0.5 * k.

We can write also Ipeak = (I_{ref} − Iphoto) * (Bn + 0.5) * k.

Please find below the formula to quickly calculate R1 resistor (resistor on I_{ref} pin):

$$I_{ref} = \frac{1.24}{R1}$$

DC/DC Converter Operation

The DC/DC converter operates with a boost structure depicted in Figure 21, the load being supplied by the pulsed current coming from the external inductor L1. The current is monitored by the internal sense resistor Rsense to Set and Reset the flip−flop U3 and U6 according to the comparators U2 and U4 output state.

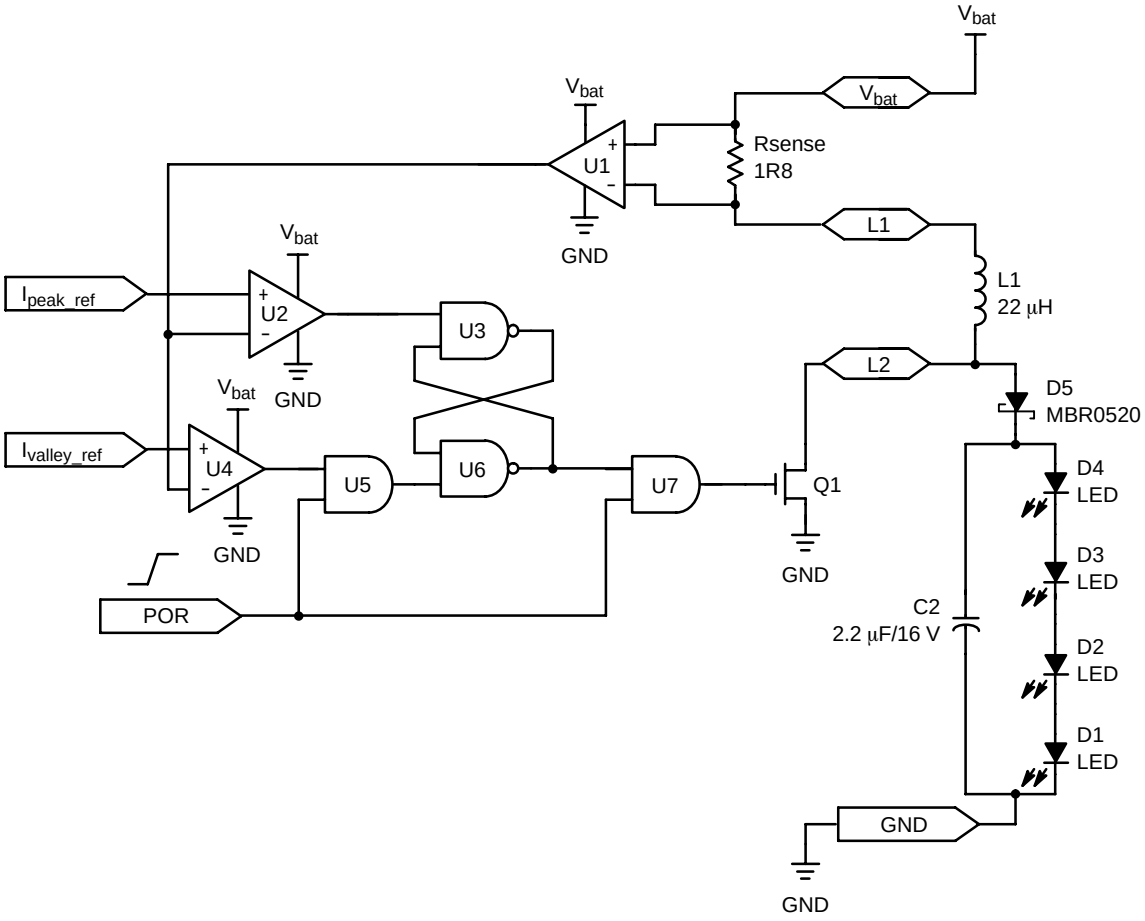


Figure 21. Basic DC/DC Boost Structure

Output Load Drive

In order to make profit of the built−in Boost capabilities, one shall operate the NCP5008/NCP5009 in the continuous output current mode. Such a mode is achieved by using and external reservoir capacitor (preferably a low ESR ceramic type) across the LED as depicted in Figures 22, 23, 24, 25, and 26.

Using an extra photo sensor is not mandatory and the related pin 2 can be either left open or connected to V_{bat}, but must not be grounded on the NCP5009 version only.

At this point, the designer must carefully analyze two parameters:

1. The output voltage must be limited to 15 V maximum. It's the designer responsibility to make sure that spike voltages beyond the maximum rating will not exist across pin 8 and ground. Depending upon a specific application (V_{bat} voltage, PCB layout…), using an external voltage clamp could be necessary.
2. The peak current flowing into the LED diodes shall be within the maximum ratings specified for these devices.

The Schottky diode D5, associated with capacitor C2, provides a rectification and filtering function.

When a pulse−operating mode is acceptable:

- The LEDs brightness can be controlled in LOCAL mode with a PWM on $\overline{CS}$ pin as depicted in Figure 24.
- Or the Schottky can be removed and replaced by at least one LED diode as depicted in Figure 23.

TYPICAL APPLICATION CIRCUIT

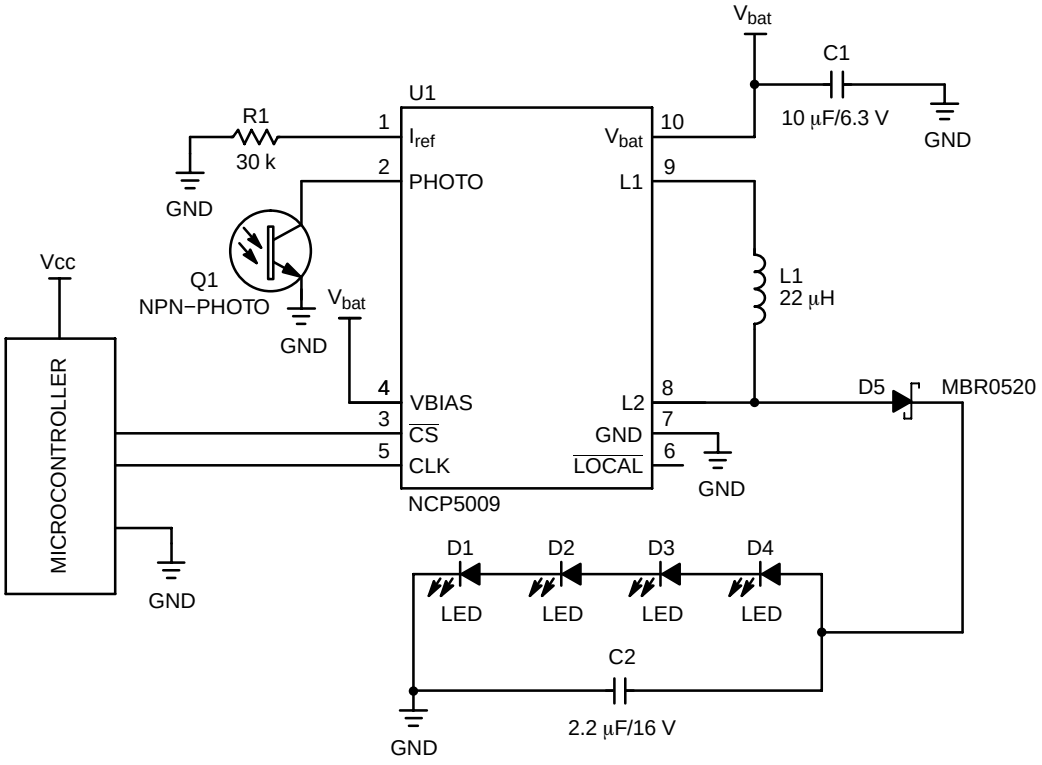


Figure 22. Basic DC Current Mode Operation in REMOTE Control

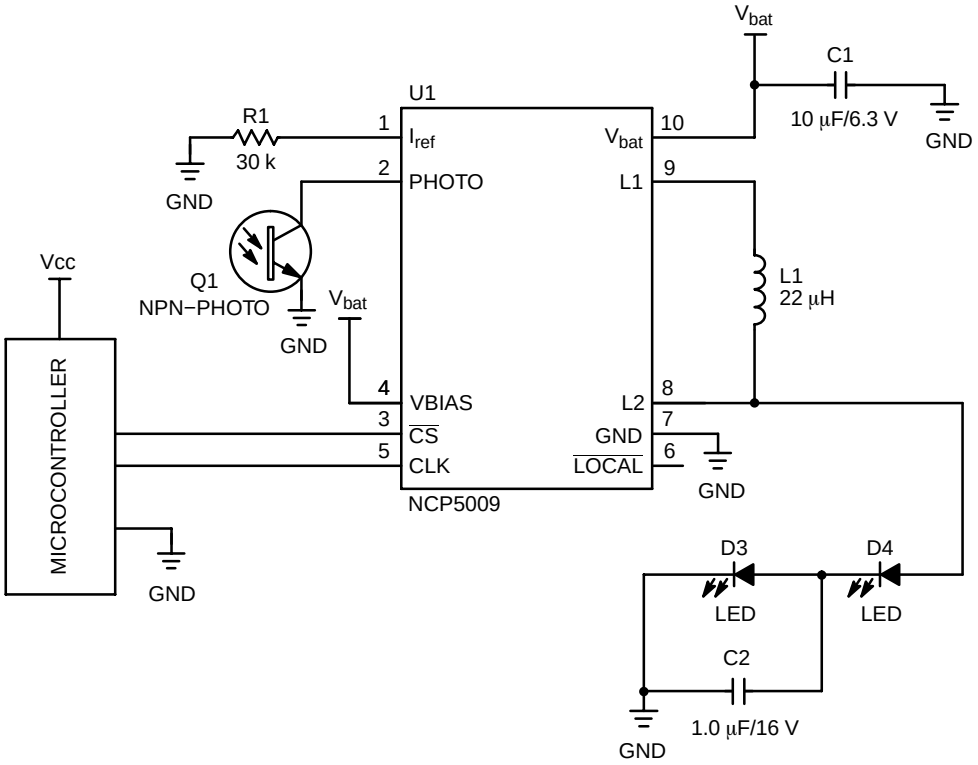


Figure 23. Typical Semi−Pulsed Mode of Operation in REMOTE Mode

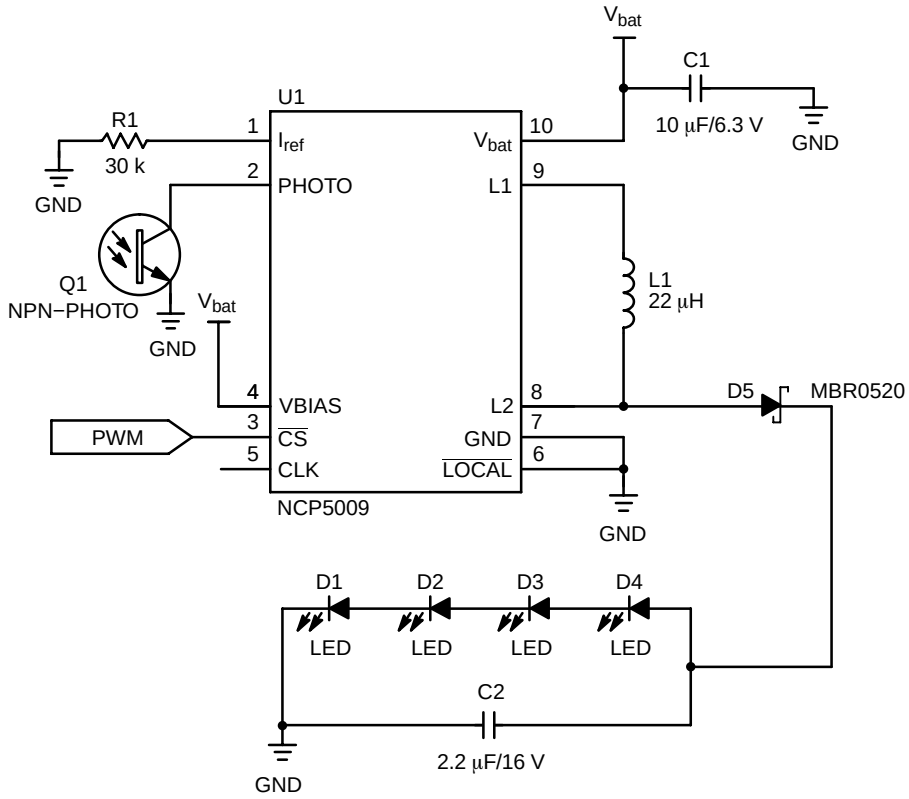


Figure 24. PWM Current Control Mode Operation in LOCAL Mode

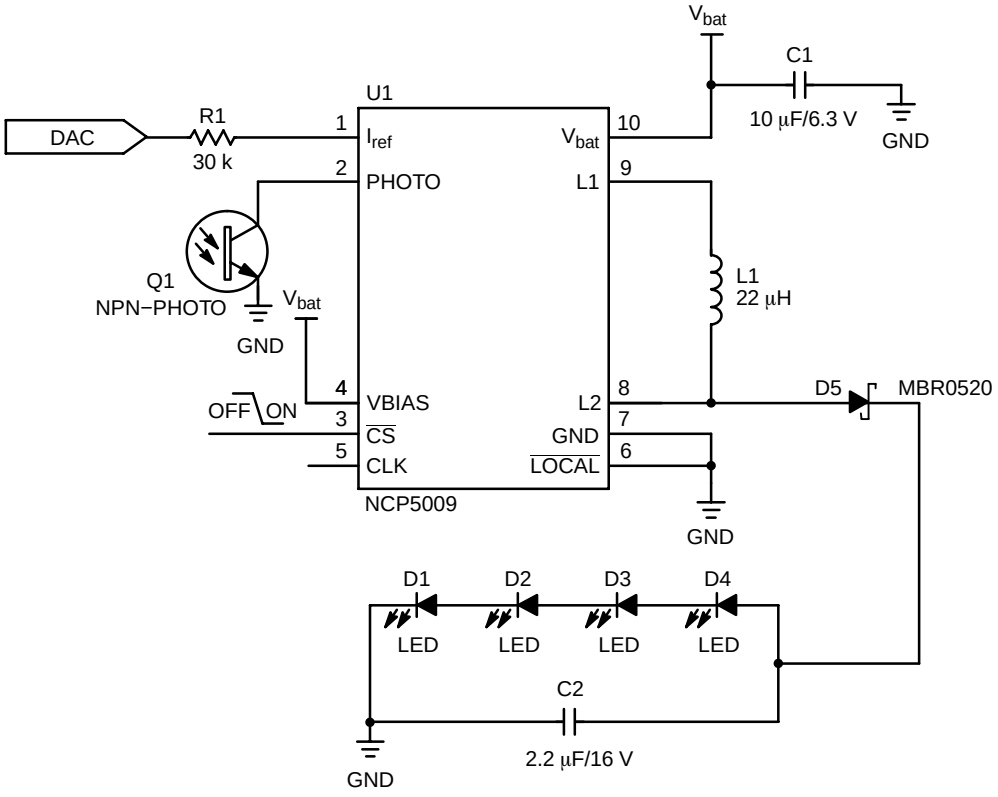


Figure 25. DAC Current Control Mode Operation in LOCAL Mode

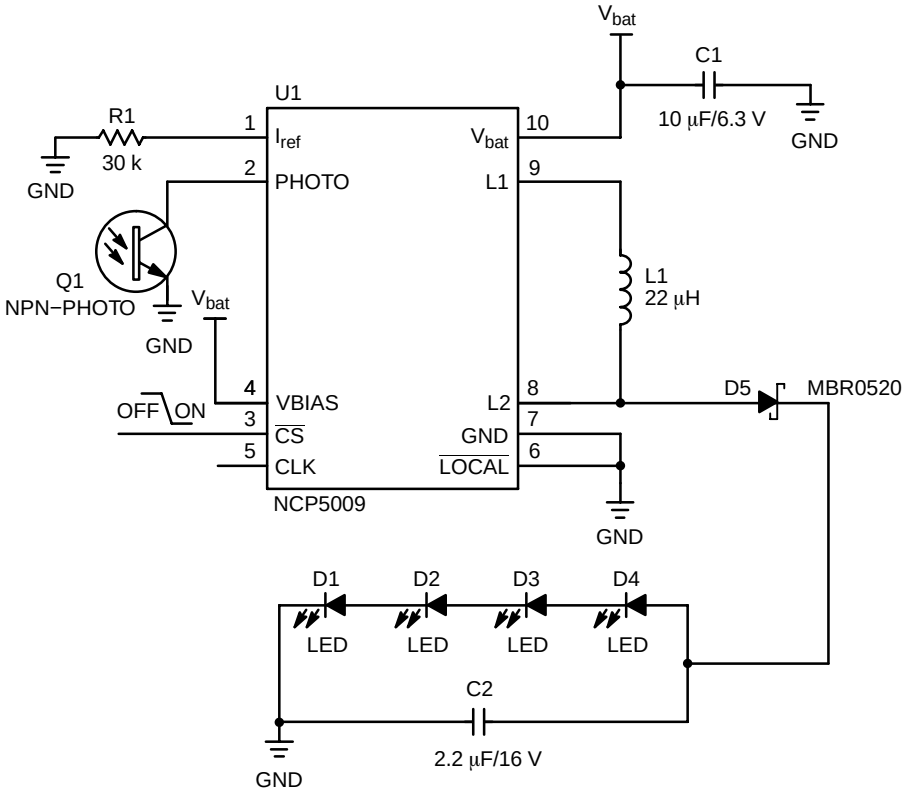


Figure 26. Basic DC Current Mode Operation in LOCAL Mode

TYPICAL LEDS LOAD MAPPING

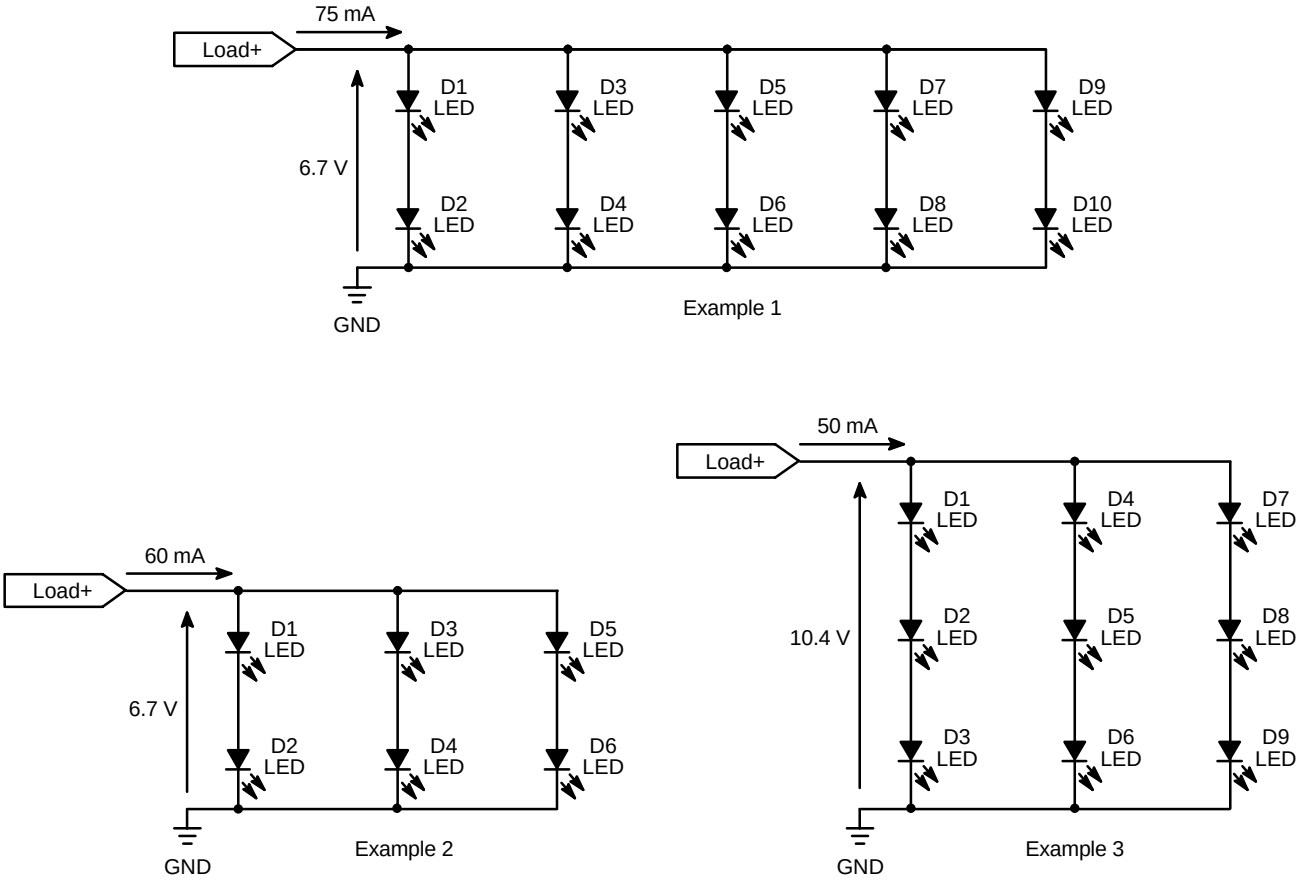


Figure 27. Three different examples of load can be driven by the NCP5009 or NCP5008
Condition: V_{bat} = 3.6 V, L = 22 μH

MANUFACTURER REFERENCE

Design Ref	Value/Reference or Size	Manufacturer	Reference Number
D5	MBR0520/SOD−123	ON Semiconductor	MBR0520
L1	22 μH/1210	MURATA	LQH3C220K34
C1	10 μF/ 6.3 V/0805	MURATA	GRM40 X5R 106K 6.3
C2	2.2 μF/16 V/1206	MURATA	GRM42−6 X7R 225K 16
Q1	SFH320/PLCC2	Osram	SFH320
D1 to D4	White LED	Osram	LW5413−VBW−1

LAYOUT EXAMPLE

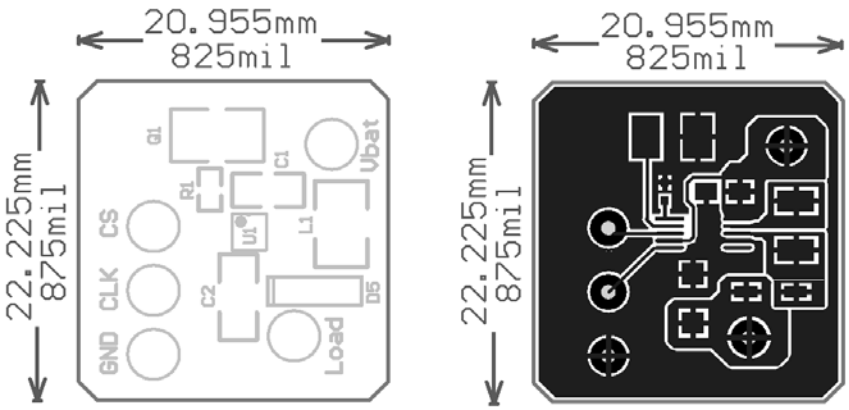


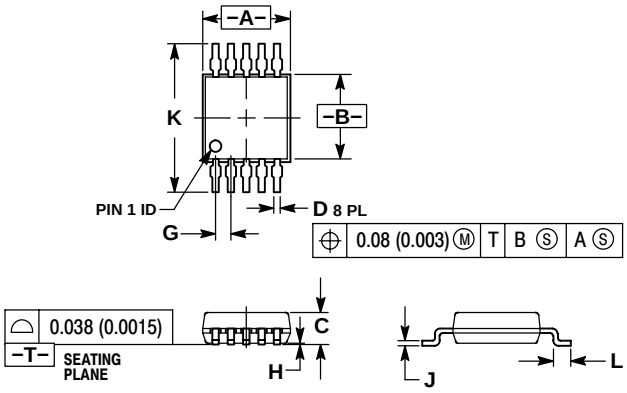
Figure 28. Typical Printed Circuit Layout (the Top Silk Screen and the Top Layer)

The Figure 28 represents the typical printed circuit layout based on the basic application Figure 1. This application has been routed on a single copper layer to save cost. A dual side PCB has better noise protection and can be the right choice for an industrial system. In order to avoid voltage spikes, care must be observed to group the capacitors, the inductor, the Schottky diode and the integrated circuit in the same area. On the other hand, using large copper tracks to reduce the resistor connectivity is strongly recommended.

Obviously, the connectors GND, CLK, $\overline{CS}$, V_{bat} and Load are for engineering purpose only and not for final application.

PACKAGE DIMENSIONS

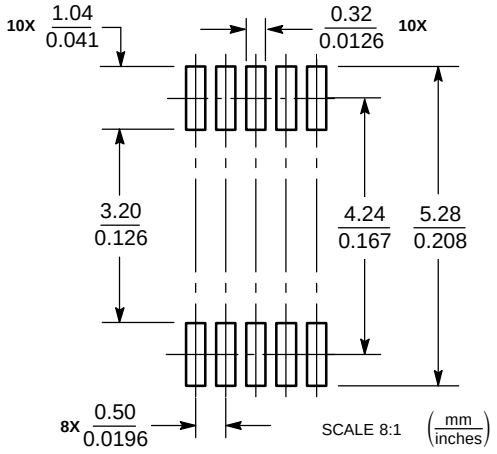
Micro10
CASE 846B−03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B−01 OBSOLETE. NEW STANDARD 846B−02

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.30	0.008	0.012
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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