



## Phase Control Thyristors (Stud Version), 80 A



TO-209AC (TO-94)

### FEATURES

- Hermetic glass-metal seal
- International standard case TO-209AC (TO-94)
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT

### TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY	
$I_{T(AV)}$	80 A
$V_{DRM}/V_{RRM}$	400 V, 800 V, 1200 V
$V_{TM}$	1.60 V
$I_{GT}$	120 mA
$T_J$	-40 °C to 125 °C
Package	TO-209AC (TO-94)
Diode variation	Single SCR

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		80	A
	$T_C$	85	°C
$I_{T(RMS)}$		125	A
$I_{TSM}$	50 Hz	1900	
	60 Hz	1990	
$I^2t$	50 Hz	18	kA <sup>2</sup> s
	60 Hz	16	
$V_{DRM}/V_{RRM}$		400 to 1200	V
$t_q$	Typical	110	µs
$T_J$		-40 to 125	°C

### ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	$V_{DRM}/V_{RRM}$ , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM}$ MAXIMUM AT $T_J = 125$ °C mA
VS-80RIA VS-81RIA	40	400	500	15
	80	800	900	
	120	1200	1300	



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave		80	A
				85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 75 °C case temperature		125	
Maximum peak, one-cycle non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reappplied	1900	A
		t = 8.3 ms		1990	
		t = 10 ms	100 % $V_{RRM}$ reappplied	1600	
		t = 8.3 ms		1675	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reappplied	18	kA <sup>2</sup> s
		t = 8.3 ms		16	
		t = 10 ms	100 % $V_{RRM}$ reappplied	12.7	
		t = 8.3 ms		11.7	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reappplied		180.5	kA <sup>2</sup> √s
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.99	V
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		1.13	
Low level value of on-state slope resistance	$r_{t1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		2.29	mΩ
High level value of on-state slope resistance	$r_{t2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		1.84	
Maximum on-state voltage	$V_{TM}$	$I_{pk} = 250$ A, $T_J = 25$ °C, $t_p = 10$ ms sine pulse		1.60	V
Maximum holding current	$I_H$	$T_J = 25$ °C, anode supply 12 V resistive load		200	mA
Typical latching current	$I_L$			400	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	$T_J = 125$ °C, $V_d = \text{Rated } V_{DRM}$ , $I_{TM} = 2 \times di/dt$ snubber 0.2 μF, 15 Ω, gate pulse: 20 V, 65 Ω, $t_p = 6$ μs, $t_r = 0.5$ μs Per JEDEC standard RS-397, 5.2.2.6.		300	A/μs
Typical delay time	$t_d$	Gate pulse: 10 V, 15 Ω source, $t_p = 6$ μs, $t_r = 0.1$ μs, $V_d = \text{Rated } V_{DRM}$ , $I_{TM} = 50$ Adc, $T_J = 25$ °C		1	μs
Typical turn-off time	$t_q$	$I_{TM} = 50$ A, $T_J = T_J$ maximum, $di/dt = -5$ A/μs, $V_R = 50$ V, $dV/dt = 20$ V/μs, gate bias: 0 V 25 Ω, $t_p = 500$ μs		110	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = 125$ °C exponential to 67 % rated $V_{DRM}$		500	V/μs
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = 125$ °C rated $V_{DRM}/V_{RRM}$ applied		15	mA



<b>TRIGGERING</b>					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms		12	W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$		3	
Maximum peak positive gate current	$I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms		3	A
Maximum peak positive gate voltage	$+V_{GM}$			20	V
Maximum peak negative gate voltage	$-V_{GM}$			10	
Maximum DC gate current required to trigger	$I_{GT}$	$T_J = -40$ °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 6 V anode to cathode applied	270	mA
		$T_J = 25$ °C		120	
		$T_J = 125$ °C		60	
Maximum DC gate voltage required to trigger	$V_{GT}$	$T_J = -40$ °C		3.5	V
		$T_J = 25$ °C		2.5	
		$T_J = 125$ °C		1.5	
DC gate current not to trigger	$I_{GD}$	$T_J = T_J$ maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated $V_{DRM}$ anode to cathode applied	6	mA
DC gate voltage not to trigger	$V_{GD}$			0.25	V

<b>THERMAL AND MECHANICAL SPECIFICATIONS</b>					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum operating junction temperature range	$T_J$			- 40 to 125	°C
Maximum storage temperature range	$T_{Stg}$			- 40 to 150	
Maximum thermal resistance, junction to case	$R_{thJC}$	DC operation		0.30	K/W
Maximum thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, smooth, flat and greased		0.1	
Mounting torque, $\pm 10$ %		Non-lubricated threads		15.5 (137)	N · m (lbf · in)
		Lubricated threads		14 (120)	
Approximate weight				130	g
Case style		See dimensions - link at the end of datasheet		TO-209AC (TO-94)	

<b><math>\Delta R_{thJC}</math> CONDUCTION</b>				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.042	0.030	$T_J = T_J$ maximum	K/W
120°	0.050	0.052		
90°	0.064	0.070		
60°	0.095	0.100		
30°	0.164	0.165		

**Note**

- The table above shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC



# VS-80RIA...PbF, VS-81RIA...PbF, VS-82RIA...PbF Series

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Vishay Semiconductors

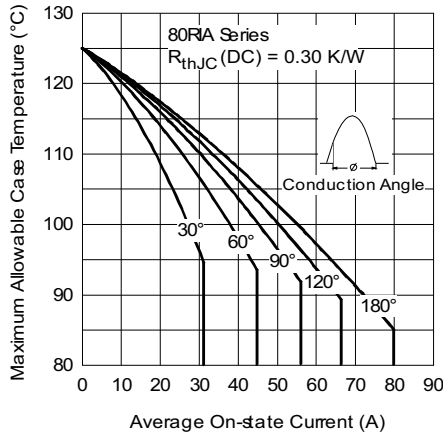


Fig. 1 - Current Ratings Characteristics

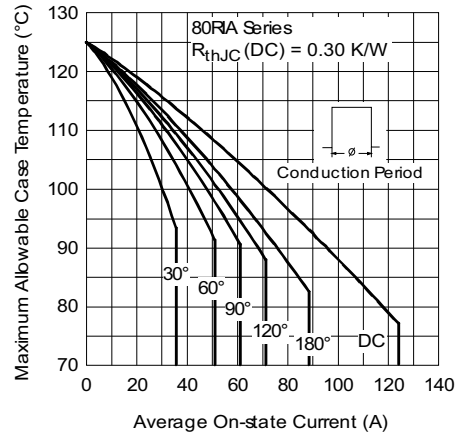


Fig. 2 - Current Ratings Characteristics

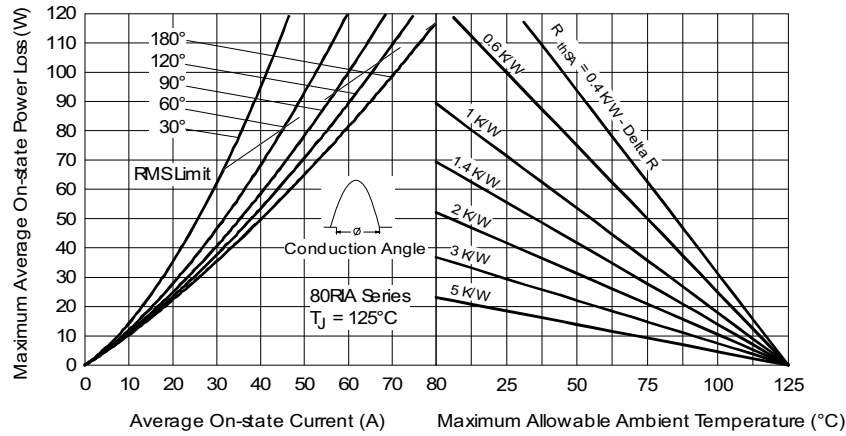


Fig. 3 - On-State Power Loss Characteristics

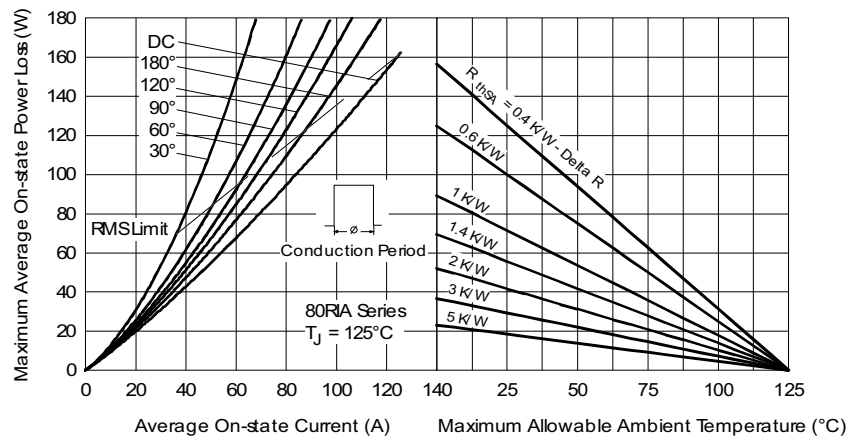


Fig. 4 - On-State Power Loss Characteristics

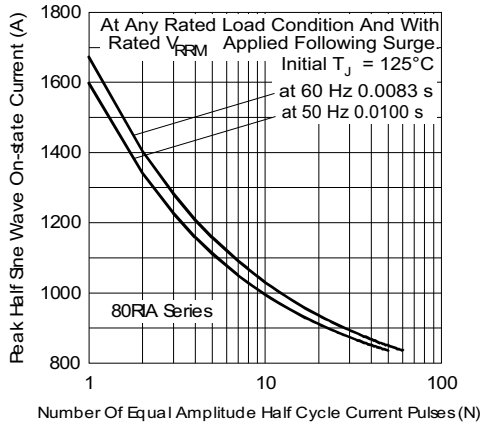


Fig. 5 - Maximum Non-Repetitive Surge Current

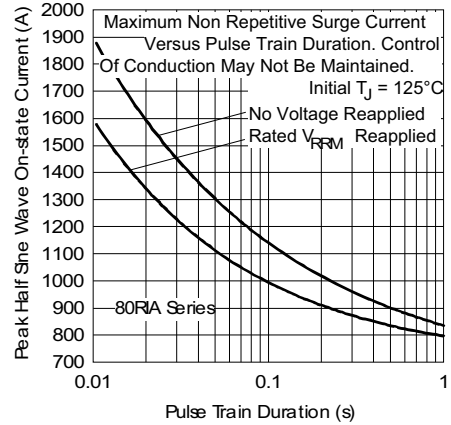


Fig. 6 - Maximum Non-Repetitive Surge Current

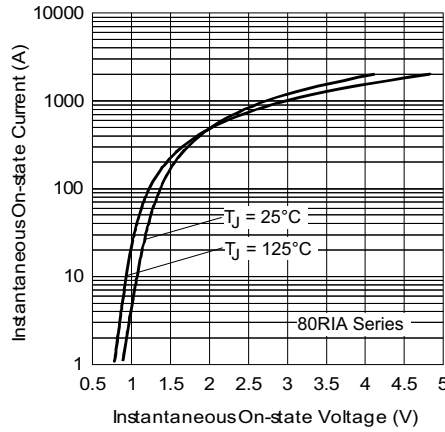


Fig. 7 - On-State Voltage Drop Characteristics

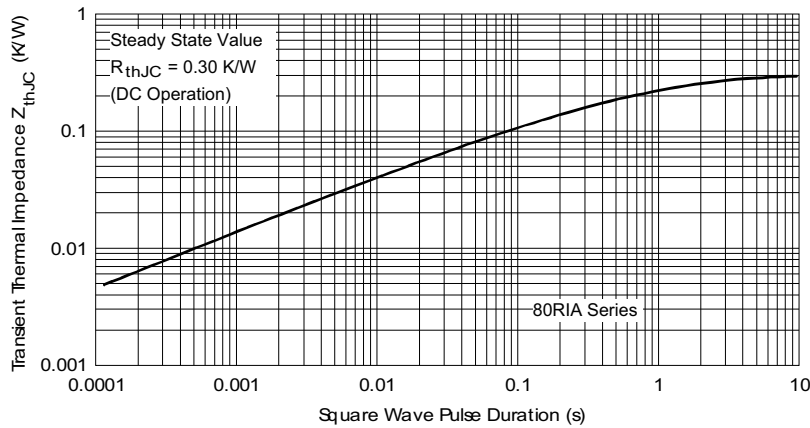


Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics

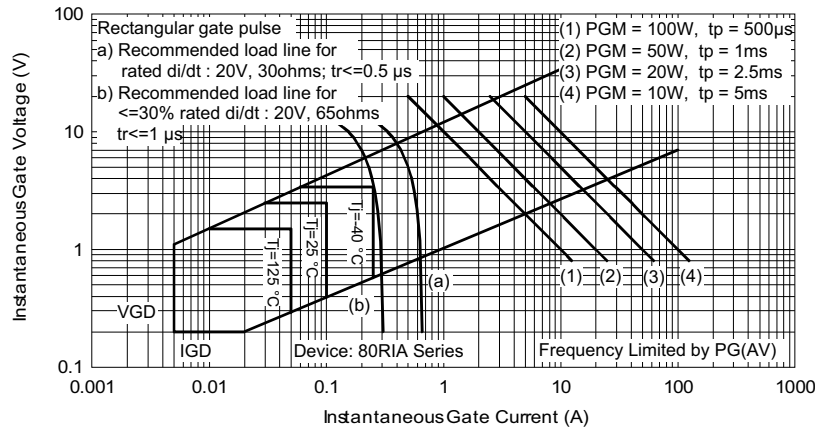


Fig. 9 - Gate Characteristics

**ORDERING INFORMATION TABLE**

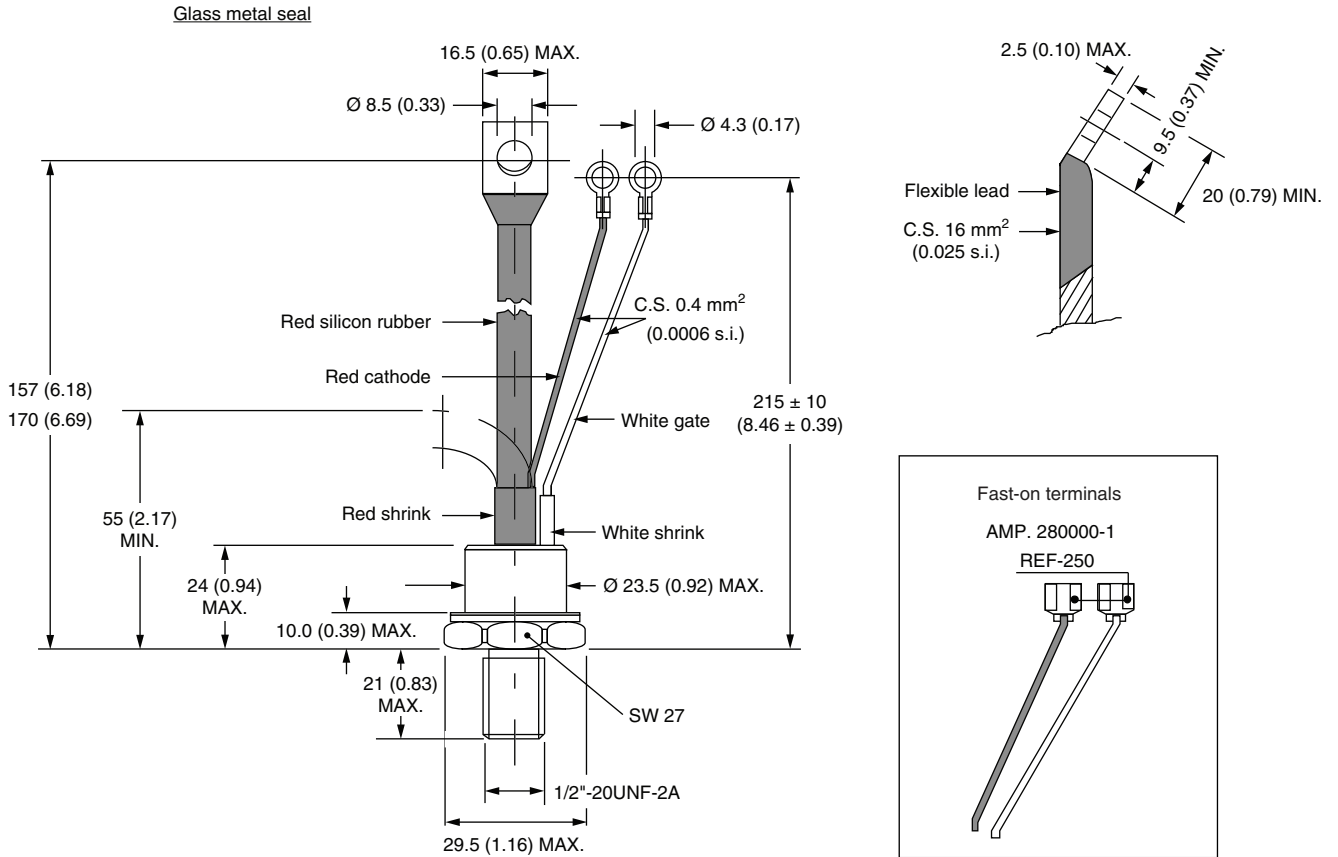
Device code	<b>VS-</b>	<b>8</b>	<b>0</b>	<b>RIA</b>	<b>120</b>	<b>M</b>	<b>PbF</b>
	(1)	(2)	(3)	(4)	(5)	(6)	(7)

- 1** - Vishay Semiconductors product
- 2** -  $I_{TAV} \times 10 \text{ A}$
- 3** -
  - 0 = Eyelet terminals (gate and auxiliary cathode leads)
  - 1 = Fast-on terminals (gate and auxiliary cathode leads)
  - 2 = Flag terminals (gate and auxiliary cathode terminals)
- 4** - RIA = Essential part number
- 5** - Voltage code  $\times 100 = V_{RRM}$  (see Voltage Ratings table)
- 6** -
  - None = Stud base 1/2"-20UNF- 2 A threads
  - M = Stud base metric threads M12 x 1.75 E 6
- 7** -
  - None = Standard production
  - PbF = Lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95362">www.vishay.com/doc?95362</a>

## TO-209AC (TO-94) for 80RIA Series

**DIMENSIONS** in millimeters (inches)





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