19-2646; Rev 3; 1/12

MAXIM

50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in WLP

General Description

The MAX4747–MAX4750 low-voltage, quad single-pole single-throw (SPST)/dual single-pole/double-throw (SPDT) analog switches operate from a single +2V to +11V supply and handle rail-to-rail analog signals. These switches exhibit low leakage current (0.1nA) and consume less than 0.5nW (typ) of quiescent power, making them ideal for battery-powered applications.

When powered from a +3V supply, these switches feature 50Ω (max) on-resistance (R_{ON}), with 3.5Ω (max) matching between channels and 9Ω (max) flatness over the specified signal range.

The MAX4747 has four normally open (NO) switches, the MAX4748 has four normally closed (NC) switches, and the MAX4749 has two NO and two NC switches. The MAX4750 has two SPDT switches. These switches are available in 14-pin TSSOP, 16-pin TQFN (4mm x 4mm), and 16-bump WLP packages. This tiny chip-scale package occupies a 2mm × 2mm area and significantly reduces the required PC board area.

Applications

Battery-Powered Systems
Audio/Video-Signal Routing
Low-Voltage Data-Acquisition Systems
Cell Phones
Communications Circuits
Glucose Meters
PDAs

Features

- **2mm × 2mm WLP**
- **Guaranteed On-Resistance (R_{ON})**
  25Ω (max) at +5V
  50Ω (max) at +3V
- **On-Resistance Matching**
  3Ω (max) at +5V
  3.5Ω (max) at +3V
- **Guaranteed < 0.1nA Leakage Current at T_A = +25°C**
- **Single-Supply Operation from +2.0V to +11V**
- **TTL/CMOS-Logic Compatible**
- **-84dB Crosstalk (1MHz)**
- **-72dB Off-Isolation (1MHz)**
- **Low Power Consumption: 0.5nW (typ)**
- **Rail-to-Rail Signal Handling**

Ordering Information

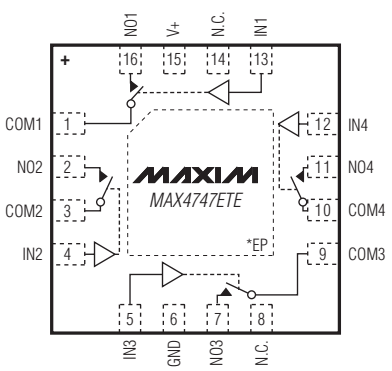
PART	TEMP RANGE	PIN-/BUMP-PACKAGE
MAX4747EUD+	-40°C to +85°C	14 TSSOP
MAX4747ETE+	-40°C to +85°C	16 Thin QFN-EP*
MAX4747EWE+T	-40°C to +85°C	16 WLP

**EP = Exposed pad.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Ordering Information continued at end of data sheet.

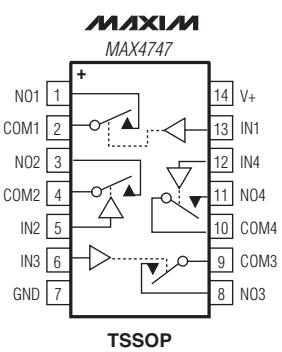
Pin/Bump Configurations/Truth Tables

TOP VIEW



TQFN

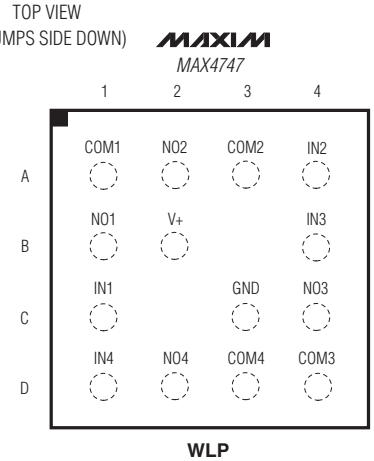
*CONNECT EP TO V+



TSSOP

INPUT	SWITCH STATE
LOW	OFF
HIGH	ON

TOP VIEW
(BUMPS SIDE DOWN)



WLP

Pin Configurations/Truth Tables continued at end of data sheet.

50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in WLP

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V+ .....-0.3V to +12V
IN_, COM_, NO_, NC_ (Note 1).....-0.3V to (V+ + 0.3V)
Continuous Current (any pin) .....±10mA
Peak Current (any pin, pulsed at 1ms, 10% duty cycle)...±20mA
Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
16-Pin Thin QFN (derate 16.9mW/°C above +70°C).....1349mW
16-Bump WLP (derate 7.3mW/°C above +70°C).....589mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Bump Temperature (soldering)
Infrared (15s) .....+220°C
Vapor Phase (60s) .....+215°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Signals on IN_, NO_, NC_, or COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = +2.7V, $I_{COM\_}$ = 5mA, $V_{NO\_}$ or $V_{NC\_}$ = +1.5V	+25°C		17	50	Ω
			T_{MIN} to T_{MAX}			60	
On-Resistance Matching Between Channels (Notes 5, 6)	ΔR_{ON}	V+ = +2.7V, $I_{COM\_}$ = 5mA, $V_{NO\_}$ or $V_{NC\_}$ = +1.5V	+25°C		0.2	3.5	Ω
			T_{MIN} to T_{MAX}			4.5	
On-Resistance Flatness (Note 7)	$R_{FLAT(ON)}$	V+ = +2.7V, $I_{COM\_}$ = 5mA, $V_{NO\_}$ or $V_{NC\_}$ = +1V, +1.5V, +2V	+25°C		2.7	9	Ω
			T_{MIN} to T_{MAX}			11	
NO_ or NC_ Off-Leakage Current (Note 8)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = +3.6V, $V_{COM\_}$ = +0.3V, +3V, $V_{NO\_}$ or $V_{NC\_}$ = +3V, +0.3V	+25°C	-0.1		+0.1	nA
			T_{MIN} to T_{MAX}	-2		+2	
COM_ Off-Leakage Current (Note 8)	$I_{COM\_(OFF)}$	V+ = +3.6V, $V_{COM\_}$ = +0.3V, +3V, $V_{NO\_}$ or $V_{NC\_}$ = +3V, +0.3V	+25°C	-0.1		+0.1	nA
			T_{MIN} to T_{MAX}	-2		+2	
COM_ On-Leakage Current (Note 8)	$I_{COM\_(ON)}$	V+ = +3.6V, $V_{COM\_}$ = +0.3V, +3.0V, $V_{NO\_}$ or $V_{NC\_}$ = +0.3V, +3V, or unconnected	+25°C	-0.2		+0.2	nA
			T_{MIN} to T_{MAX}	-4		+4	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +3V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
DYNAMIC							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = +1.5V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		57	150	ns
			T_{MIN} to T_{MAX}			170	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = +1.5V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		24	60	ns
			T_{MIN} to T_{MAX}			70	
Break-Before-Make (MAX4749/MAX4750 Only) (Note 8)	t_{BBM}	$V_{NO\_}$ or $V_{NC\_}$ = +1.5V, R_L = 300Ω, C_L = 35pF, Figure 3	+25°C		33		ns
			T_{MIN} to T_{MAX}	1			
Charge Injection	Q	V_{GEN} = 0V, R_{GEN} = 0Ω, C_L = 1.0nF, Figure 4	+25°C		7		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, 50Ω in and out	+25°C		250		MHz
Off-Isolation (Note 9)	V_{ISO}	f = 1MHz, $V_{NO\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF, Figure 5	+25°C		-72		dB
Crosstalk (Note 10)	V_{CT}	f = 1MHz, $V_{NO\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF, Figure 6	+25°C		84		dB
NO_ or NC_ Off-Capacitance	C_{OFF}	f = 1MHz, Figure 7	+25°C		20		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	f = 1MHz, Figure 7	+25°C		20		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz, Figure 7	+25°C		40		pF
LOGIC INPUT							
Input Logic High	V_{IH}			1.4			V
Input Logic Low	V_{IL}					0.8	V
Input Leakage Current	I_{IN}	$V_{IN\_}$ = 0V or V+		-1	+0.005	+1	µA
POWER SUPPLY							
Power-Supply Range	V+			2		11	V
Positive Supply Current	I+	V+ = +5.5V, $V_{IN\_}$ = 0V or V+, all switches on or off			0.0001	1	µA

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ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = +4.5V, $I_{COM\_}$ = 5mA, $V_{NO\_}$ or $V_{NC\_}$ = +3.0V	+25°C		8.2	25	Ω
			T_{MIN} to T_{MAX}			30	
On-Resistance Matching Between Channels (Notes 5, 6)	ΔR_{ON}	V+ = +4.5V, $I_{COM\_}$ = 5mA, $V_{NO\_}$ or $V_{NC\_}$ = +3.0V	+25°C		0.1	3	Ω
			T_{MIN} to T_{MAX}			4	
On-Resistance Flatness (Notes 7)	$R_{FLAT(ON)}$	V+ = +4.5V, $I_{COM\_}$ = 5mA, $V_{NO\_}$ or $V_{NC\_}$ = +1V, +2V, +3V	+25°C		2.2	5	Ω
			T_{MIN} to T_{MAX}			7	
NO_ or NC_ Off-Leakage Current (Note 8)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = +5.5V, $V_{COM\_}$ = +1V, +4.5V, $V_{NO\_}$ or $V_{NC\_}$ = +4.5V, +1V	+25°C	-0.1		+0.1	nA
			T_{MIN} to T_{MAX}	-2		+2	
COM_ Off-Leakage Current (Note 8)	$I_{COM\_(OFF)}$	V+ = +5.5V, $V_{COM\_}$ = +1V, +4.5V, $V_{NO\_}$ or $V_{NC\_}$ = +4.5V, +1V	+25°C	-0.1		+0.1	nA
			T_{MIN} to T_{MAX}	-2		+2	
COM_ On-Leakage Current (Note 8)	$I_{COM\_(ON)}$	V+ = +5.5V, $V_{COM\_}$ = +1V, +4.5V, $V_{NO\_}$ or $V_{NC\_}$ = +1V, +4.5V, or unconnected	+25°C	-0.2		+0.2	nA
			T_{MIN} to T_{MAX}	-4		+4	
DYNAMIC							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = +3.0V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		36	85	ns
			T_{MIN} to T_{MAX}			95	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = +3.0V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		19	45	ns
			T_{MIN} to T_{MAX}			55	
Break-Before-Make (MAX4749/MAX4750 Only) (Note 8)	t_{BBM}	$V_{NO\_}$ or $V_{NC\_}$ = +3.0V, R_L = 300Ω, C_L = 35pF, Figure 3	+25°C		14		ns
			T_{MIN} to T_{MAX}	1			
Charge Injection	Q	V_{GEN} = 0V, R_{GEN} = 0Ω, C_L = 1.0nF, Figure 4	+25°C		9		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, 50Ω in and out	+25°C		250		MHz
Off-Isolation (Note 9)	V_{ISO}	f = 1MHz, $V_{NO\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF, Figure 5	+25°C		-72		dB

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5V, T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Crosstalk (Note 10)	V_{CT}	f = 1MHz, $V_{NO\_}$ = 1V_{RMS}, R_L = 50Ω, C_L = 5pF, Figure 6	+25°C		-84		dB
NO_ or NC_ Off-Capacitance	C_{OFF}	f = 1MHz, Figure 7	+25°C		20		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	f = 1MHz, Figure 7	+25°C		20		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz, Figure 7	+25°C		40		pF
LOGIC INPUT							
Input Logic High	V_{IH}			2			V
Input Logic Low	V_{IL}					0.8	V
Input Leakage Current	I_{IN}	$V_{IN\_}$ = 0V or V+		-1	+0.005	+1	µA
POWER SUPPLY							
Power-Supply Range	V+			2		11	V
Positive Supply Current	I+	V+ = +5.5V, $V_{IN\_}$ = 0V or V+, all switches on or off			0.0001	1	µA

Note 3: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 4: WLP parts are 100% tested at +25°C only, and are guaranteed by design over temperature. TSSOP and Thin QFN parts are 100% tested at +85°C and guaranteed by design over temperature.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: WLP and Thin QFN on-resistance matching between channels is guaranteed by design.

Note 7: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 8: Guaranteed by design.

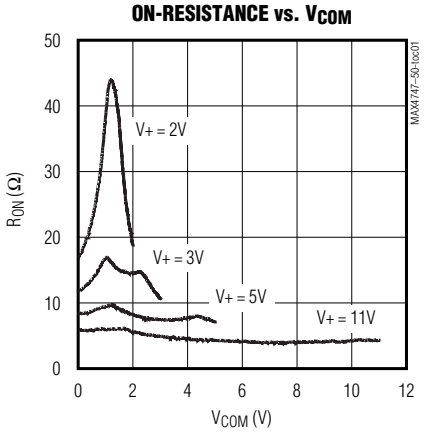
Note 9: Off-isolation = 20 $\log_{10}$ ($V_{NO\_}$/$V_{COM\_}$), $V_{NO\_}$ = output, $V_{COM\_}$ = input to off switch.

Note 10: Between any two switches.

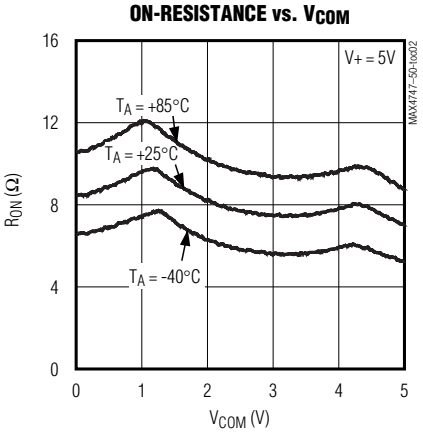
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

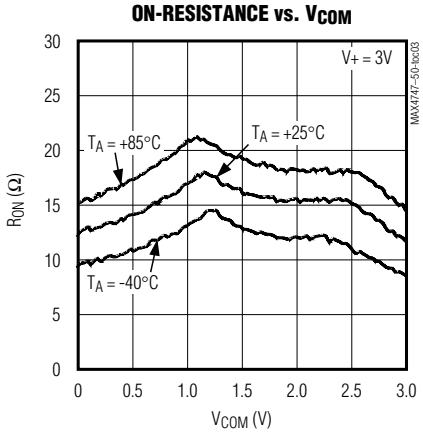
ON-RESISTANCE vs. V_{COM}



ON-RESISTANCE vs. V_{COM}



ON-RESISTANCE vs. V_{COM}

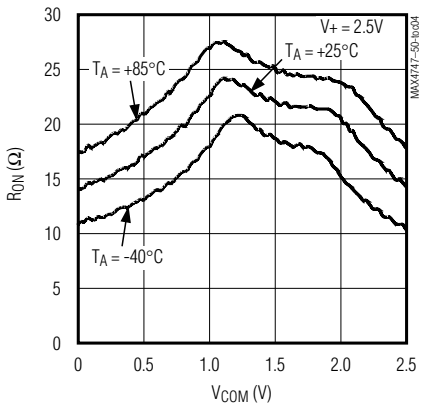


50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in WLP

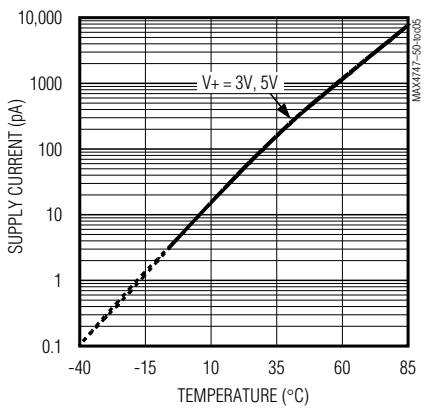
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

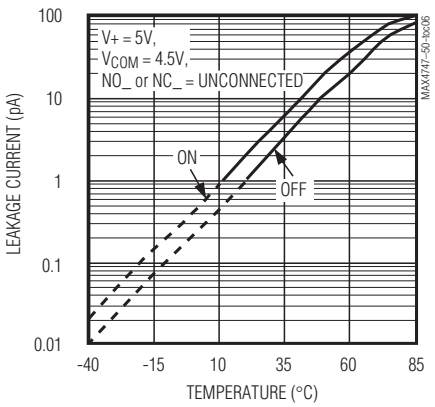
ON-RESISTANCE vs. V_{COM}



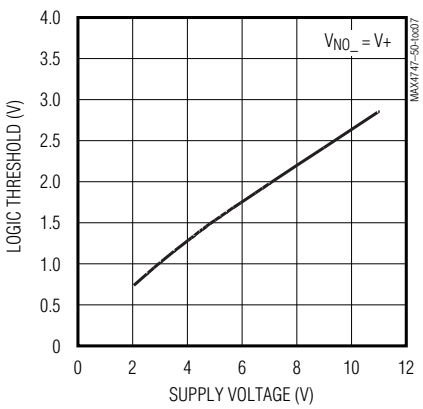
SUPPLY CURRENT vs. TEMPERATURE



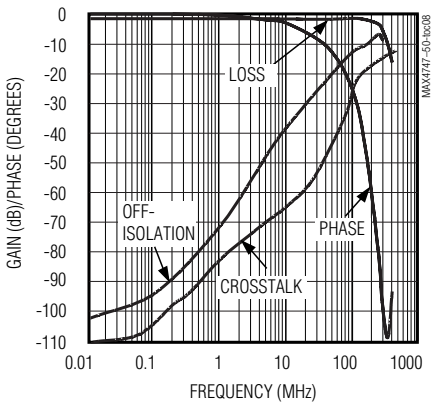
LEAKAGE vs. TEMPERATURE



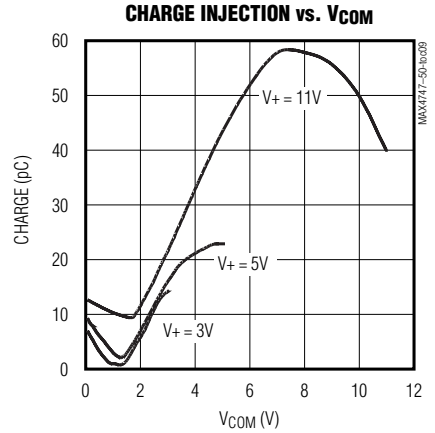
IN LOGIC THRESHOLD vs. SUPPLY VOLTAGE



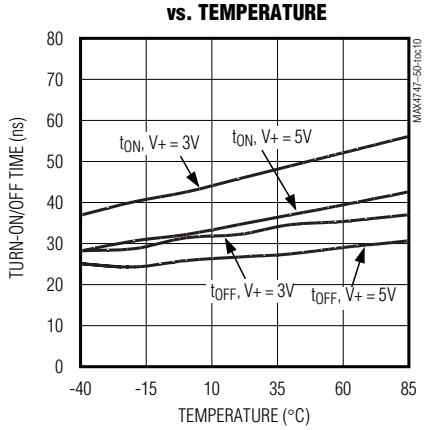
FREQUENCY RESPONSE



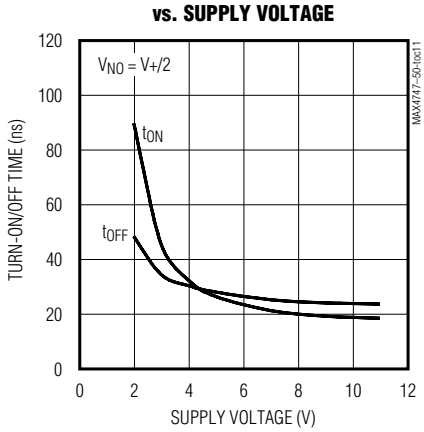
CHARGE INJECTION vs. V_{COM}



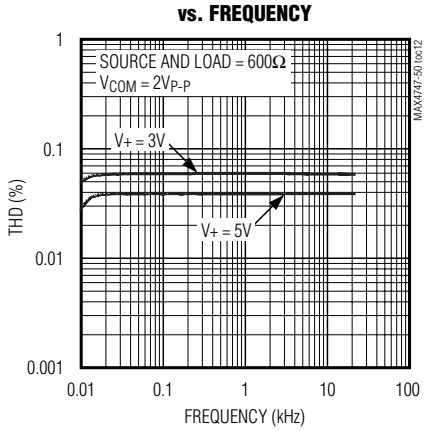
TURN-ON/OFF TIME vs. TEMPERATURE



TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description—TSSOP

PIN				NAME	FUNCTION
MAX4747	MAX4748	MAX4749	MAX4750		
1, 3, 8, 11	—	—	—	NO1–NO4	Analog-Switch Normally Open Terminals
—	1, 3, 8, 11	—	—	NC1–NC4	Analog-Switch Normally Closed Terminals
—	—	1, 8	—	NO1, NO3	Analog-Switch Normally Open Terminals
—	—	—	1, 8	NO1, NO2	Analog-Switch Normally Open Terminals
—	—	—	4, 11	NC1, NC2	Analog-Switch Normally Closed Terminals
—	—	3, 11	—	NC2, NC4	Analog-Switch Normally Closed Terminals
2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	—	COM1–COM4	Analog-Switch Common Terminal
—	—	—	2, 9	COM1, COM2	Analog-Switch Common Terminal
13, 5, 6, 12	13, 5, 6, 12	13, 5, 6, 12	—	IN1–IN4	Logic-Control Digital Input
—	—	—	13, 6	IN1, IN2	Logic-Control Digital Input
7	7	7	7	GND	Ground. Connect to digital ground.
14	14	14	14	V+	Positive Analog and Digital Supply Voltage Input. Internally connected to substrate.
—	—	—	3, 5, 10, 12	N.C.	No Connection. Not internally connected.

Bump Description—WLP

PIN				NAME	FUNCTION
MAX4747	MAX4748	MAX4749	MAX4750		
B1, A2, C4, D2	—	—	—	NO1–NO4	Analog-Switch Normally Open Terminals
—	B1, A2, C4, D2	—	—	NC1–NC4	Analog-Switch Normally Closed Terminals
—	—	B1, C4	—	NO1, NO3	Analog-Switch Normally Open Terminals
—	—	—	B1, C4	NO1, NO2	Analog-Switch Normally Open Terminals
—	—	—	A3, D2	NC1, NC2	Analog-Switch Normally Closed Terminals
—	—	A2, D2	—	NC2, NC4	Analog-Switch Normally Closed Terminals
A1, A3, D4, D3	A1, A3, D4, D3	A1, A3, D4, D3	—	COM1–COM4	Analog-Switch Common Terminal
—	—	—	A1, D4	COM1, COM2	Analog-Switch Common Terminal
C1, A4, B4, D1	C1, A4, B4, D1	C1, A4, B4, D1	—	IN1–IN4	Logic-Control Digital Input
—	—	—	C1, B4	IN1, IN2	Logic-Control Digital Input
C3	C3	C3	C3	GND	Ground. Connect to digital ground.
B2	B2	B2	B2	V+	Positive Analog and Digital Supply Voltage Input. Internally connected to substrate.
—	—	—	A2, A4, D1, D3	N.C.	No Connection. Not internally connected.

50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in WLP

Pin Description—TQFN-EP

PIN				NAME	FUNCTION
MAX4747	MAX4748	MAX4749	MAX4750		
1, 3	1, 3	1, 3	1, 9	COM1, COM2	Analog-Switch Common Terminals
2	—	—	7	NO2	Analog-Switch Normally Open Terminal
4, 13	4, 13	4, 13	5, 13	IN2, IN1	Logic-Control Digital Inputs
5, 12	5, 12	5, 12	—	IN3, IN4	Logic-Control Digital Inputs
6	6	6	6	GND	Ground. Connect to digital ground.
7	—	7	—	NO3	Analog-Switch Normally Open Terminal
8, 14	8, 14	8, 14	2, 4, 8, 10, 12, 14	N.C.	No Connection. Not internally connected.
9, 10	9, 10	9, 10	—	COM3, COM4	Analog-Switch Common Terminals
11	—	—	—	NO4	Analog-Switch Normally Open Terminal
15	15	15	15	V+	Positive Supply-Voltage Input
16	—	16	16	NO1	Analog-Switch Normally Open Terminal
—	2	2	11	NC2	Analog-Switch Normally Closed Terminal
—	7	—	—	NC3	Analog-Switch Normally Closed Terminal
—	11	11	—	NC4	Analog-Switch Normally Closed Terminal
—	16	—	3	NC1	Analog-Switch Normally Closed Terminal
—	—	—	—	EP	Exposed Pad. Connect EP to V+.

Applications Information

Operating Considerations for High-Voltage Supply

The MAX4747–MAX4750 operate to +11V with some precautions. The absolute maximum rating for V+ is +12V (referenced to GND). When operating near this region, bypass V+ with a minimum 0.1µF capacitor to ground as close to the IC as possible.

Logic Levels

The MAX4747–MAX4750 are TTL compatible when powered from a single +3V supply. When powered from other supply voltages, the logic inputs should be driven rail-to-rail. For example, with a +11V supply, IN_ should be driven low to 0V and high to 11V. With a +3.3V supply, IN_ should be driven low to 0V and high to 3.3V. Driving IN_ rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (GND to V+) pass with very little change in R_{ON} (see the *Typical Operating Characteristics*). The bidirectional switches allow NO_, NC_, and COM_ connections to be used as either inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

CAUTION: Do not exceed the absolute maximum ratings. Stresses beyond the listed ratings can cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to < 20mA, add small-signal diode D1 as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ (for D1), and to a diode drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +11V.

Test Circuits/Timing Diagrams

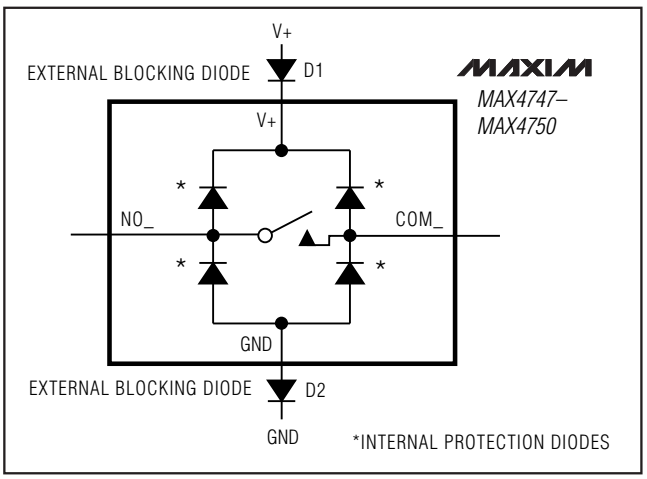


Figure 1. Overvoltage Protection Using External Blocking Diodes

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. The most significant shift occurs when using low supply voltages (+5V or less). With a +5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN_ and IN_ all the way to the supply rails (i.e., to a diode drop higher than the V+ pin, or to a diode drop lower than the GND pin) is always acceptable.

Protection diodes D1 and D2 also protect against some overvoltage situations. Using the circuit in Figure 1, no damage results if the supply voltage is below the absolute maximum rating (+12V) and if a fault voltage up to the absolute maximum rating (V+ + 0.3V) is applied to an analog signal terminal.

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and its Applications* on Maxim's web site at **www.maxim-ic.com/wlp**.

50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in WLP

Test Circuits/Timing Diagrams (continued)

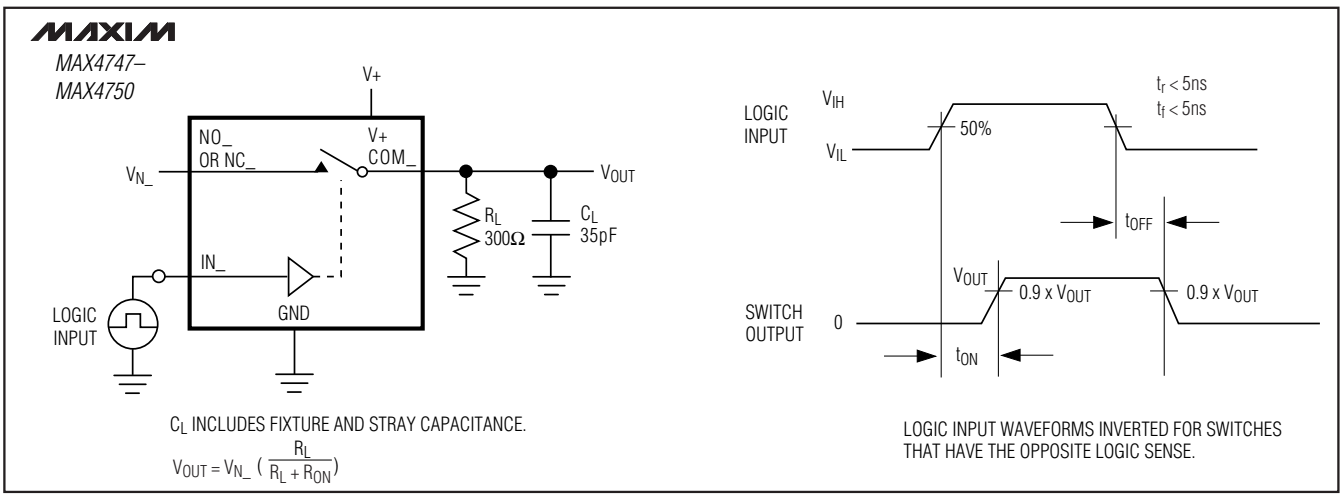


Figure 2. Switching Time

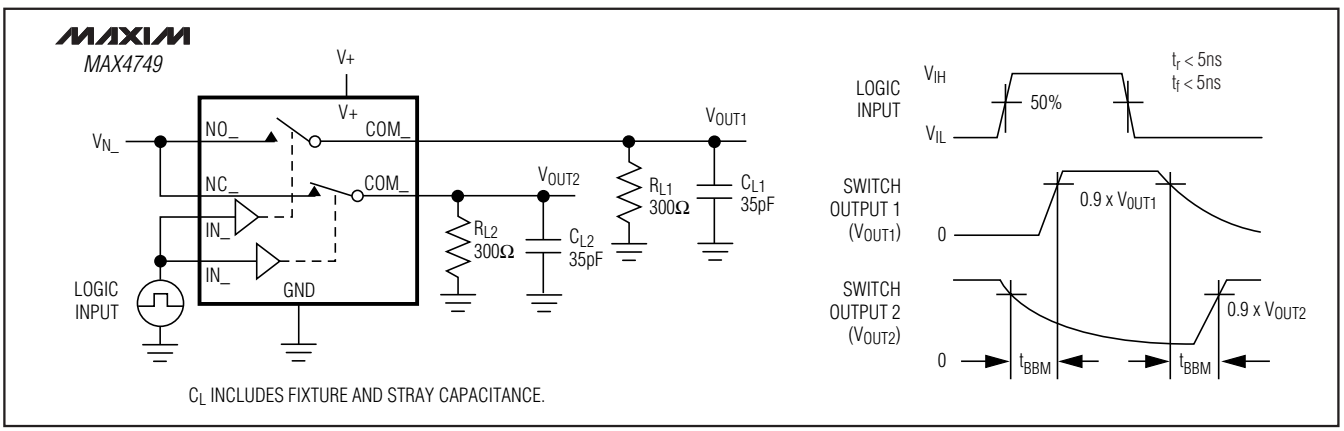


Figure 3. Break-Before-Make Interval

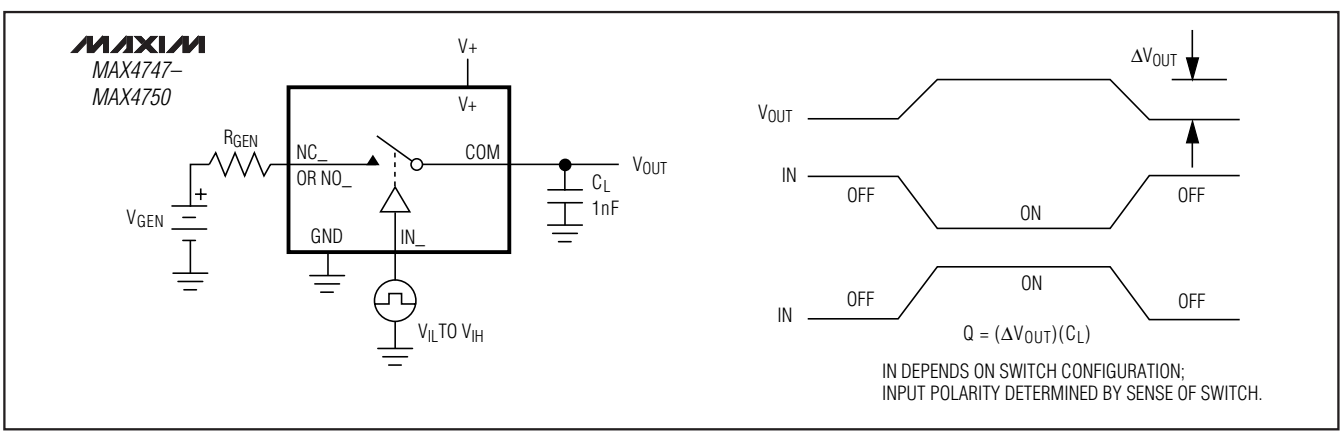


Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

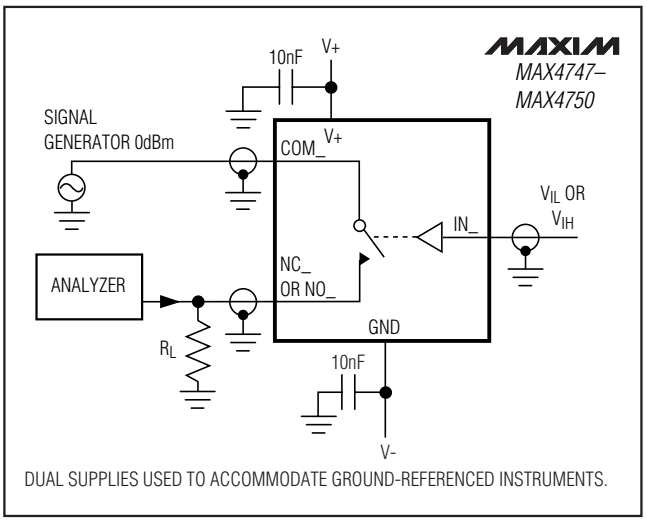


Figure 5. Off-Isolation/On-Channel Bandwidth

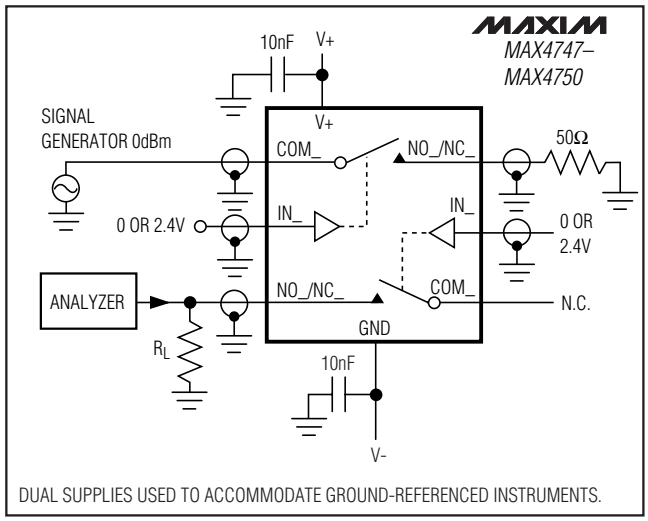


Figure 6. Crosstalk

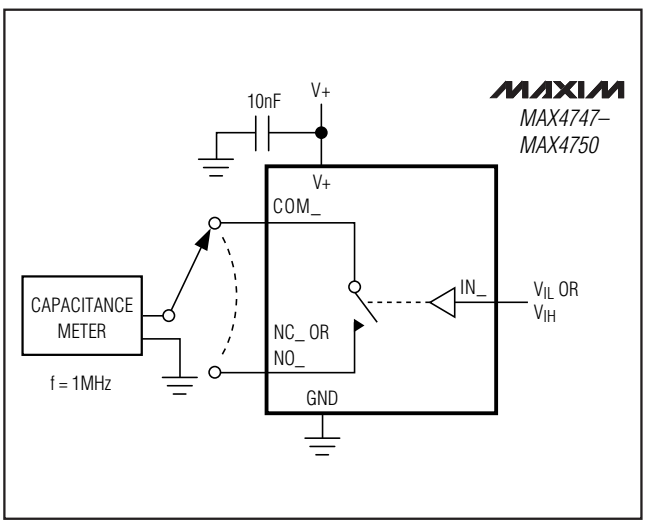


Figure 7. Channel Off-/On-Capacitance

Ordering Information (continued)

PART	TEMP RANGE	PIN-/BUMP-PACKAGE
MAX4748EUD+	-40°C to +85°C	14 TSSOP
MAX4748ETE+	-40°C to +85°C	16 Thin QFN-EP*
MAX4748EWE+T	-40°C to +85°C	16 WLP
MAX4749EUD+	-40°C to +85°C	14 TSSOP
MAX4749ETE+	-40°C to +85°C	16 Thin QFN-EP*
MAX4749EWE+T**	-40°C to +85°C	16 WLP
MAX4750EUD+	-40°C to +85°C	14 TSSOP
MAX4750ETE+	-40°C to +85°C	16 Thin QFN-EP*
MAX4750EWE+T**	-40°C to +85°C	16 WLP

**EP = Exposed pad.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

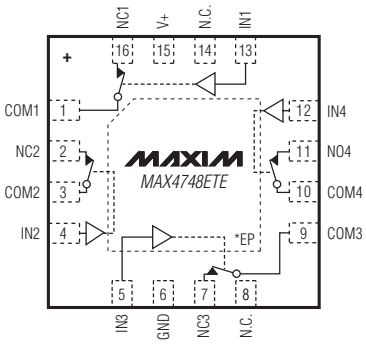
***Future products. Contact factory for availability.*

T = Tape and reel.

50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in WLP

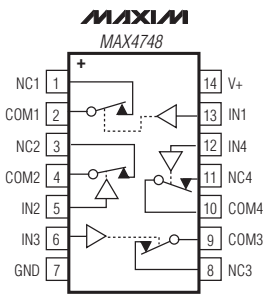
Pin/Bump Configurations/Truth Tables (continued)

TOP VIEW



TQFN

*CONNECT EP TO V+

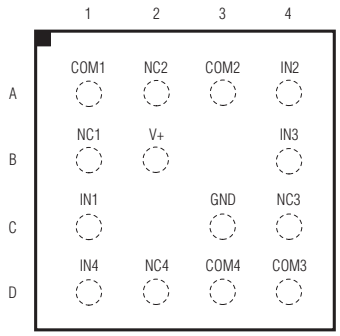


TSSOP

INPUT	SWITCH STATE
LOW	ON
HIGH	OFF

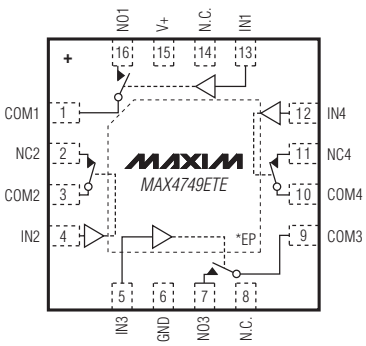
TOP VIEW
(BUMPS SIDE DOWN)

MAXIM
MAX4748



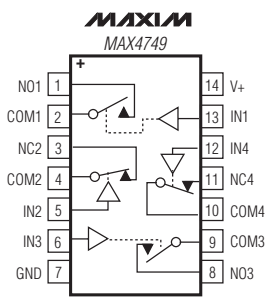
WLP

TOP VIEW



TQFN

*CONNECT EP TO V+

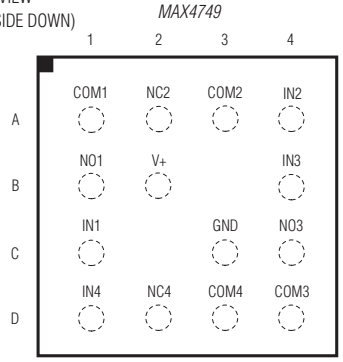


TSSOP

INPUT	NO1, NO3	NC2, NC4
LOW	OFF	ON
HIGH	ON	OFF

TOP VIEW
(BUMPS SIDE DOWN)

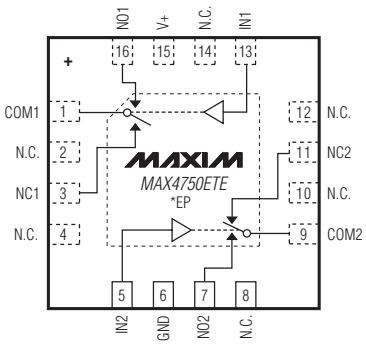
MAXIM
MAX4749



WLP

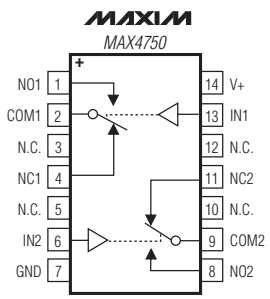
MAXIM
MAX4748

TOP VIEW



TQFN

*CONNECT EP TO V+

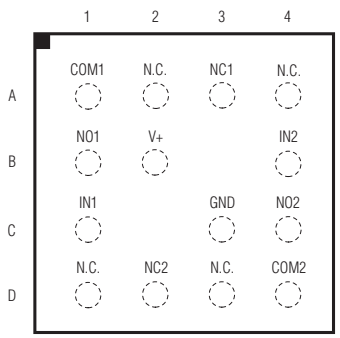


TSSOP

INPUT	NO1, NO2	NC1, NC2
LOW	OFF	ON
HIGH	ON	OFF

TOP VIEW
(BUMPS SIDE DOWN)

MAXIM
MAX4750



WLP

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TSSOP	U14+1	**21-0066**	**90-0113**
16 TQFN	T1644+4	**21-0139**	**90-0070**
16 WLP	W162D2+1	**21-0200**	Refer to **Application Note 1891**

50Ω, Low-Voltage, Quad SPST/Dual SPDT Analog Switches in WLP

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	12/06	Various changes	1-15
3	1/12	Updated UCSP to WLP packaging, corrected pin configuration, added lead-free packaging	1-9, 11-13