



### FEATURES

- ◆ Improved Electrical Performance over MAX6025
- ◆ Initial Accuracy:
  - 0.08% (max) – TS6001A
  - 0.16% (max) – TS6001B
- ◆ Temperature Coefficient:
  - 7ppm/°C (max) – TS6001A
  - 10ppm/°C (max) – TS6001B
- ◆ Quiescent Supply Current: 35µA (max)
- ◆ Low Supply Current Change with  $V_{IN}$ : 0.1µA/V
- ◆ Output Source/Sink Current: ±500µA
- ◆ Low Dropout at 500µA Load Current: 75mV
- ◆ Load Regulation: 30ppm/mA
- ◆ Line Regulation: 10ppm/V
- ◆ Stable with  $C_{LOAD}$  up to 2200pF

### APPLICATIONS

Battery-Operated Equipment  
 Data Acquisition Systems  
 Hand-Held Equipment  
 Smart Industrial Transmitters  
 Industrial and Process-Control Systems  
 Precision 3V/5V Systems  
 Hard-Disk Drives

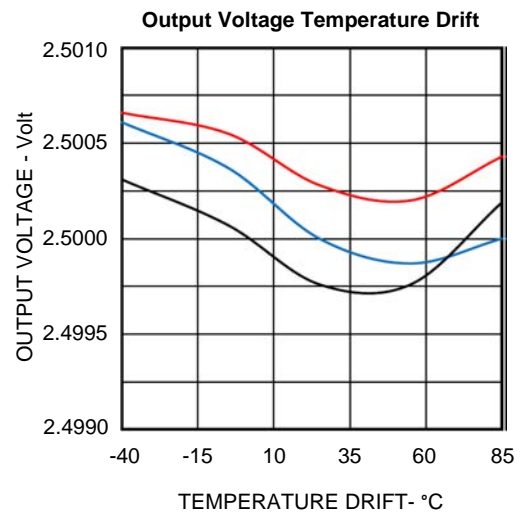
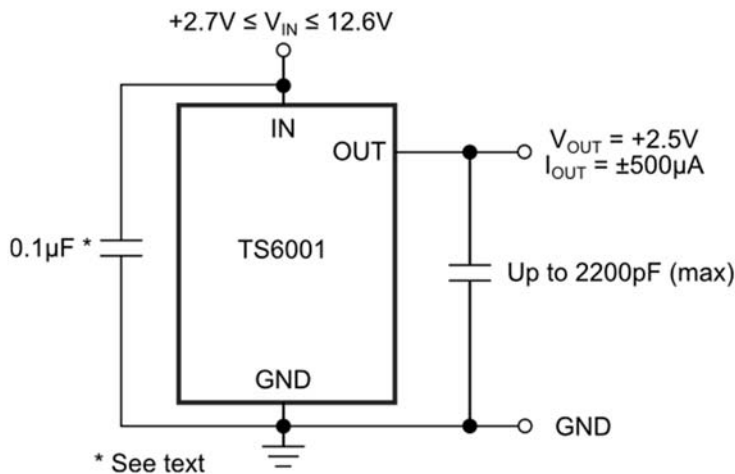
### DESCRIPTION

The TS6001 is a 3-terminal, series-mode 2.5-V precision voltage reference and is a pin-for-pin, identical to the MAX6025 voltage reference with improved electrical performance. The TS6001 consumes only 31µA of supply current at no-load, exhibits an initial output voltage accuracy of less than 0.08%, and a low output voltage temperature coefficient of 7ppm/°C. In addition, the TS6001's output stage is stable for all capacitive loads to 2200pF and is capable of sinking and sourcing load currents up to 500µA.

Since the TS6001 is a series-mode voltage reference, its supply current is not affected by changes in the applied supply voltage unlike two-terminal shunt-mode references that require an external resistor. The TS6001's small form factor and low supply current operation all combine to make it an ideal choice in low-power, precision applications.

The TS6001 is fully specified over the -40°C to +85°C temperature range and is available in a 3-pin SOT23 package.

### TYPICAL APPLICATION CIRCUIT



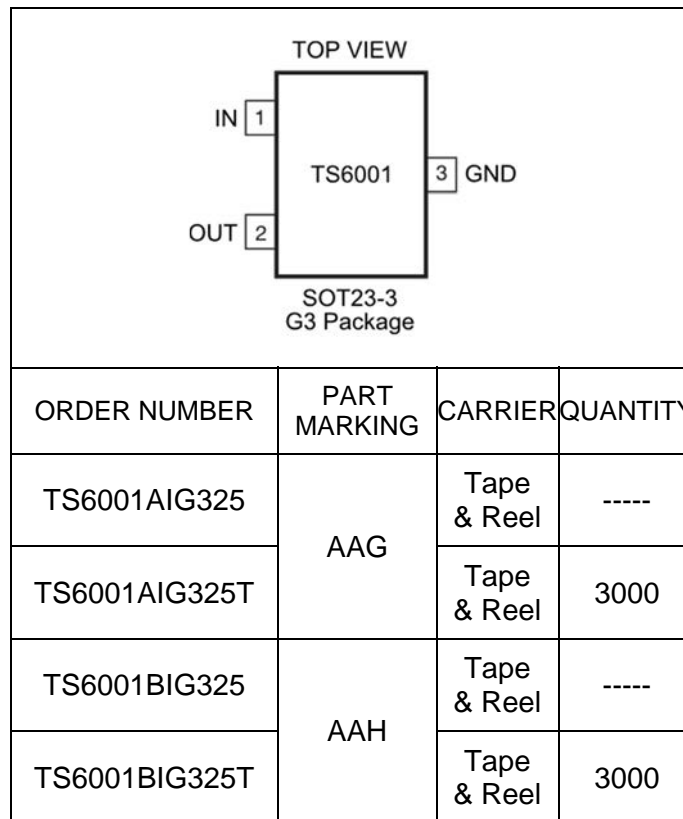
## ABSOLUTE MAXIMUM RATINGS

IN to GND..... -0.3V to +13.5V  
 OUT to GND..... -0.3V to 7V  
 Short Circuit to GND or IN ( $V_{IN} < 6V$ )..... Continuous  
 Output Short Circuit to GND or IN ( $V_{IN} \geq 6V$ ) ..... 60s  
 Continuous Power Dissipation ( $T_A = +70^\circ C$ )  
 3-Pin SOT23 (Derate at 4.0mW/°C above +70°C)..... 320mW

Operating Temperature Range..... -40°C to +85°C  
 Storage Temperature Range..... -65°C to +150°C  
 Lead Temperature (Soldering, 10s)..... +300°C

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

## PACKAGE/ORDERING INFORMATION



**Lead-free Program:** Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = +5V$ ,  $I_{OUT} = 0$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . See Note 1.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>OUTPUT</b>							
Output Voltage	$V_{OUT}$	$T_A = +25^\circ C$	TS6001A	2.498	2.500	2.502	V
				-0.08		0.08	%
			TS6001B	2.496	2.500	2.504	V
				-0.16		0.16	%
Output Voltage Temperature Coefficient (See Note 2)	$TCV_{OUT}$	$0^\circ C \leq T_A \leq +85^\circ C$	TS6001A		2	7	ppm/ $^\circ C$
		$-40^\circ C \leq T_A \leq +85^\circ C$			2.5	10	
		$0^\circ C \leq T_A \leq +85^\circ C$	TS6001B		3	10	
		$-40^\circ C \leq T_A \leq +85^\circ C$			4	15	
Line Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	$(V_{OUT} + 0.2V) \leq V_{IN} \leq 12.6V$		10	30	ppm/V	
Load Regulation	$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	Sourcing	$0 \leq I_{OUT} \leq 500\mu A$		30	240	ppm/mA
		Sinking	$-500\mu A \leq I_{OUT} \leq 0$		70	320	
Dropout Voltage (See Note 3)	$V_{IN} - V_{OUT}$	$I_{OUT} = 500\mu A$		75	150	mV	
OUT Short-Circuit Current	$I_{SC}$	$V_{OUT}$ Short to GND		4		mA	
		$V_{OUT}$ Short to IN		4			
Temperature Hysteresis (See Note 4)				100		ppm	
Long-Term Stability (See Note 5)	$\Delta V_{OUT}/\text{time}$	168hr at $T_A = +25^\circ C$		75		ppm/168hr	
<b>DYNAMIC</b>							
Noise Voltage	$e_{OUT}$	$f = 0.1\text{Hz to }10\text{Hz}$		50		$\mu V_{P-P}$	
		$f = 10\text{Hz to }10\text{kHz}$		75		$\mu V_{RMS}$	
Ripple Rejection	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{IN} = 5V \pm 100\text{mV}$ , $f = 120\text{Hz}$		82		dB	
Turn-On Settling Time	$t_R$	To $V_{OUT} = 0.1\%$ of final value, $C_{OUT} = 50\text{pF}$		340		$\mu s$	
Capacitive-Load Stability Range	$C_{OUT}$	See Note 6	0		2200	pF	
<b>INPUT</b>							
Supply Voltage Range	$V_{IN}$	Guaranteed by line-regulation test	$V_{OUT} + 0.2$		12.6	V	
Quiescent Supply Current	$I_{IN}$			31	35	$\mu A$	
Change in Supply Current	$I_{IN}/V_{IN}$	$(V_{OUT} + 0.2V) \leq V_{IN} \leq 12.6V$		0.1	2	$\mu A/V$	

**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ C$  and are guaranteed by characterization for  $T_A = T_{MIN}$  to  $T_{MAX}$ , as specified.

**Note 2:** Temperature Coefficient is measured by the "box" method; i.e., the maximum  $\Delta V_{OUT}$  is divided by the maximum  $\Delta T$ .

**Note 3:** Dropout voltage is the minimum input voltage at which  $V_{OUT}$  changes  $\leq 0.2\%$  from  $V_{OUT}$  at  $V_{IN} = 5.0V$ .

**Note 4:** Temperature hysteresis is defined as the change in the  $+25^\circ C$  output voltage before and after cycling the device from  $+25^\circ C$  to  $T_{MIN}$  to  $+25^\circ C$  and from  $+25^\circ C$  to  $T_{MAX}$  to  $+25^\circ C$ .

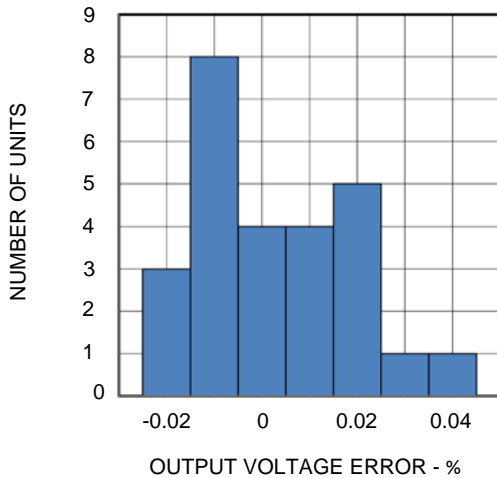
**Note 5:** Reference long-term drift or stability listed in the table is an intermediate result of a 1000-hour evaluation. Soldered onto a printed circuit board (pcb), voltage references exhibit more drift early in the evaluation because of assembly-induced differential stresses between the package and the pcb.

**Note 6:** Not production tested; guaranteed by design.

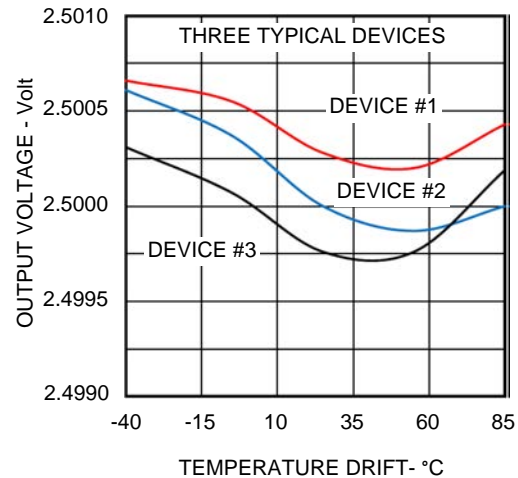
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = +5V$ ;  $I_{OUT} = 0mA$ ;  $T_A = +25^{\circ}C$ , unless otherwise noted.

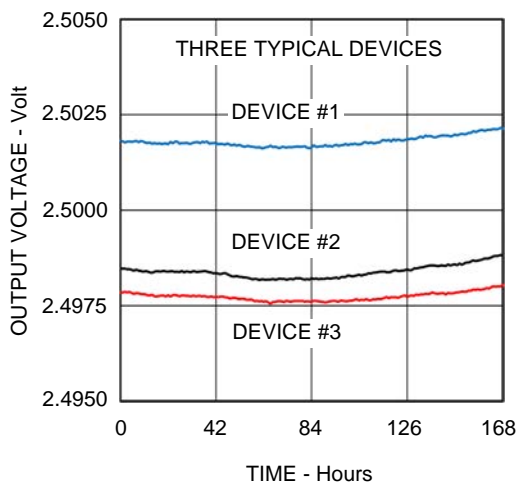
**Output Voltage Histogram**



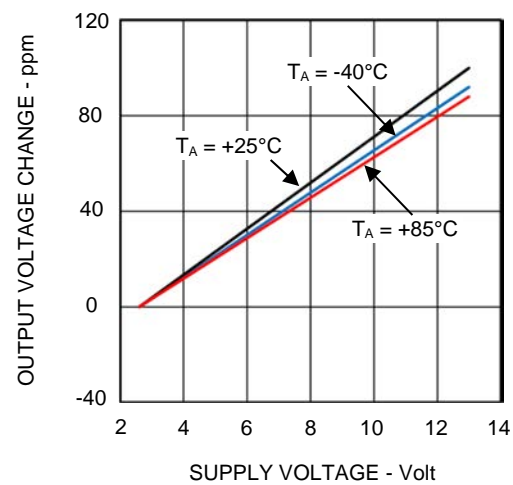
**Output Voltage Temperature Drift**



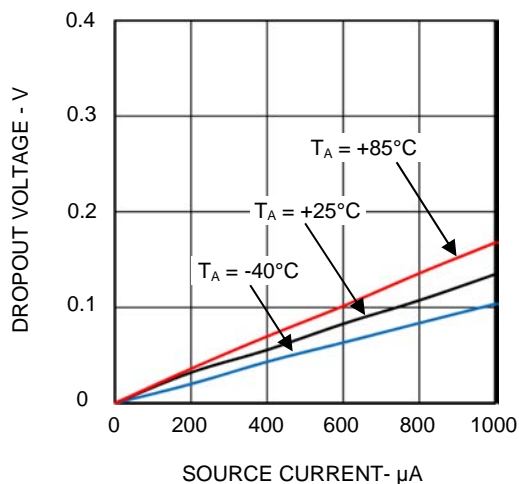
**Long-Term Output Voltage Drift**



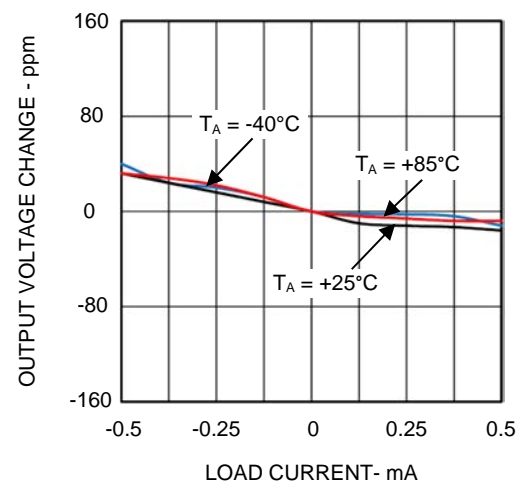
**Line Regulation**



**Dropout Voltage vs Source Current**



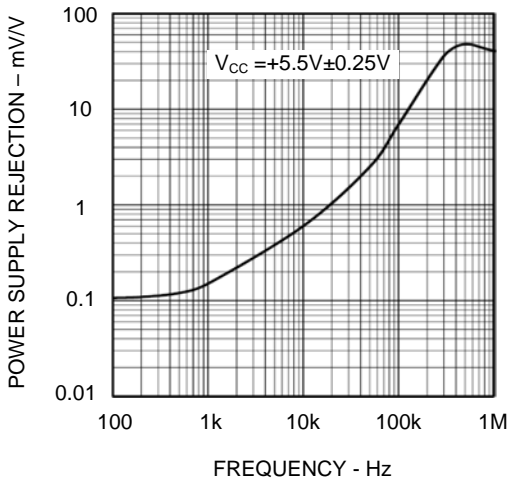
**Load Regulation**



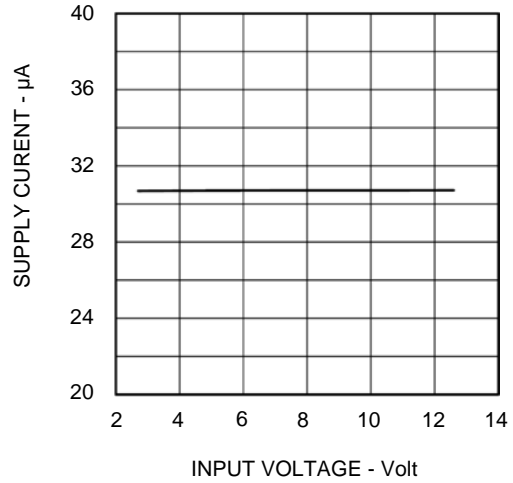
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = +5V$ ;  $I_{OUT} = 0mA$ ;  $T_A = +25^{\circ}C$ , unless otherwise noted.

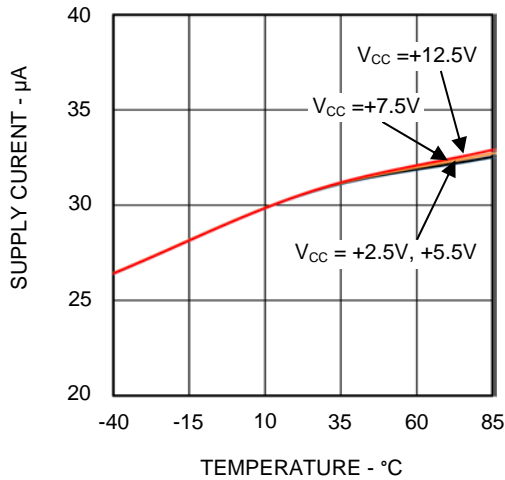
**Power Supply Rejection vs Frequency**



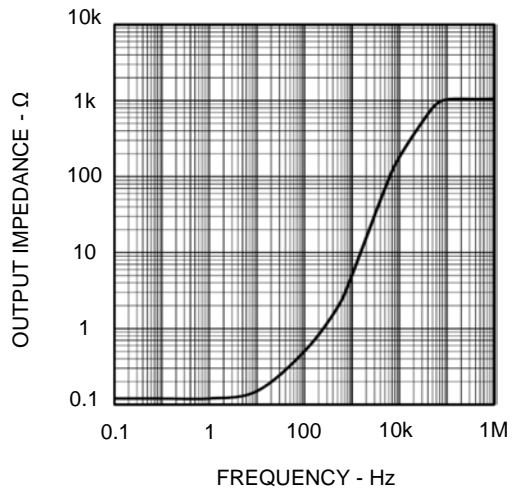
**Supply Current vs Input Voltage**



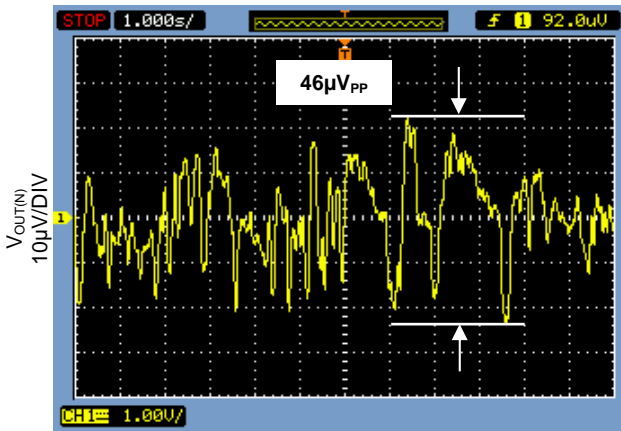
**Supply Current vs Temperature**



**Output Impedance vs Frequency**

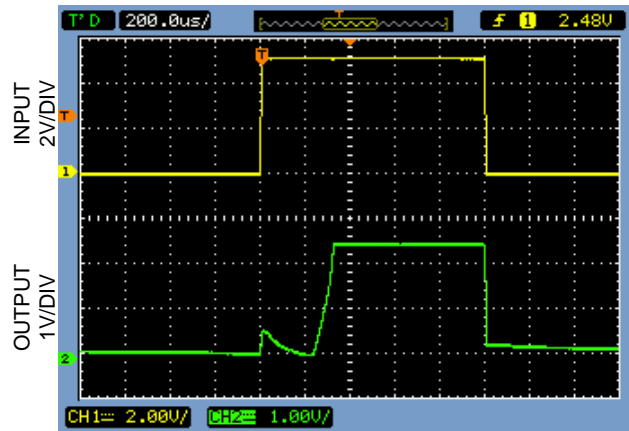


**0.1Hz to 10Hz Output Noise**



1s/DIV

**Power-On Transient Response**

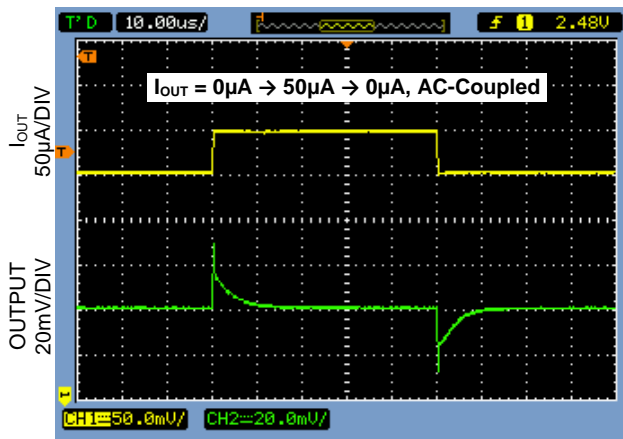


200  $\mu s/DIV$

## TYPICAL PERFORMANCE CHARACTERISTICS

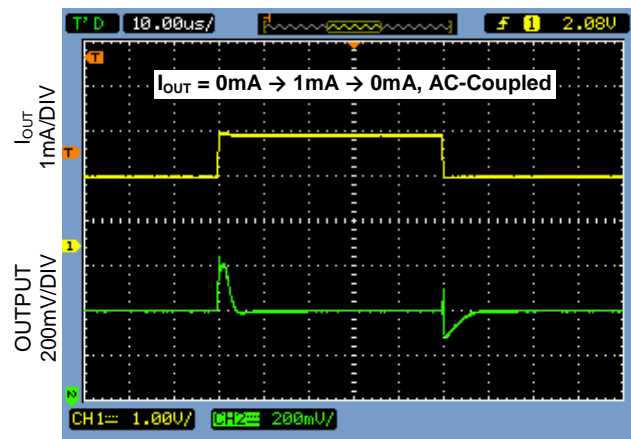
$V_{IN} = +5V$ ;  $I_{OUT} = 0mA$ ;  $T_A = +25^{\circ}C$ , unless otherwise noted.

### Small-signal Load Transient Response



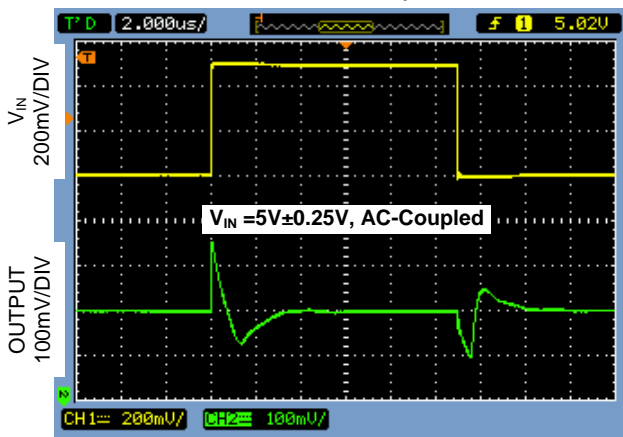
10 $\mu s/DIV$

### Large-signal Load Transient Response



10 $\mu s/DIV$

### Line Transient Response



2 $\mu s/DIV$



### PIN FUNCTIONS

PIN	NAME	FUNCTION
1	IN	Supply Voltage Input
2	OUT	+2.5V Output
3	GND	Ground

### DESCRIPTION/THEORY OF OPERATION

The TS6001 incorporates a precision 1.25-V bandgap reference that is followed by an output amplifier configured to amplify the base bandgap output voltage to a 2.5-V output. The design of the bandgap reference incorporates proprietary circuit design techniques to achieve its low temperature coefficient of 7ppm/°C and initial output voltage

accuracy less than 0.08%. The design of the output amplifier’s frequency compensation does not require a separate compensation capacitor and is stable with capacitive loads up to 2200pF. The design of the output amplifier also incorporates low headroom design as it can source and sink load currents to 500µA with a dropout voltage less than 100mV.

### APPLICATIONS INFORMATION

#### Power Supply Input Bypass Capacitance

If there are other analog ICs within 1 to 2 inches of the TS6001 with their own bypass capacitors to GND, the TS6001 would not then require its own bypass capacitor. If this is not the case, then it is considered good analog circuit engineering practice to place a 0.1µF ceramic capacitor in as close proximity to the TS6001 as practical with very short pcb track lengths.

#### Output/Load Capacitance Considerations

As mentioned previously, the TS6001 does not require a separate, external capacitor at V<sub>OUT</sub> for transient response stability as it is stable for

capacitive loads up to 2200pF. For improved load regulation transient response, the use of a capacitor at V<sub>OUT</sub> helps to reduce output voltage overshoot/undershoot to transient load current conditions. Figure 1 illustrates the TS6001’s transient load regulation performance with C<sub>LOAD</sub> = 0pF to a 50-µA transient upon a 175-µA steady-state load current. Peak transients are approximately 20mV and the TS6001 settles in less than 8µs. As shown in Figure 2, adding a capacitive load reduces peak transients at the expense of settling time. In this case, the TS6001’s output was loaded with C<sub>LOAD</sub> = 1000pF and subjected to the same transient load current profile. Peak transients were reduced to less than 10mV and the TS6001 settled in less than 10µs.

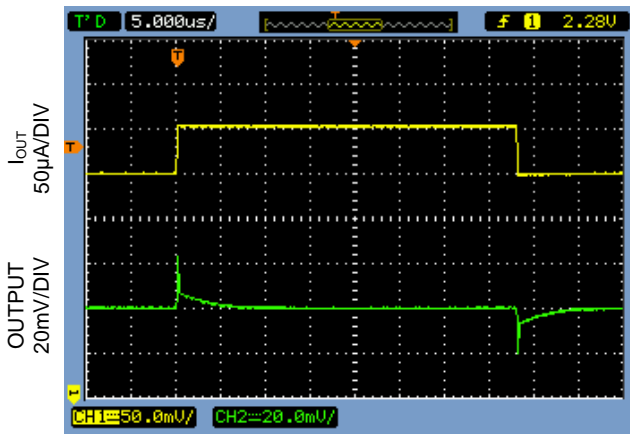


Figure 1: TS6001 Transient Load Regulation Response, C<sub>LOAD</sub> = 0pF

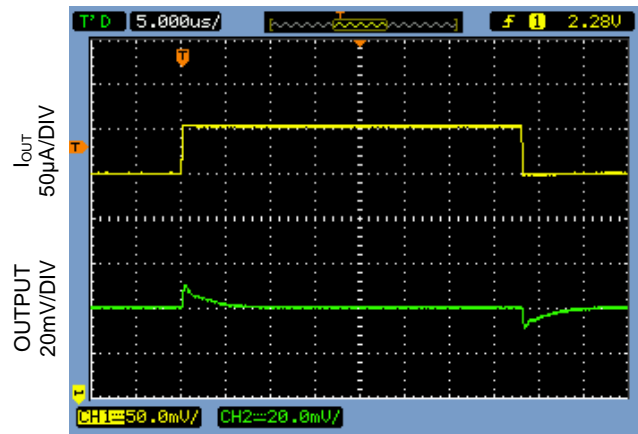


Figure 2: TS6001 Transient Load Regulation Response, C<sub>LOAD</sub> = 1000pF

## Supply Current

The TS6001 exhibits excellent dc line regulation as its supply current changes slightly as a function of the applied supply voltage. Because of a unique bias loop design, the change in its supply current as a function of supply voltage (its  $\Delta I_{IN}/\Delta V_{IN}$ ) is less than  $0.1\mu A/V$ . Since the TS6001 is a series-mode reference, load current is drawn from the supply voltage only when required. In this case, circuit efficiency is maintained at all applied supply voltages. Reducing power dissipation and extending battery life are the net benefits of improved circuit efficiency.

When the applied supply voltage is less than the minimum specified input voltage of the TS6001 (for example, during the power-up or “cold-start” transition), the TS6001 performs an internal calibration routine and can draw up to  $200\mu A$  above its nominal, steady-state supply current. This internal calibration sequence also dominates the TS6001’s turn-on time. To ensure reliable power-up behavior, the input power source must have sufficient reserve power to provide the extra supply current drawn during the power-up transition.

## Voltage Reference Turn-On Time

With a  $(V_{IN} - V_{OUT})$  voltage differential larger than  $200mV$  and  $I_{LOAD} = 0mA$ , the TS6001’s typical combined turn-on and settling time to within  $0.1\%$  of its  $2.5V$  final value is approximately  $340\mu s$ .

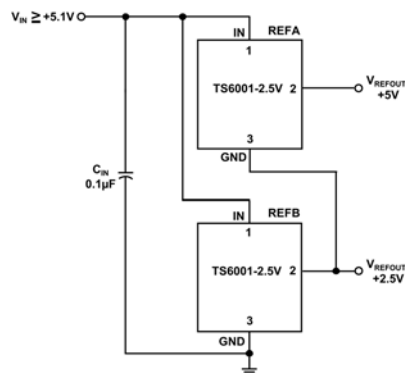
## Output Voltage Hysteresis

Reference output voltage thermal hysteresis is the change in the reference’s  $+25^{\circ}C$  output voltage after temperature cycling from  $+25^{\circ}C$  to  $+85^{\circ}C$  to  $+25^{\circ}C$  and from  $+25^{\circ}C$  to  $-40^{\circ}C$  to  $+25^{\circ}C$ . Thermal hysteresis is caused by differential package stress impressed upon the TS6001’s internal bandgap core transistors and depends on whether the reference IC was previously at a higher or lower temperature. At  $100ppm$ , the TS6001’s typical temperature hysteresis is equal to  $0.25mV$  with respect to a  $2.5V$  output voltage.

## Connecting Two or More TS6001s in Stacked $V_{OUT}$ Arrangements

In many applications, it is desired to combine the outputs of two or more precision voltage references, especially if the combined output voltage is not available or is an uncommon output voltage. One such technique for combining (or “stacking”) the

outputs of precision voltage references is illustrated in Figure 3.



**Figure 3:** Connecting Two TS6001-2.5s in a Stacked  $V_{REFOUT}$  Arrangement

In this example and powered by an unregulated supply voltage ( $V_{IN} \geq +5.2V$ ), two TS6001-2.5 precision voltage references are used. The GND terminal of REFA is connected to the OUT terminal of REFB. This connection produces two output voltages,  $V_{REFOUT1}$  and  $V_{REFOUT2}$ , where  $V_{REFOUT1}$  is the terminal voltage of REFB and  $V_{REFOUT2}$  is  $V_{REFOUT1}$  plus the OUT terminal voltage of REFA. By implementing this stacked arrangement with a pair of TS6001-2.5s,  $V_{REFOUT2}$  is  $5V$  and  $V_{REFOUT1}$  is  $2.5V$ .

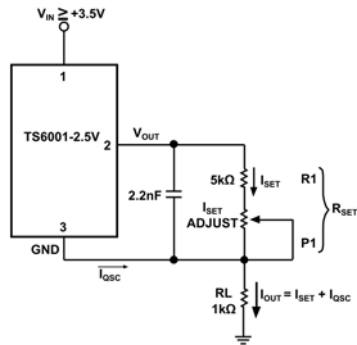
Although the TS6001-2.5s do not specifically require input bypass capacitors, it is good engineering practice to bypass both references from  $V_{IN}$  to the global GND terminal (at REFB). If either or both reference ICs are required to drive a load capacitance, it is also good engineering practice to route the load capacitor’s return lead to each reference’s corresponding REF’s GND terminal. The circuit’s minimum input supply voltage,  $V_{IN}$ , is determined by  $V_{REFOUT2}$  and REFB’s dropout voltage ( $75mV$ , typically).

## How to Configure the TS6001 into a General-Purpose Current Source

In many low-voltage applications, a general-purpose current source is needed with very good line regulation. The TS6001-2.5 can be configured as a grounded-load, floating current source as shown Figure 4. In this example, the TS6001-2.5’s output voltage is bootstrapped across an external resistor ( $R1 + P1$ ) which, in turn, sets the output current. The circuit’s total output current is  $I_{OUT} = I_{SET} + I_{QSC}$  where  $I_{QSC}$  is the TS6001 supply current (up to  $35\mu A$ ). For



improved output current accuracy,  $I_{SET}$  should be at least 10 times  $I_{QSC}$ .



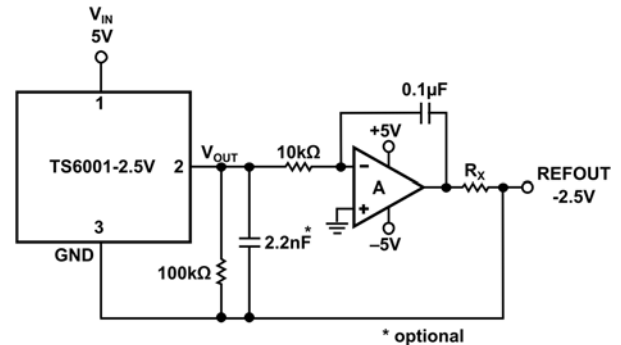
**Figure 4:** A Low-power, General-Purpose Current Source.

### A Negative, Precision Voltage Reference without Precision Resistors

When using current-output DACs, it is oftentimes desired that the polarity of the output signal voltage is the same as the external reference voltage. There are two conventional techniques used to accomplish this objective: a) inverting the full-scale DAC output voltage or b) converting a current-output DAC into a voltage-switching DAC. In the first technique, an op amp and pair of precision resistors would be required because the DAC's output signal voltage requires re-inversion to match the polarity of the external reference voltage. The second technique is a bit more involved and requires converting the current-output DAC into a voltage-switching DAC by driving the DAC's  $V_{REF}$  and  $I_{OUT}$  terminals in reverse. Additional components required are two precision resistors, an op amp, and an external voltage reference, typically a 1.25-V reference. If the 1.25-V full-scale output voltage requires scaling to a 2.5-V or a 5-V full scale, then a second op amp and pair of precision resistors would be necessary to perform the amplification.

To avoid the need for either re-inversion of the current-switching DAC's output voltage or amplifying the voltage-switching DAC's output voltage, it would then be desired to apply a negative voltage reference to the original current-switching DAC. In general, any positive voltage reference can be converted into a negative voltage reference using pair of matched resistors and an op amp configured for inverting mode operation. The disadvantage to this approach is that the largest single source of error in the circuit is the relative matching of the resistors used.

The circuit illustrated in Figure 5 avoids the need for multiple op amps and well-matched resistors by using an active integrator circuit. In this circuit, the voltage reference's output is used as the input signal to the integrator. Because of op amp loop action, the integrator adjusts its output voltage to establish the correct relationship between the reference's OUT and GND terminals ( $=V_{REF}$ ). In other words, the output voltage polarity of the integrator stage is opposite that of the reference's output voltage.



**Figure 5:** How to Convert a  $V_{REF}$  to a  $-V_{REF}$  without Precision Resistors.

The 2200pF capacitor at the output of the TS6001 is optional and the resistor in series with the output of the op amp should be empirically determined based on the amplifier choice and whether the amplifier is required to drive a large capacitive load.

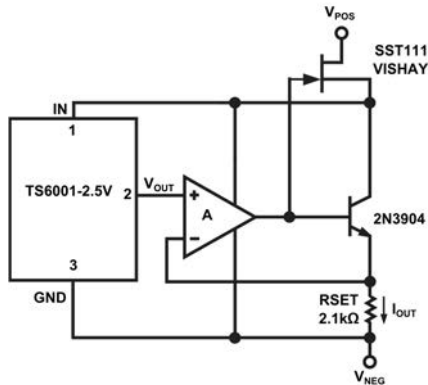
Rail-to-rail output op amps used for the integrator stage work best in this application; however, these types of op amps require a finite amount of headroom (in the millivolt range) when sinking load current. Therefore, good engineering judgment is always recommended when selecting the most appropriate negative supply for the circuit.

### How to Use the TS6001 in a High-Input Voltage Floating Current Source

By adopting the technique previously shown in Figure 2, the basic floating current source circuit can be adapted to operate at much higher supply voltages beyond the supply voltage rating of the TS6001-2.5 by adding a discrete n-channel JFET. As shown in Figure 6, the JFET acts as a supply voltage regulator since its source voltage will always be 2.5V higher than  $V_{SY}$ . The circuit minimizes reference IC self-heating because the JFET and the 2N3904 NPN transistor carry the load current. This circuit can operate up to +35V and is determined by the  $BV_{DS}$  breakdown voltage of the external JFET.

For example, if  $V_{SY}$  is 0V, then the upper input supply voltage level for the circuit is 35V. With a 2.1k $\Omega$  load and the TS6001's supply current of 35 $\mu$ A (max), this circuit supplies approximately a 1.23-mA current to the load.

excellent load regulation while sourcing load currents up to 150mA. If the application circuit is designed to operate across a wide temperature range, it is recommended that circuit performance is thoroughly evaluated across the PNP transistor's beta ( $\beta$ , or current gain) distribution. When the PNP transistor's current gain is a minimum, the increase in base current must be absorbed by the TS6001 for a given load current. For higher output load currents, higher output power PNP transistors can be used so long as good thermal management techniques are applied and transistor current-gain vs ambient temperature behavior is evaluated.

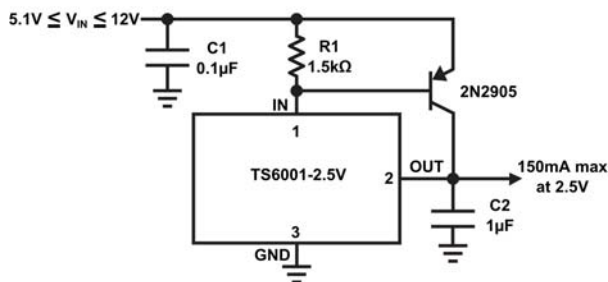


**Figure 6:** Using the TS6001-2.5 in a High-Input Voltage Floating Current Source.

In many current source applications, the possibility of an output short-circuit condition - whether transient or sustained - exists. It is recommended to test thoroughly for either scenario to prevent the possibility that the TS6001 would be exposed to a total voltage from its IN terminal to GND terminal higher than its absolute maximum rating of 13.5V.

### Boosting the TS6001's Output Current Drive

While the TS6001 is capable of sourcing up to 500 $\mu$ A with excellent load regulation, there are applications where tight load regulation is required at much higher output load currents. By adding a general-purpose, industry-standard PNP transistor and one resistor to the TS6001's basic configuration as shown in Figure 7, increasing a precision



**Figure 7:** Boosting the TS6001's Output Current with an External PNP Transistor.

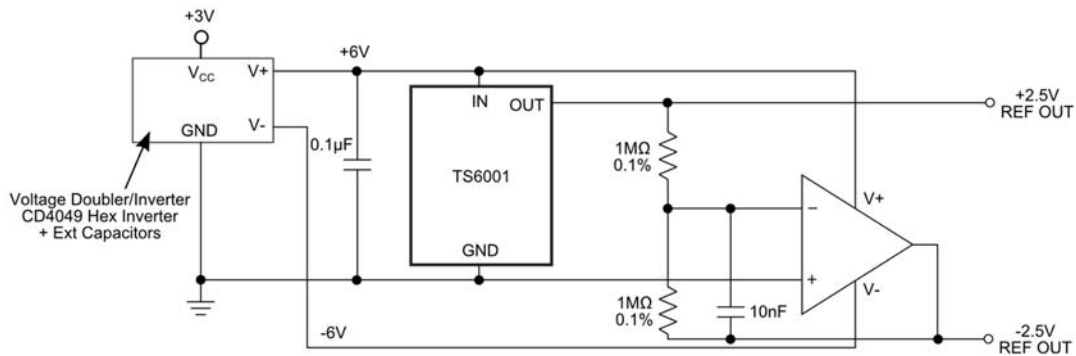
reference's output source current drive is straightforward. Using a 2N2905 PNP transistor and a 1.5k $\Omega$  resistor, the TS6001 is able to maintain



## Generating Positive and Negative Low-Power Voltage References

The circuit in Figure 8 uses a CD4049 hex inverter and a few external capacitors as the power supply to a dual-supply precision op amp to form a  $\pm 2.5V$  precision, bipolar output voltage reference around

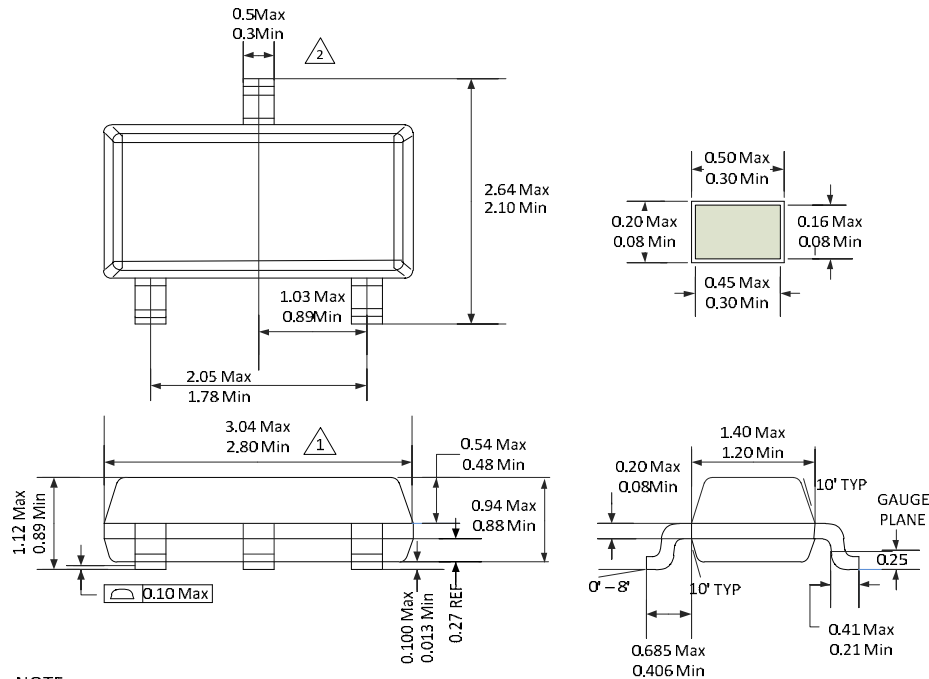
the TS6001. The CD4049-based circuit is a discrete charge pump voltage doubler/inverter that generates  $\pm 6V$  supplies for any precision, micropower op amp with  $V_{OS}$  and  $TCV_{OS}$  specifications consistent with the TS6001's initial accuracy and output voltage drift performance.



**Figure 8:** Generating Positive and Negative 2.5V References from a Single  $+3V$  or  $+5V$  Supply.

## PACKAGE OUTLINE DRAWING

### 3-Pin SOT23 Package Outline Drawing (N.B., Drawings are not to scale)



**NOTE:**

- 1 Does not include mode flash, protrusions or gate burns. Mode flash, protrusions or gate burns shall not exceed 0.127 mm per side
- 2 Does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.127 mm per side.
- 3. Die is facing up for mold die and trim-form.
- 4. Lead span/stand of high/coplanarity are considered as special characteristic.
- 5. All specifications referd JEDEC TO-236AB except for lead length dimension.
- 6. Controlling dimension in (mm)

**Patent Notice**

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.  
Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.



Smart.  
Connected.  
Energy-Friendly



**Products**  
[www.silabs.com/products](http://www.silabs.com/products)



**Quality**  
[www.silabs.com/quality](http://www.silabs.com/quality)



**Support and Community**  
[community.silabs.com](http://community.silabs.com)

#### Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

#### Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOmodem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
USA

<http://www.silabs.com>