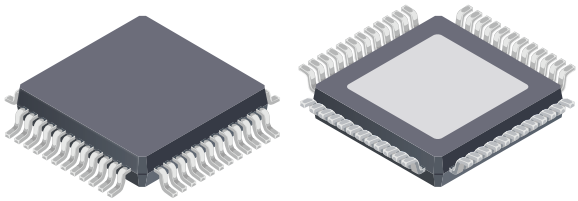
Automotive 3-Phase MOSFET Driver

Features and Benefits

- High-current 3-phase gate drive for N-channel MOSFETs
- 3-phase current sense amplifiers
- SPI-compatible serial or direct parallel control
- Cross-conduction protection
- Programmable dead time
- Top-off charge pump for 100% PWM
- Uncommitted buffer amplifier
- 5.5 to 50 V supply voltage range
- CMOS inputs, 3.3 to 5 V logic supply
- Extensive diagnostics output
- Low-current sleep mode

PACKAGE:

48-pin LQFP with exposed thermal pad (suffix JP)



Not to scale

Description

The A4910 is a three-phase controller for use with N-channel external power MOSFETs and is specifically designed for automotive applications.

A unique charge-pump regulator provides full (>10 V) gate drive for battery voltages down to 7 V, and allows the A4910 to operate with a reduced gate drive down to 5.5 V.

A bootstrap capacitor is used to provide the above battery supply voltage required for N-channel MOSFETs. An internal charge pump for the high-side drive allows DC (100% duty cycle) operation.

Full control over all six power MOSFETs in the 3-phase bridge is provided, allowing motors to be driven with block commutation or sinusoidal excitation. The power MOSFETs are protected from shoot-through by integrated crossover control and programmable dead time.

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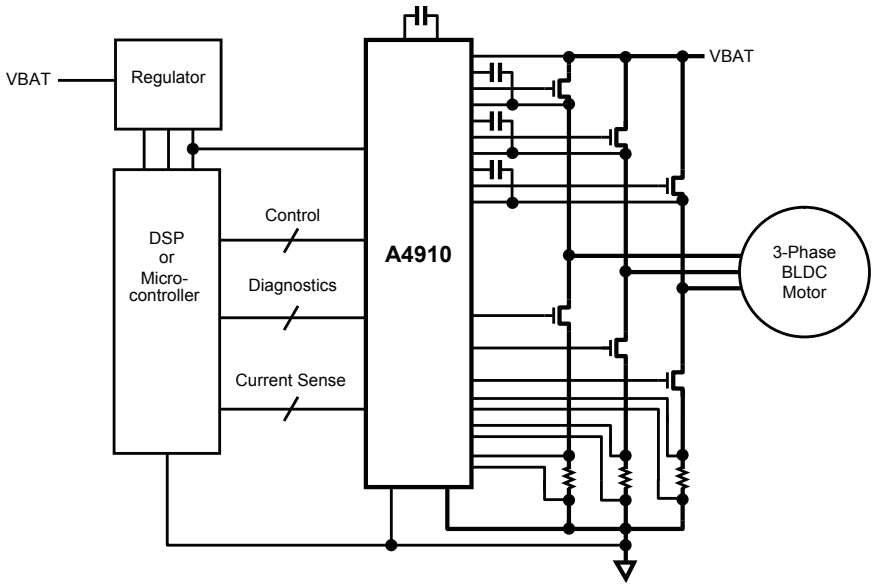
Applications

- Electronic power steering (EPS, EHPS, EAS)
- Hydraulic pumps
- Engine cooling fan
- Gearbox actuator

Typical Application Drawing



Description (continued)

Current in each half bridge can be measured using integrated current sense amplifiers. These are three user-configurable differential amplifiers, with below-ground common-mode range and excellent transient response and settling time, allowing them to be used in low-side current-sense applications.

Integrated diagnostics provide indication of undervoltage, overtemperature, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions. Detailed diagnostics are available as a serial data word.

The A4910 is supplied in a small footprint (81 mm^2) 48-pin LQFP with exposed thermal pad (suffix JP). It is lead (Pb) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Package	Packing*
A4910KJPTR-T	1500 pieces per 13-in. reel	7 mm × 7 mm, 1.6 mm nominal height LQFP with exposed thermal pad

*Contact Allegro™ for additional packing options.

ABSOLUTE MAXIMUM RATINGS with respect to AGND, PGND connected directly to AGND

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 50	V
Logic Supply Voltage	V_{DD}		–0.3 to 6	V
Terminal VREG	V_{REG}		–0.3 to 16	V
Terminal CP1	V_{CP1}		–0.3 to 16	V
Terminal CP2	V_{CP2}		V_{CP1} – 0.3 to V_{REG} + 0.3	V
Logic Inputs		STRn, SDI, SCK, RESETn, COASTn, xHI, and xLO terminals	–0.3 to 6	V
Logic Outputs		SDO, and DIAG terminals	–0.3 to V_{DD} + 0.3	V
Sense Amplifier Inputs		CSAP, CSAM, CSBP, CSBM, CSCP, and CSCM terminals	–4 to 6.5	V
Sense Amplifier Outputs		CSAO, CSBO, and CSCO terminals	–0.3 to V_{DD} + 0.3	V
Operational Amplifier Inputs		OPAP and OPAM terminals	–0.3 to 6.5	V
Operational Amplifier Outputs		OPAO terminals	–0.3 to V_{DD} + 0.3	V
Terminal VBRG	V_{BRG}		–5 to 55	V
Terminals CA, CB, and CC [1]	V_{Cx}		–0.3 to V_{REG} + 50	V
Terminals GHA, GHB, and GHC [2]	V_{GHx}		V_{Cx} – 16 to V_{Cx} + 0.3	V
Terminals SA, SB, and SC [2]	V_{Sx}		V_{Cx} – 16 to V_{Cx} + 0.3	V
Terminals GLA, GLB, and GLC	V_{GLx}		V_{REG} – 16 to 18	V
Terminals LSSA, LSSB, and LSSC	V_{LSSx}		V_{REG} – 16 to 18	V
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Junction Temperature	T_J(max)	Continuous	150	°C
		Overtemperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, determined by design characterization	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] For example, at V_{REG} = 13 V the most positive rating is 13 V + 50 V = 63 V, while at V_{REG} = 8 V the most positive rating is 8 V + 50 V = 58 V.
[2] For example, at V_{REG} = 13 V the most negative rating is V_{Cx} – 16 V = –0.3 V – 16 V = –16.3 V, and the most positive rating is V_{Cx} + 0.3 V = V_{REG} + 50 V + 0.3 V = 13 V + 50 V + 0.3 V = 63.3 V. If V_{REG} = 8 V, the most negative rating remains at –16.3 V, and the most positive rating is 58.3 V.

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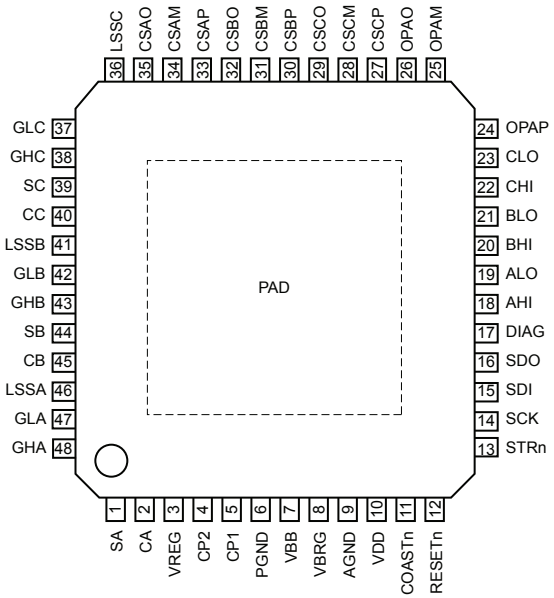
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Power Dissipation section

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	23	°C/W
		On 2-layer PCB with 3 in.^{2} of copper area each side	44	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W

*Additional thermal information available on the Allegro website.

Pinout Diagram

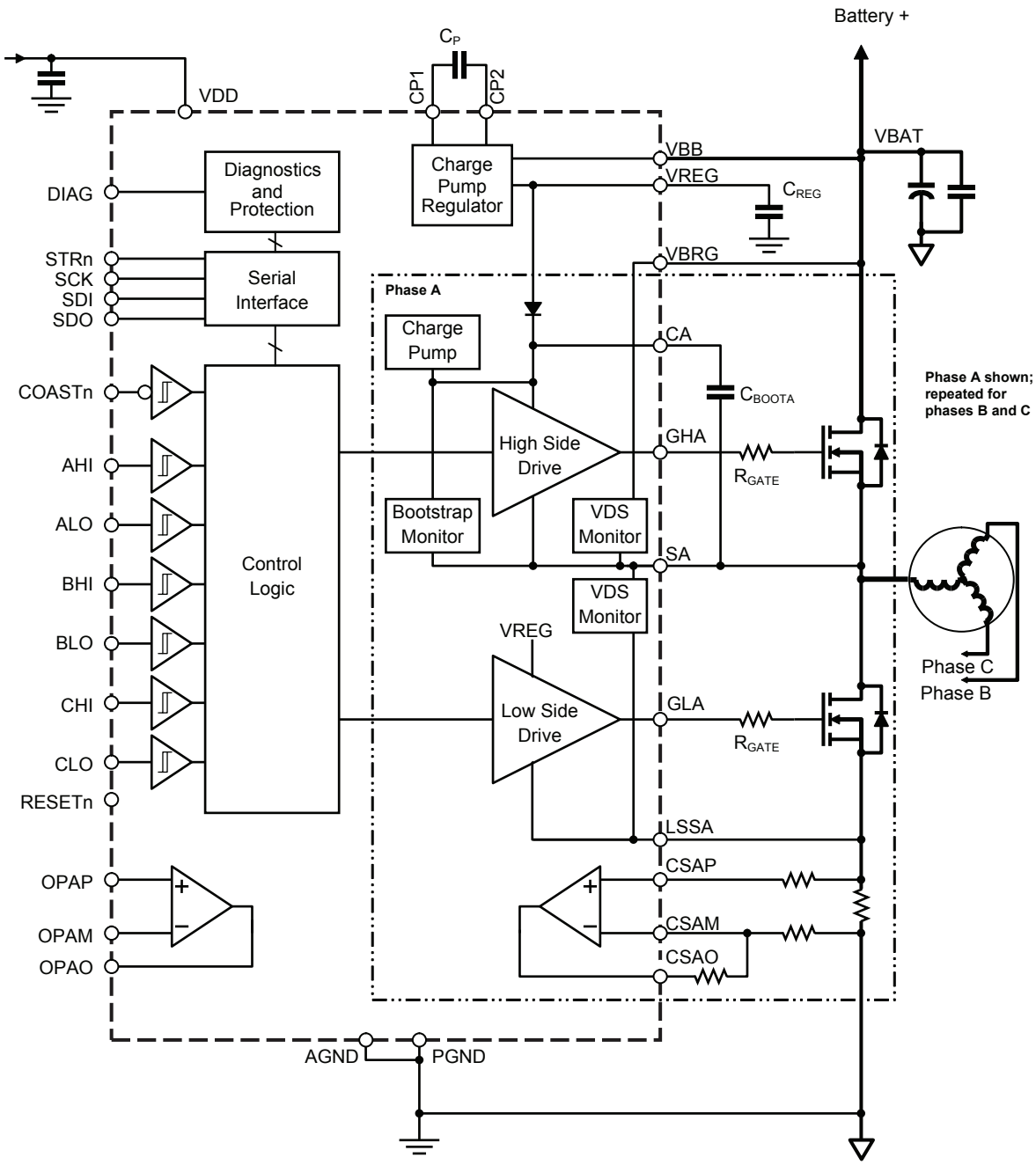


Terminal List Table

Name	Number	Function
AGND	9	Analog ground
AHI	18	Control input high side, phase A
ALO	19	Control input low side, phase A
BHI	20	Control input high side, phase B
BLO	21	Control input low side, phase B
CA	2	Bootstrap capacitor, phase A
CB	45	Bootstrap capacitor, phase B
CC	40	Bootstrap capacitor, phase C
CHI	22	Control input high side, phase C
CLO	23	Control input low side, phase C
COASTn	11	Coast input
CP1	5	Pump capacitor
CP2	4	Pump capacitor
CSAM	34	Current sense input –, phase A
CSAO	35	Current sense output, phase A
CSAP	33	Current sense input +, phase A
CSBM	31	Current sense input –, phase B
CSBO	32	Current sense output, phase B
CSBP	30	Current sense input +, phase B
CSCM	28	Current sense input –, phase C
CSCO	29	Current sense output, phase C
CSCP	27	Current sense input +, phase C
DIAG	17	Programmable diagnostic output
GHA	48	High-side gate drive, phase A
GHB	43	High-side gate drive, phase B

Name	Number	Function
GHC	38	High-side gate drive, phase C
GLA	47	Low-side gate drive, phase A
GLB	42	Low-side gate drive, phase B
GLC	37	Low-side gate drive, phase C
LSSA	46	Low-side source, phase A
LSSB	41	Low-side source, phase B
LSSC	36	Low-side source, phase C
OPAM	25	Operational amplifier input –
OPAO	26	Operational amplifier output
OPAP	24	Operational amplifier input +
PAD	–	Exposed thermal pad
PGND	6	Power ground
RESETn	12	Standby mode control
SA	1	Motor connection, phase A
SB	44	Motor connection, phase B
SC	39	Motor connection, phase C
SCK	14	Serial clock input
SDI	15	Serial data input
SDO	16	Serial data output
STRn	13	Serial strobe (chip select) input
VBB	7	Main power supply
VBRG	8	High-side drain voltage sense
VDD	10	Logic supply
VREG	3	Gate drive supply output

Functional Block Diagram



ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{DD} = 5 V, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
VBB Functional Operating Range	V_{BB}		5.5	–	50	V
VBB Quiescent Current	I_{BBQ}	RESETn = high, outputs low, V_{BB} = 12 V	–	10	14	mA
	I_{BBS}	RESETn = low, sleep mode, V_{BB} = 12 V	–	–	10	µA
VDD Logic Supply	V_{DD}		3.0	–	5.5	V
VDD Quiescent Current	I_{DDQ}	RESETn = high, outputs low	–	10	13	mA
	I_{DDS}	RESETn = low, sleep mode	–	–	10	µA
VREG Output Voltage	V_{REG}	V_{BB} > 9 V, I_{REG} = 0 to 30 mA	9	13	13.8	V
		7.5 V < V_{BB} ≤ 9 V, I_{REG} = 0 to 20 mA	9	13	13.8	V
		6 V < V_{BB} ≤ 7.5 V, I_{REG} = 0 to 15 mA	7.9	–	–	V
		5.5 V < V_{BB} ≤ 6 V, I_{REG} < 9 mA	7.9	9.5	–	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA	0.4	0.7	1.0	V
		I_D = 100 mA	1.5	2.2	2.8	V
Bootstrap Diode Resistance	r_D	$r_{D(100\ mA)} = (V_{fBOOT(150\ mA)} - V_{fBOOT(50mA)})/100\ mA$	6	11	22	Ω
Bootstrap Diode Current Limit	I_{DBOOT}		250	500	750	mA
Top-Off Charge Pump Current Limit	I_{TOCPM}		–	100	–	µA
High-Side Gate Drive Static Load Resistance	R_{GSH}		250	–	–	kΩ
System Clock Period	t_{OSC}		45	50	55	ns
GATE OUTPUT DRIVE						
Turn-On Time	t_r	C_{LOAD} = 10 nF, 20% to 80% points	–	190	–	ns
Turn-Off Time	t_f	C_{LOAD} = 10 nF, 80% to 20% points	–	120	–	ns
Pull-Up On-Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GHx} = –150 mA	5	8	11	Ω
		T_J = 150°C, I_{GHx} = –150 mA	10	15	20	Ω
Pull-Down On-Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GLx} = 150 mA	1.7	2.5	3.1	Ω
		T_J = 150°C, I_{GLx} = 150 mA	2.9	4	5	Ω
GHx Output Voltage (High)	V_{GHH}	Bootstrap capacitor fully charged	V_{Cx} – 0.2	–	–	V
GHx Output Voltage (Low)	V_{GHL}	–10 µA < I_{GHx} < 10 µA	–	–	V_{Sx} + 0.3	V
GLx Output Voltage (High)	V_{GLH}		V_{REG} – 0.2	–	–	V
GLx Output Voltage (Low)	V_{GLL}	–10 µA < I_{GLx} < 10 µA	–	–	V_{LSSx} + 0.3	V
GHx Passive Pull-Down	R_{GHPD}	V_{BB} = 0 V, V_{GHx} – V_{Sx} < 0.1 V	–	950	–	kΩ
		V_{BB} = 0 V, I_{GHx} = 500 µA	–	4	–	kΩ
GLx Passive Pull-Down	R_{GLPD}	V_{BB} = 0 V, V_{GLx} – V_{LSSx} < 0.1 V	–	950	–	kΩ
		V_{BB} = 0 V, I_{GLx} = 500 µA	–	4	–	kΩ

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{DD} = 5 V, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE (continued)						
Turn-Off Propagation Delay	$t_{P(off)}$	Input change to unloaded gate output change (see figure 5)	60	90	140	ns
Turn-On Propagation Delay	$t_{P(on)}$	Input change to unloaded gate output change (see figure 5)	50	80	130	ns
Propagation Delay Matching (Phase-to-Phase)	Δt_{PP}	Same phase change, DT[6..0] = 0	–	5	15	ns
Propagation Delay Matching (On-to-Off)	Δt_{OO}	Single phase, DT[6..0] = 0	–	15	30	ns
Propagation Delay Matching (GHx-to-GLx)	Δt_{HL}	Rising to rising edges, falling to falling edges, DT[6..0] = 0	–	–	20	ns
LOGIC INPUTS AND OUTPUTS						
Input Low Voltage	V_{IL}	RESETn pin	–	–	0.2 × V_{DD}	V
		All other logic pins	–	–	0.3 × V_{DD}	V
Input High Voltage	V_{IH}		0.7 × V_{DD}	–	–	V
Input Hysteresis	V_{Ihys}	RESETn pin	200	350	–	mV
		All other logic pins	250	500	–	mV
Input Pull-Up Resistor	R_{PU}	STRn	30	50	70	kΩ
Input Pull-Down Resistor	R_{PD}	COASTn, RESETn, SCK, SDI, AHI, ALO, BHI, BLO, CHI, and CLO pins	30	50	70	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	–	0.2	0.4	V
Output High Voltage[1]	V_{OH}	I_{OL} = –1 mA	V_{DD} – 0.4	V_{DD} – 0.2	–	V
Output Leakage (SDO pin)[1]	I_{SDOlkg}	0 V < V_{SDO} < V_{DD}, STRn = 1	–1	–	1	µA
LOGIC INPUTS AND OUTPUTS DYNAMIC PARAMETERS						
Reset Pulse Width	t_{RST}		0.2	–	4.5	µs
Reset Shutdown Time	t_{RSD}		10	–	–	µs
Clock High Time	t_{SCKH}	A in Figure 2	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 2	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 2	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 2	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 2	300	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 2	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 2	–	–	30	ns
Data Out Valid Time from Clock Falling	t_{SDOV}	H in Figure 2	–	–	40	ns
Data Out Hold Time from Clock Falling	t_{SDOH}	I in Figure 2	5	–	–	ns

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{DD} = 5 V, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS AND OUTPUTS DYNAMIC PARAMETERS (continued)						
Data In Set-Up Time to Clock Rising	t_{SDIS}	J in Figure 2	15	–	–	ns
Data In Hold Time from Clock Rising	t_{SDIH}	K in Figure 2	10	–	–	ns
Wake Up from Reset	t_{EN}	RESETn high to POR bit set	–	–	1	ms
CURRENT SENSE AMPLIFIERS[2] (refer to Figure 1 for definitions)						
Input Offset Voltage	$V_{IOS(SA)}$		–10	–	+10	mV
Input Offset Voltage Drift[3]	$\Delta V_{IOS(SA)}$		–	±10	–	µV/°C
Input Bias Current[1]	$I_{BIAS(SA)}$	0 V < V_P < V_{DD}, 0 V < V_M < V_{DD}	–1	0	+1	µA
Input Offset Current[1]	$I_{OS(SA)}$	V_{ID} = 0 V, V_{CM}in range	–1	–	+1	µA
Input Common-Mode Range (DC)	$V_{CM(SA)}$	V_{ID} = 0 V	–1	–	2	V
Differential Input Voltage	$V_{ID(SA)}$		–	–	200	mV
Open Loop Gain[3]	$A_{VOL(SA)}$	V_{CM} in range	80	100	–	dB
Closed Loop Gain	$A_{VCL(SA)}$	V_{CM} in range	5	–	–	V/V
Small Signal –3 dB Bandwidth	$BW_{(SA)}$	Gain = 20, V_{IND} = 10 mV_{pp}, R_P = R_M = 4 kΩ, CSB bit = 1	500	–	–	kHz
		Gain = 20, V_{IND} =10 mV_{pp}, R_P = R_M = 4 kΩ, CSB bit = 0	150	–	–	kHz
Output Settling Time	$t_{SET(SA)}$	To within 40 mV of steady state, V_{OUT} = 1 V_{pp} square wave, R_P = R_M = 4 kΩ, Gain = 20, capacitive load = 200 pF	–	1	1.8	µs
Output Dynamic Range	$V_{OUT(SA)}$	–100 µA < I_{OUT} <100 µA	0.3	–	V_{DD} – 0.3	V
Output Current Sink	$I_{sink(SA)}$	V_{IND} = 0 V, V_{OUT} =1.5 V, R_P = R_M = 4 kΩ, Gain = 20	2	–	–	mA
Output Current Source[1]	$I_{source(SA)}$	V_{IND} = 200 mV, V_{OUT} =1.5 V, R_P = R_M = 4 kΩ, Gain = 20, V_{OZ} = 0 V	–	–	–2	mA
VDD Supply Ripple Rejection	$PSRR_{(SA)}$	DC, V_{INP} = V_{INM} = 0 V, R_P = R_M = 4 kΩ, Gain = 20	80	–	–	dB
		f = 100 kHz, V_{INP} = V_{INM} = 0 V, R_P = R_M = 4 kΩ, Gain = 20	–	30	–	dB
Common-Mode Rejection	$CMRR_{(SA)}$	DC, V_{INCM} step from 0 V to 2.0 V, R_P = R_M = 4 kΩ, Gain = 20	60	80	–	dB
		f = 100 kHz, V_{INCM} = 200 mV_{PP}, R_P = R_M = 4 kΩ, Gain = 20	–	62	–	dB
		f = 1 MHz, V_{INCM} = 200 mV_{PP}, R_P = R_M = 4 kΩ, Gain = 20	–	43	–	dB
		f = 10 MHz, V_{INCM} = 200 mV_{PP}, R_P = R_M = 4 kΩ, Gain = 20	–	33	–	dB
Common-Mode Recovery Time	$t_{CMrec(SA)}$	To within 100 mV of steady state, V_{INCM} step from –4 V to +1 V, R_P = R_M = 4 kΩ, Gain = 20, capacitive load = 200 pF	–	1	–	µs

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{DD} = 5 V, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT SENSE AMPLIFIERS[2] (continued) (refer to Figure 1 for definitions)						
Output Slew Rate (Peak)	SR	V_{IND} step from 0 V to 175 mV, $R_P = R_M$ = 4 kΩ, Gain = 20, capacitive load = 200 pF	–	10	–	V/µs
Input Overload Recovery	$t_{IDrec(SA)}$	To within 40 mV of steady state, V_{IND} step from 250 mV to 0 V, $R_P = R_M$ = 4 kΩ, Gain = 20, capacitive load = 200 pF	–	1	–	µs
UNCOMMITTED OPERATIONAL AMPLIFIER[2] (refer to Figure 1 for definitions)						
Input Offset Voltage	$V_{IOS(OA)}$		–10	–	+10	mV
Input Offset Voltage Drift[3]	$\Delta V_{IOS(OA)}$		–	±10	–	µV/°C
Input Bias Current[1]	$I_{BIAS(OA)}$	0 V < V_P < V_{DD}, 0 V < V_M < V_{DD}	–1	0	+1	µA
Input Offset Current[1]	$I_{OS(OA)}$	V_{ID} = 0 V, V_{CM} in range	–1	–	+1	µA
Input Common-Mode Range (DC)	$V_{CM(OA)}$	V_{ID} = 0	0.3	–	V_{DD} – 0.3	V
Differential Input Voltage	$V_{ID(OA)}$		–	–	200	mV
Open Loop Gain[3]	$A_{VOL(OA)}$	V_{CM} in range	80	100	–	dB
Closed Loop Gain	$A_{VCL(OA)}$	V_{CM} in range	1	–	–	V/V
Small Signal –3 dB Bandwidth	$BW_{(OA)}$	V_{IND} = 10 mV_{PP}, $R_P = R_M$ = 4 kΩ, Gain = 20	50	–	–	kHz
Output Settling Time	$t_{SET(OA)}$	To within 40 mV of steady state, V_{OUT} = 1 V_{PP} square wave, $R_P = R_M$ = 4 kΩ, Gain = 20, capacitive load = 200 pF	–	10	20	µs
Output Dynamic Range	$V_{OUT(OA)}$	–100 µA < I_{OUT} < 100 µA	0.3	–	V_{DD} – 0.3	V
Output Current Sink	$I_{sink(OA)}$	V_{IND} = 0 V, V_{OUT} =1.5 V, $R_P = R_M$ = 4 kΩ, Gain = 20	150	–	–	µA
Output Current Source[1]	$I_{source(OA)}$	V_{IND} = 200 mV, V_{OUT} = 1.5 V, $R_P = R_M$ = 4 kΩ, Gain = 20, V_{OZ} = 0 V	–	–	–2	mA
VDD Supply Ripple Rejection	$PSRR_{(OA)}$	DC, V_P = 0.5 VDC, voltage follower	–	40	–	dB
		f = 100 kHz, V_P = 0.5VDC, voltage follower	–	40	–	dB
Common-Mode Rejection	$CMRR_{(OA)}$	DC, V_{INCM} step from 0 V to 2.0 V, $R_P = R_M$ = 4 kΩ, Gain = 20	–	80	–	dB
		f = 100 kHz, V_{INCM} = 200 mV_{PP}, $R_P = R_M$ = 4 kΩ, Gain = 20	–	60	–	dB
		f = 1 MHz, V_{INCM} = 200 mV_{PP}, $R_P = R_M$ = 4 kΩ, Gain = 20	–	45	–	dB
		f = 10 MHz, V_{INCM} = 200 mV_{PP}, $R_P = R_M$ = 4 kΩ, Gain = 20	–	45	–	dB
Common-Mode Recovery Time	$t_{CMrec(OA)}$	To within 100 mV of steady state, V_{INCM} step from –4 V to +1 V, $R_P = R_M$ = 4 kΩ, Gain = 20, capacitive load = 200 pF	–	10	–	µs
Input Overload Recovery	$t_{IDrec(OA)}$	To within 40 mV of steady state, V_{IND} step from 250 mV to 0 V, $R_P = R_M$ = 4 kΩ, Gain = 20, capacitive load = 200 pF	–	10	–	µs

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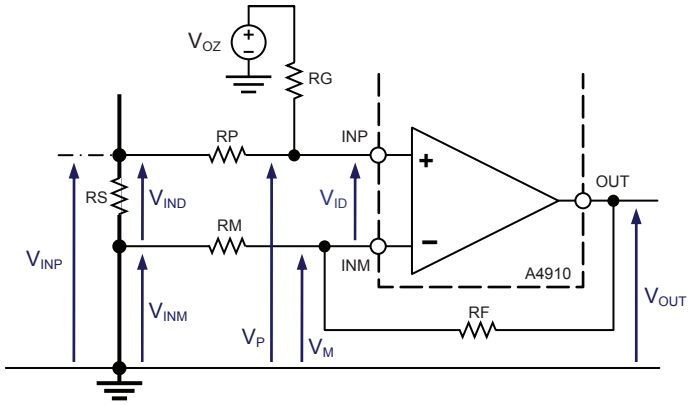
ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{DD} = 5 V, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION						
VREG Undervoltage Lockout	V_{REGON}	V_{REG} rising	7.6	7.95	8.2	V
	V_{REGOFF}	V_{REG} falling	6.9	7.18	7.4	V
Bootstrap Undervoltage	V_{BOOTUV}	Cx with respect to Sx	60	–	74	%V_{REG}
Bootstrap Undervoltage Hysteresis	$V_{BOOTUVhys}$		–	9	–	%V_{REG}
VDD Undervoltage Turn Off	V_{DDUV}	V_{DD} falling	2.45	2.7	2.85	V
VDD Undervoltage Hysteresis	$V_{DDUVhys}$		50	100	150	mV
VDS Threshold	V_{DSTH}	Default power–up level	–	800	–	mV
VBRG Input Voltage	V_{BRG}		5.5	V_{BB}	50	V
VBRG Input Current	I_{VBRG}	V_{DSTH} = 2 V, V_{BB} = 12 V, 0 V < V_{BRG} < V_{BB}	–	–	250	µA
	I_{VBRGQ}	RESETn = low, sleep mode, V_{BB} = 12 V	–	–	5	µA
Short-to-Ground Threshold Offset[4]	V_{STGO}	V_{DSTH} ≥ 1 V, V_{BB} > 7 V	–	±100	–	mV
		V_{DSTH} < 1 V	–150	±50	+150	mV
Short-to-Battery Threshold Offset[5]	V_{STBO}	V_{DSTH} ≥ 1 V, V_{BB} > 7 V	–	±100	–	mV
		V_{DSTH} < 1 V	–150	±50	+150	mV
Fault Blanking Time	t_{BL}	Default power–up state	2.8	3.2	3.6	µs
DIAG Output Clock Division Ratio	N_D	DIAG[1..0] = 01	–	409600	–	–
DIAG Output Temperature Offset[6]	V_{TJD}	DIAG[1..0] = 11	–	1420	–	mV
DIAG Output Temperature Slope[6]	A_{TJD}	DIAG[1..0] = 11	–	–3.85	–	mV/°C
DIAG output V_{DS} Threshold Error	V_{DSE}	DIAG[1..0] = 10	–10	–	10	mV
Hot Temperature Warning Threshold	T_{JWH}	Temperature increasing	125	135	145	°C
Hot Temperature Warning Hysteresis	T_{JWHhys}		–	15	–	°C
Overtemperature Flag	T_{JF}	Temperature increasing	155	170	–	°C
Overtemperature Hysteresis	T_{Jhys}	Recovery = T_{JF} – T_{Jhys}	–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
[2] V_{OZ} = 0.5 V unless otherwise specified.
[3] Confirmed by design and characterization.
[4] With high-side on; as V_{Sx} decreases, fault occurs if $V_{BAT} - V_{Sx} > V_{STG}$, given Short-to-Ground Threshold: $V_{STG} = V_{DSTH} + V_{STGO}$.
[5] With low-side on; as V_{Sx} increases, fault occurs if $V_{Sx} - V_{LSSx} > V_{STB}$, given Short-to-Battery Threshold: $V_{STB} = V_{DSTH} + V_{STBO}$.
[6] $T_J \approx (V_{DIAG} - V_{TJD}) / A_{TJD}$ where T_J is junction temperature in °C, V_{DIAG} is voltage measured on the DIAG pin in mV, V_{TJD} is temperature offset in mV, and A_{TJD} is temperature slope in mV/°C.

Characteristic Definitions



$$V_{INCM} = (V_{INP} + V_{INM}) / 2$$

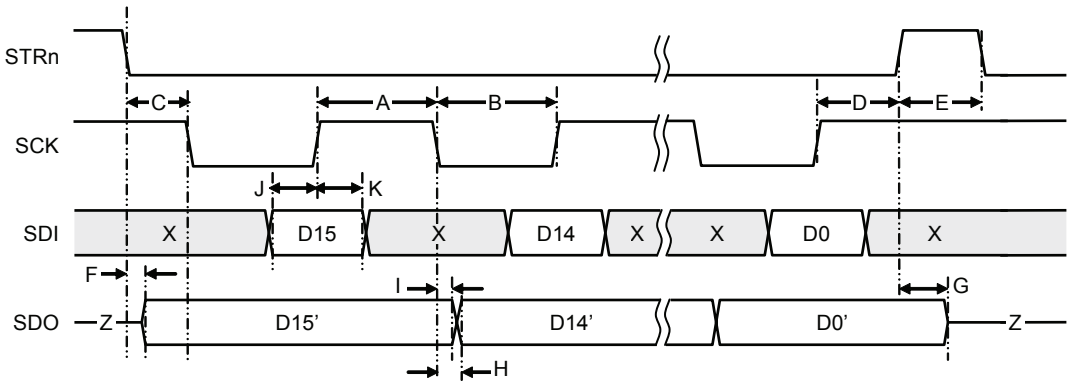
$$V_{CM} = (V_P + V_M) / 2$$

$$V_{OUT} = V_{OZ} + \frac{R_F}{R_M} (V_{INP} - V_{INM})$$

Where: $R_P = R_M$ and $R_G = R_F$

Figure 1: Operational amplifier voltage definitions

Timing Diagrams



X=don't care, Z=high impedance (tri-state)

Figure 2: Serial interface timing

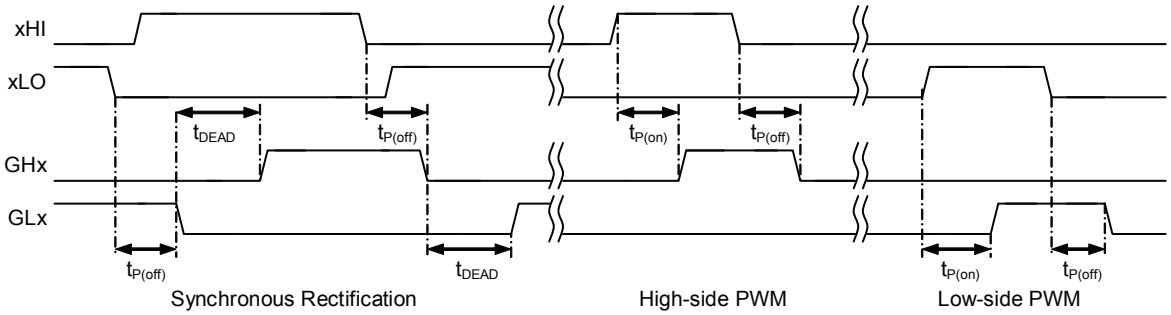


Figure 3: Gate drive timing, phase inputs

(A) xHI pin = high, xLO pin = low

(B) xHI pin = low, xLO pin = high

Figure 4: Gate drive timing, COASTn input

Timing Diagrams (continued)

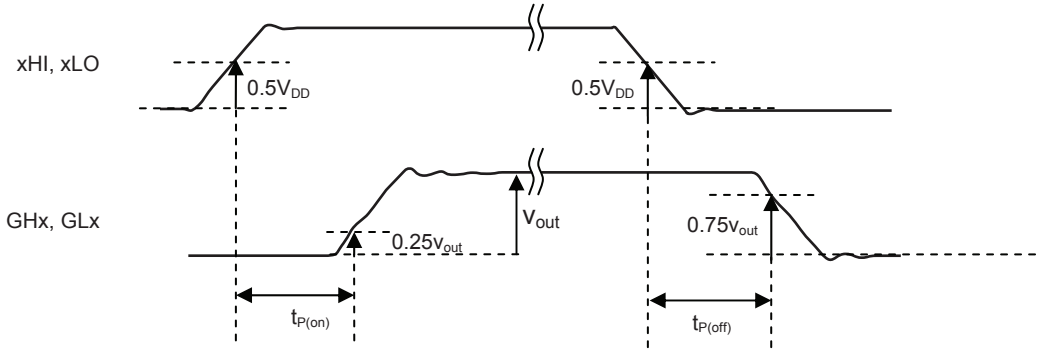


Figure 5: Propagation delay definition

Logic Truth Tables

Table 1: Mapping of Phase Control Inputs to Internal Phase Control States

Phase Control Inputs		Resultant Control States (Inputs for Table 2)
External Control Pins	Run Register Control Bits	
xHI	**xH**	**HIx**
0	0	0
0	1	1
1	0	1
1	1	1
xLO	**xL**	**LOx**
0	0	0
0	1	1
1	0	1
1	1	1

Table 2: Mapping of Internal Phase Control States to Gate Drive Outputs

Inputs			Gate Drive Outputs			
Output Override Pin	Control States (From Table 1)					
COASTn	**HIx**	**LOx**	**GHx**	**GLx**	**Sx**	**Comment**
1	0	0	Low	Low	Z	Phase disabled
1	0	1	Low	High	Low	Phase sinking
1	1	0	High	Low	High	Phase sourcing
1	1	1	Low	Low	Z	Phase disabled
0	X	X	Low	Low	Z	Phase disabled

X = don't care, Z = high impedance

All three motor drive phases are controlled independently. Control states (HIx, LOx) are derived by combining the logic states applied to the control input pins (xHI, xLO) with the bit patterns held in the Run register (xH, xL). Normally the input pins or the Run register method is used for control with the other being held inactive (all pins or bits at logic 0). Table 1 details how the two control mechanisms are combined and Table 2 shows the way in which the resultant control states map to the gate drive outputs.

Characteristic Performance

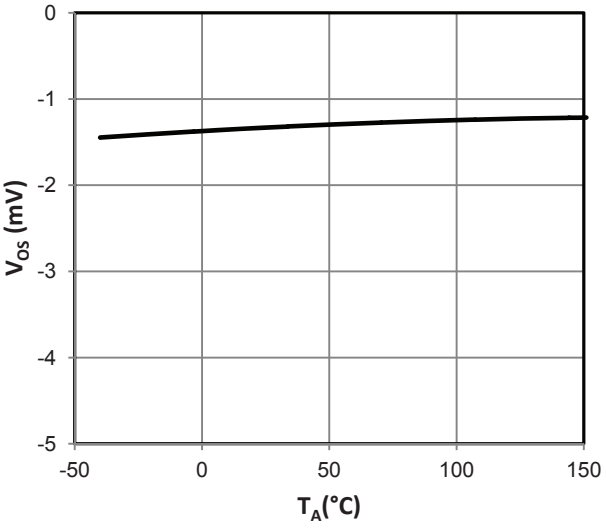


Figure 6: Current-Sense Amplifier Input Offset Voltage versus Temperature

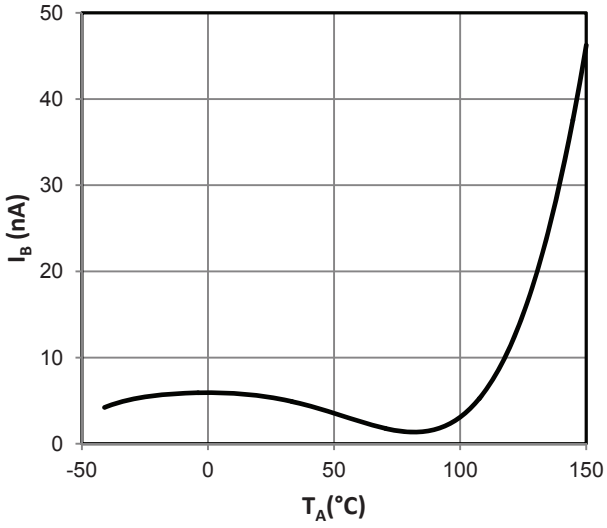


Figure 7: Current-Sense Amplifier Input Bias Current versus Temperature

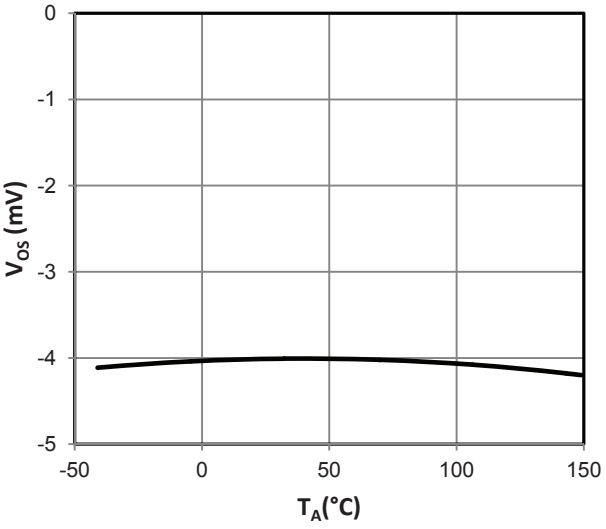


Figure 8: Uncommitted Operational Amplifier Input Offset Voltage versus Temperature

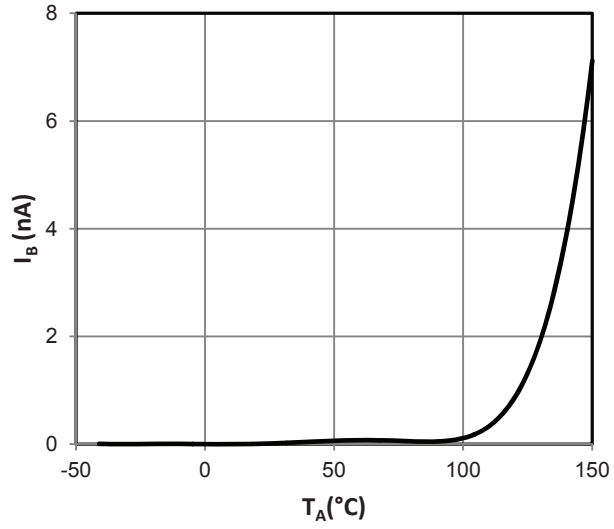


Figure 9: Uncommitted Operational Amplifier Input Bias Current versus Temperature

Functional Description

The A4910 provides six high-current gate drives capable of driving a wide range of N-channel power MOSFETs. The gate drives are configured as three high-side drives and three low-side drives. Gate drives can be controlled individually with logic inputs or through the SPI-compatible serial interface. CMOS input thresholds are compatible with 3.3 or 5 V logic outputs. The serial interface also provides configuration control, programmable dead time and programmable V_{DS} threshold for short detection.

The A4910 provides all the necessary circuits to ensure that the gate-source voltage of both high-side and low-side external MOSFETs are above 10 V at supply voltages down to 7 V. For extreme battery voltage drop conditions correct function is maintained down to 5.5 V, but with reduced gate drive.

The control inputs to the A4910 provide a very flexible solution for many motor control applications. Independent control over each MOSFET allows each driver to be driven with an independent PWM signal for full sinusoidal excitation.

Three current-sense amplifiers allow the current in each leg of the three-phase bridge to be sensed by a low-value sense resistor in the ground connection. With fast settling time, high-transient immunity, and fast overload recovery, the current-sense amplifiers are designed especially for current sensing in switched power systems.

An additional uncommitted operational amplifier provides analog signal buffering and amplification.

Specific functions are described more fully in the following sections.

Input and Output Terminal Functions

VBB Main power supply for internal regulators and charge pump. The main power supply should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.

VDD Logic supply. Should be decoupled to ground with a 100 nF capacitor. Inputs have CMOS thresholds making them compatible with 3.3 V and 5 V logic.

CP1, CP2 Pump capacitor connection for charge pump. Connect a minimum 220 nF, typically 470 nF, capacitor between CP1 and CP2.

VREG Regulated voltage, nominally 13 V, used to supply the low-side gate drivers and to charge the bootstrap capacitors. A sufficiently large storage capacitor must be connected to this terminal to provide the transient charging current.

AGND Analog reference ground. Quiet return for measurement and input references. Connect to PGND (see Layout Recommendations section).

PGND Digital and power ground. Connect to supply ground and AGND (see Layout Recommendations section).

LSSA, LSSB, LSSC Low-side return path for discharge of the capacitance on the MOSFET gates. Connected independently to the source of the low-side MOSFET on the corresponding phase of the power bridge through a low-impedance track.

VBRG Sense input to the top of the external MOSFET bridge. Allows accurate measurement of the voltage at the drain of the high-side MOSFETs.

CA, CB, CC High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers.

GHA, GHB, GHC High-side, gate-drive outputs for external N-channel MOSFETs.

SA, SB, SC Motor phase connections. These terminals sense the voltages switched across the load. They are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drivers

GLA, GLB, GLC Low-side, gate-drive outputs for external N-channel MOSFETs.

AHI, ALO Phase A gate drive controls. Logically ORed with the corresponding bits in the Run register to control the GHA and GLA ouputs. Refer to tables 1 and 2 for detailed logic and safety lockouts.

BHI, BLO Phase B gate drive controls. Logically ORed with the corresponding bits in the Run register to control the GHB and GLB ouputs. Refer to tables 1 and 2 for detailed logic and safety lockouts.

CHI, CLO Phase C gate drive controls. Logically ORed with the corresponding bits in the Run register to control the GHC and GLC ouputs. Refer to tables 1 and 2 for detailed logic and safety lockouts.

COASTn Active-low input. Forces all gate drive outputs low and turns all external MOSFETs off. Overrides all gate drive control inputs and registers.

CSAP, CSAM Phase A current-sense amplifier inputs.

CSAO Phase A current-sense amplifier output.

CSBP, CSBM Phase B current-sense amplifier inputs.

CSBO Phase B current-sense amplifier output.

CSCP, CSCM Phase C current-sense amplifier inputs.

CSCO Phase C current-sense amplifier output.

OPAP, OPAM Uncommitted operational amplifier inputs.

OPAO Uncommitted operational amplifier output.

RESETn Resets faults when pulsed low. Forces low-power shutdown (sleep) when held low for more than the RESET shutdown time, t_{RSD}. Can be pulled to V_{BB} with a 30 kΩ resistor.

SDI Serial data input. 16-bit serial word input, MSB first.

SDO Serial data output. High impedance when STRn is high. Outputs bit 15 of the fault register, the fault flag, as soon as STRn goes low.

SCK Serial clock. Data is latched in from SDI on the rising edge of CLK. There must be 16-rising edges per write and SCK must be held high when STRn changes.

STRn Serial data strobe and serial access enable. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

DIAG Diagnostic output. Programmable output to provide one of four functions: fault flag, temperature, clock, and V_{DS} threshold. Default is fault flag.

Power Supplies

Two power supply voltages are required, one for the logic interface and one for the analog and output drive sections. The logic supply, connected to VDD, can be driven from 3 to 5.5 V, allowing the inputs to be driven from a 3.3 or 5 V logic interface. The main power supply should be connected to VBB through a reverse voltage protection circuit. Both supplies should be decoupled with ceramic capacitors connected close to the supply and ground terminals. The A4910 will operate within specified parameters with a V_{BB} supply from 7 to 50 V and will function correctly with a supply down to 5.5 V. This provides a very rugged solution for use in the harsh automotive environment.

CP1,CP2, VREG The gate drivers are powered by an internal regulator that limits the supply to the drivers and therefore the maximum gate voltage. For V_{BB} supply greater than about 16 V the regulator is a simple buck regulator. Below 16 V the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor, typically 470 nF, connected between the CP1 and CP2 terminals.

The regulated voltage, nominally 13 V, is available on the VREG terminal. A sufficiently large storage capacitor (see the Applications Information section) must be connected to this terminal to provide the transient charging current to the low-side drivers and the bootstrap capacitors.

Gate Drives

The A4910 is designed to drive external, low on-resistance, power N-channel MOSFETs. It supplies the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drives is provided by the capacitor on the VREG terminal. The charge current for the high-side drives is provided by the bootstrap capacitors connected between the Cx and Sx terminals, one for each phase. The charge and discharge rate can be controlled using an external resistor in series with the connection to the gate of the MOSFET.

Bootstrap Charge Management The A4910 monitors the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive. Before a high-side drive can be turned on, the bootstrap capacitor voltage must be higher than the turn-on voltage limit. If this is not the case, then the A4910 will attempt to charge the bootstrap capacitor by activating the complementary low-side drive. Under normal circumstances this will charge the capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled.

The bootstrap voltage monitor remains active while the high-side drive is active, and if the voltage drops below the turn-off voltage, a charge cycle is also initiated. The bootstrap charge management circuit may actively charge the bootstrap capacitor regularly when the PWM duty cycle is very high, particularly when the PWM off-time is too short to permit the bootstrap capacitor to become sufficiently charged. If, for any reason, the bootstrap capacitor cannot be sufficiently charged, a bootstrap fault will occur (see the Diagnostics section for further details).

In systems where the bootstrap voltage is managed by the controller, the bootstrap management in the A4910 can be disabled. The bootstrap voltage monitor remains active and will still indicate bootstrap faults.

Top-Off Charge Pump An additional top-off charge pump is provided for each phase, which allows the high-side drive to maintain the gate voltage on the external MOSFET indefinitely, ensuring so-called 100% PWM if required. This is a low current trickle charge pump and is only operated after a high-side has been signaled to turn on. There is a small amount of bias current drawn from the Cx terminal to operate the floating high-side circuit (<40 µA) and the charge pump simply provides enough drive to ensure the bootstrap voltage, and hence the gate voltage, will not droop due to this bias current.

In some applications, a safety resistor is added between the gate and source of each MOSFET in the bridge. When a high-side MOSFET is held in the on-state, the current through the associated high-side gate-source resistor, R_{GSH}, is provided by the high-side driver and therefore appears as a static resistive load on the top-off charge pump. The minimum value of R_{GSH} for which the top-off charge pump can provide current, without dropping below the bootstrap undervoltage threshold, is defined in the Electrical Characteristics table.

In all cases, the charge required for initial turn-on of the high-side gate is always supplied by the bootstrap capacitor. If the bootstrap capacitor becomes discharged the top-off charge pump alone will not provide sufficient current to allow the MOSFET to turn on.

High-Side Gate Drives GHA, GHB, GHC High-side, gate drive outputs for external N-channel MOSFETs. External resistors between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) can be used to control the slew rate seen at the gate, thereby controlling the di/dt and dv/dt of the voltage at the SA, SB, and SC terminals.

GHx set high means that the upper half of the driver is turned on and its drain will source current to the gate of the high-side MOSFET in the external motor-driving bridge, turning it on. *GHx set low* means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET gate circuit to the respective Sx terminal, turning it off.

CA, CB, CC High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers. The bootstrap capacitors are charged to approximately V_{REG} when the associated output Sx terminal is low. When the output swings high, the voltage on this terminal rises with the output to provide the boosted gate voltage required for the high-side N-channel power MOSFETs.

SA, SB, SC are directly connected to the motor phase connections. These terminals sense the voltages switched across the load. These terminals are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drivers. The discharge current from the high-side MOSFET gate capacitance flows through these connections which should have low-impedance traces to the MOSFET bridge.

Low-Side Gate Drives GLA, GLB, GLC The low-side, gate drive outputs are referenced to the corresponding LSSx terminal. These outputs are designed to drive external N-channel power MOSFETs. External resistors between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) can be used to control the slew rate seen at the gate, thereby providing some control of the di/dt and dv/dt of the voltage at the SA, SB, and SC terminals. *GLx set high* means that the upper half of the driver is turned on and its drain will source current to the gate of the low-side MOSFET in the external power bridge, turning it on. *GLx set low* means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET gate circuit to the corresponding LSSx terminal, turning it off.

LSSA, LSSB, LSSC Return paths for discharge of the low-side external MOSFET gate-source capacitances. Each LSSx pin to be connected to its associated MOSFET source by a low-impedance PCB trace.

If a single sense resistor is used across all three phases, the LSSx pins may be connected together and linked to the sources of all three low-side MOSFETs.

Gate Drive Passive Pull-Downs Each gate drive output includes a discharge circuit to ensure that any external MOSFET connected to the gate drive output is held off when the power is removed. This discharge circuit appears as a variable resistance pull-down, but is not active when the A4910 is in normal operating mode. At low gate source voltage, less than 100 mV, the resistance is approximately 950 kΩ to ensure that any charge accumulated on the MOSFET gate has a discharge path. This resistance reduces rapidly as the voltage increases such that any MOSFET gate that becomes charged by external means is rapidly discharged to below the turn-on threshold. In some applications, this can eliminate the requirement for a permanent external gate source resistor.

Dead Time To prevent cross-conduction (shoot-through) in any phase of the power MOSFET bridge, it is necessary to have a dead-time delay between a high- or low-side turn-off and the next complementary turn-on event. The potential for cross-conduction occurs when any complementary high-side and low-side pair of MOSFETs are switched at the same time—for example, when using synchronous rectification, or after a bootstrap capacitor charging cycle. In the A4910, the dead time for all three phases is set by the contents of the DT[6..0] bits in the Config0 register. These seven bits contain a positive integer that determines the dead time in system clock cycles.

The dead time is defined as:

$$t_{DEAD} = n \times 50 \text{ ns} \quad (1)$$

where n is a positive integer defined by DT[6..0] and 50 ns is the typical system clock period.

For example, when DT[6..0] contains [0 1 1 0 0 0 0] (48 decimal), then t_{DEAD} is 2.4 µs (typical). If n = 1 or 2, t_{DEAD} = 100 ns, the minimum dead time. The accuracy of t_{DEAD} is determined by the accuracy of the system clock as defined in the Electrical Characteristics table.

If the dead time is to be generated externally, for example by the PWM output of a microcontroller, then entering a value of zero in DT[6..0] will disable the dead timer. However, the logic that prevents cross-conduction will still be active.

The internally generated dead time will only be present if the on-command for one MOSFET occurs within one dead-time period after the off-command for its complementary partner. In the case where one side of a phase drive is permanently off, for example when using diode rectification with slow decay, then the dead time will not occur. In this case, the gate drive will turn on within the specified propagation delay after the corresponding phase input goes high (see Figure 3).

Logic Control Inputs

All three motor drive phases are controlled independently as detailed in Table 1 and Table 2. Control states (HIx, LOx) are derived by combining the logic states applied to the control input pins (xHI, xLO) with the bit patterns held in the Run register (xH, xL). Normally, either the input pin or the Run register method is used for control, with the other held inactive (all pins or all bits at 0).

The control input pins (xHI, xLO) are CMOS and can be driven from 3.3 or 5 V logic. Logic thresholds are ratiometric with respect to V_{DD} and hysteresis is provided to improve noise immunity as detailed in the Electrical Characteristics table.

AHI, ALO, BHI, BLO, CHI, and CLO can be used to directly control the gate drives. The xHI inputs correspond to the high-side drives and the xLO inputs correspond to the low-side drives. These logic inputs are combined, using logical OR, with the corresponding bits, xH, xL, in the serial interface Run register to determine the state of the gate drive. If the result of the OR is a logic high then the corresponding gate drive output will be high and the MOSFET will be active. Internal lockout logic ensures that the high-side output drive and low-side output drive cannot be active simultaneously.

COASTn is an active-low input, which overrides any other gate control signals and forces all gate drive outputs, GHx or GLx, low to turn off all external MOSFETs. This can be used to protect the MOSFETs and the motor in the case of a short-circuit. COASTn does not clear any faults so that the fault flags can be decoded or the serial fault word can be read. It may also be used to provide fast decay PWM without synchronous rectification.

RESETn is an active-low input which allows the A4910 to enter sleep mode, in which the current consumption from the V_{BB} and V_{DD} supplies is reduced to its minimum level. When RESETn is held low for longer than the reset shutdown time, t_{RSD}, the regulator and all internal circuitry is disabled and the A4910 enters sleep mode. In sleep mode, the latched faults and corresponding fault flags are cleared. When coming out of sleep mode, the protection logic ensures that the gate drive outputs are off until the charge pump reaches its correct operating condition. The charge pump stabilizes in approximately 1 ms under nominal conditions.

To allow the A4910 to start up without an external logic input, the RESETn terminal can be pulled to V_{BB} with an external pull-up resistor. The resistor value should be between 20 and 33 kΩ.

RESETn can also be used to clear any fault conditions without entering sleep mode by taking it low for the reset pulse width, t_{RST}. Any latched fault conditions such as short detection or bootstrap capacitor undervoltage, which disable the outputs, will be cleared, as will the serial fault register.

Current-Sense Amplifiers

Three user-configurable differential sense amplifiers are provided to allow the use of low-value sense resistors or current shunts as the current-sensing elements. The input common-mode range of the CSxP and CSxM inputs allows below-ground current sensing typically required for low-side current sense in PWM motor control during switching transients. The output of the sense amplifiers are available at the CSxO outputs and can be used in peak or average current control systems.

The gain of each sense amplifier is set using external input and feedback resistors. The gain must be set to be greater than the specified minimum to ensure stability. Typically the gain is set between 5 and 50 V/V. Output offset can also be added using external resistors. Examples of setting the sense amplifier gain and offset are provided in the Applications Information section.

If the sense amplifiers are used for average current measurement, or in any system where peak signal full scale might not be directly accommodated, it is possible to reduce amplifier bandwidth by setting the CSB bit to 0 in the Config1 register. This will approximately reduce the bandwidth of the sense amplifier by half and will also reduce the quiescent current.

Uncommitted Operational Amplifier

One additional uncommitted operational amplifier is provided for general use as an analog buffer. The gain of the operational amplifier is set using external input and feedback resistors. There is sufficient open loop gain to allow closed loop gain up to 50 V/V, and the operational amplifier can be configured as a unity gain buffer.

Diagnostics

Several diagnostic features are integrated into the A4910 to provide indication of fault conditions. In addition to system-wide faults such as undervoltage and overtemperature, the A4910 integrates individual drain-source monitors for each external MOSFET, to provide short-circuit detection. Detailed diagnostic information can be read from the Diagnostic register through the serial interface any time.

DIAG Output

A single pin output that may be programmed via the serial interface to carry any one of four diagnostic signals:

- a general fault flag
- a voltage representing the temperature of the internal silicon
- the programmed V_{DS} threshold voltage
- a clock signal derived from the internal chip clock

The power-on default for the DIAG output is the general fault flag, which is low at any time when a fault is present or when one of the transient faults has been latched. Note that this is not exactly the same signal as the fault flag in the Diagnostic register.

System Faults

Parameters critical for the safe operation of the A4910 and of the external MOSFETs are monitored. These include chip temperature, logic supply voltage, and the voltages required to drive the external MOSFETs, namely, V_{REG} and each of the bootstrap voltages. Note that the main supply voltage, V_{BB}, is not monitored because the critical voltages are generated by the charge pumps internal to the A4910.

VREG Undervoltage VREG powers the low-side gate drivers and provides current to charge the bootstrap capacitors. It is critical that the voltage on VREG (and, for high-side switching, the voltages on the bootstrap capacitors) is high enough prior to attempting to switch any gate drive outputs into the high, external MOSFET on, state.

At power-up, all gate drive outputs and the general fault flag on the DIAG pin remain low until V_{REG} exceeds the VREG Undervoltage Lockout threshold, V_{REGON} (approximately 8 V). This value of V_{REG} should be sufficient to turn on standard-threshold

external power MOSFETs at a battery voltage as low as 5.5 V, though the resultant MOSFET on-resistance may be higher than its specified maximum.

During normal operation, when a VREG undervoltage is detected, the general fault flag and the Diagnostic register will be set and the outputs will be disabled. When the VREG undervoltage condition is removed, the general fault flag will be cleared and the outputs enabled. The VR flag in the Diagnostic register will remain set until cleared by a register reset (see the Diagnostic Register section for serial access information).

Bootstrap Undervoltage In addition to a monitor on VREG, the A4910 also monitors the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive.

Before a high-side drive can be turned on, the bootstrap capacitor voltage must be higher than the turn-on voltage limit. If this is not the case, and bootstrap management is enabled (Config1 register DBM bit set to 0), then the A4910 will attempt to charge the bootstrap capacitor by activating the complementary low-side drive. Under normal circumstances this will charge the capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled.

While the high-side drive is active, the bootstrap voltage monitor remains active. If the voltage drops below the turn-off voltage, a charge cycle is initiated.

In either case, if there is a fault that prevents the bootstrap capacitor from charging, then the charge cycle will timeout, the general fault flag will be set, and the outputs will be disabled. The appropriate bit in the Diagnostic register will be set to allow the faulty bootstrap capacitor to be identified by reading the serial interface.

The bootstrap undervoltage fault state will be latched until RESETn is low, a serial read is completed, or a power-on reset occurs due to a VDD undervoltage on the logic supply.

VDD Undervoltage The logic supply voltage at VDD is monitored to ensure correct logical operation. If the voltage on VDD drops below the VDD undervoltage threshold, V_{DDUV}, then the logical function of the A4910 cannot be guaranteed and the outputs will be immediately disabled. The A4910 will enter a power-down state and all internal activity, other than the VDD voltage monitor, will be suspended. When the voltage at VDD rises above the rising undervoltage threshold, $V_{DDUV} + V_{DDUVhys}$, the A4910 will perform a power-on reset. All serial control registers will be reset to their power-on state and all fault states and the general fault flag will be reset. The FF bit and the POR bit in the Diagnostic register will be set to 1 to indicate that a power-on reset has taken place. The same power-on reset sequence occurs at initial start-up or after recovery from a VDD brown-out. (A brown-out is defined as V_{DD} momentarily dropping below the V_{DDUV} threshold during operation.)

Overtemperature An internal temperature-to-voltage converter provides a measurement of the surface temperature of the silicon. This voltage is available as an analog output on the DIAG terminal by setting DIAG[1..0] to [1 1].

Two temperature thresholds are provided: a hot warning, and an overtemperature shutdown.

• If the chip temperature rises above the hot temperature warning threshold, T_{JWH}, the Diagnostic register temperature warning bit, TW, will be set to 1 and the general fault flag will go low. No action will be taken by the A4910. When the temperature drops below T_{JW} by more than the hysteresis value, T_{JWHhys}, the general fault flag goes high but the TW bit remains set to 1 until reset.

• If the chip temperature rises above the overtemperature threshold, T_{JF}, the overtemperature bit, OT in the Diagnostic register, will be set to 1. If the ESF bit in the Config1 register is set to 1, when an overtemperature is detected, all gate drive outputs will be disabled automatically. If ESF is set to 0, then no circuitry will be disabled and action must be taken by the user to limit the power dissipation in some way to prevent overtemperature damage to the chip and unpredictable device operation. When the temperature drops below T_{JF} by more than the hysteresis value, T_{JFhys}, the OT bit remains set to 1 until reset.

MOSFET Faults

Faults on any external MOSFETs are determined by measuring the drain-source voltage of the MOSFET and comparing it to the drain-source threshold voltage, V_{DSTH}, defined by the VT[6..0] bits in the Config1 register. These bits provide the input to a 7-bit D-to-A converter that has a least significant bit value of 25 mV (typical). For example, when VT[6..0] contains [1 0 1 1 0 1 0] (90 decimal), then V_{DSTH} = 2.25 V (typical).

The low-side drain-source voltage for any MOSFET is measured between the LSSx terminal and the corresponding Sx terminal. Using the LSSx terminal rather than the ground connection

avoids adding any low-side current sense voltage to the real low-side drain-source voltage. The high-side drain-source voltage for any MOSFET is measured between the VBRG terminal and the appropriate Sx terminal. Using the VBRG terminal rather than the bridge supply avoids adding any high-side current-sense voltage to the real high-side drain-source voltage.

VBRG is a low-current input allowing a voltage-sense connection to be made with the top of the external MOSFET bridge. It should be connected directly to the common connection point for the drains of the power bridge MOSFETs at the positive supply connection point. The input current to the VBRG terminal is proportional to the drain-source threshold voltage, V_{DSTH}, and can be approximated by:

$$I_{VBRG} = 72 \times V_{DSTH} + 52 \quad (2)$$

where I_{VBRG} is the current into the VBRG terminal in µA and V_{DSTH} is the voltage on the V_{DSTH} terminal in V.

Fault Blanking Time To avoid false MOSFET fault detection during switching transients, the V_{DS} to V_{DSTH} comparison is delayed by an internal fault blanking timer. The fault blanking time is defined by the contents of the BT[5..0] bits in the Config0 register. These bits provide the input to a 6-bit counter that is clocked by a divide-by-four clock derived from the system clock (typically 20 MHz).

The fault blanking time is defined as:

$$t_{BL} = n \times 100 \text{ ns} \quad (3)$$

where n is a positive integer defined by BT[5..0] and 100 ns is twice the typical system clock period.

For example, when BT[5..0] contains [0 1 1 0 1 0] (26 decimal), then t_{BL} is 2.6 µs (typical).

Short Fault Operation As the phase switches, the measured drain-source voltage may generate a fault because power MOSFETs take a finite time to reach their rated on-resistance. To overcome this and avoid generating false short faults, the voltages are not sampled until one fault blanking time period after the external MOSFET is turned on. If the drain-source voltage remains above the threshold after the fault blanking time expires, then a short fault will be generated. If the ESF bit in the Config1 register is set to 1, this fault will be latched and the MOSFET disabled until reset.

In some applications it may be necessary to increase the switching time of the external MOSFET by increasing the value of the gate resistor. This will mean that the fault blanking time may be insufficient to avoid generating incorrect fault states. In these cases, by setting the ESF bit to 0, the microcontroller driving the A4910 can be used to determine the correct fault condition. This will disable fault flag latching during a short condition and the general fault flag, available on the DIAG terminal, will only remain low while the measured drain-source voltages show a fault. The microcontroller can then monitor the fault flags and use its own timers to validate the fault condition. Note that, regardless of the ESF setting, any fault detected by the A4910 will still be latched in the Diagnostic register and remain there until reset.

If a short-circuit fault occurs and ESF is set to 0, the external MOSFETs are not disabled by the A4910. To limit any damage to the external MOSFETs or to the motor, the A4910 can either be fully disabled by the RESETn input or all MOSFETs can be switched off by pulling the COASTn input low. Alternatively, setting ESF to 1 allows the A4910 to disable the MOSFETs as soon as a fault is detected.

Fault Actions

Actions taken in the event of fault conditions are as detailed in Table 3. Device behavior changes according to the state of the Enable Stop on Fault (ESF) bit in the Config1 register.

If ESF is set to 1, any short fault or overtemperature condition disables all gate drive outputs and coasts the motor. Short faults are latched until RESETn goes low, a serial read is completed, or a power-on reset occurs. If ESF is set to 0, all gate drive outputs remain active if a short or overtemperature fault occurs, so as not to disrupt normal system operation.

In this latter case (ESF set to 0) it is imperative that the master controller or other external device takes all steps necessary to protect the motor and the drive circuit. For example, COASTn or all gate drive inputs (xHi, xLO) might be taken low to turn off all external MOSFETs.

Table 3: Fault Actions

Fault Description	Outputs Disabled		Fault Latched
	ESF=0	ESF=1	
No fault	No	No	-
VDD Undervoltage	Yes*	Yes*	No
VREG Undervoltage	Yes*	Yes*	No
Bootstrap Undervoltage	Yes*	Yes*	Yes
Temperature Warning	No	No	No
Overtemperature	No	Yes*	No
Short to Ground	No	Yes*	Only when ESF = 1
Short to Supply	No	Yes*	
Shorted Load	No	Yes*	

*All gate drives low, all MOSFETs off.

Fault States

Short to Supply A short from any of the motor phase connections to the battery or VBB connection is detected by monitoring the voltage across the low-side MOSFETs in each phase using the appropriate Sx and LSSx terminals. This drain-source voltage is then compared to the drain-source threshold voltage, V_{DSTH}, after one fault blanking time period. While the drain-source voltage exceeds V_{DSTH}, the general fault flag will be low, and if ESF is set to 1, the fault will be latched and the outputs will be disabled.

Short to Ground A short from any of the motor phase connections to ground is detected by monitoring the voltage across the high-side MOSFETs in each phase using the appropriate Sx terminal and the voltage at VBRG. This drain-source voltage is then compared to the drain-source threshold voltage, V_{DSTH}, after one fault blanking time period. While the drain-source voltage exceeds V_{DSTH}, the general fault flag will be low, and if ESF is set to 1, the fault will be latched and the outputs will be disabled.

Note that the distinction between short to ground and short to supply can only be made by reading the Diagnostic register via the serial bus. The general fault flag simply indicates the presence of a probable short-circuit.

Shorted Motor Winding The short-to-ground and short-to-supply detection circuits also detect shorts across a motor phase winding. In most cases, a shorted winding is indicated by a high-side and low-side fault latched at the same time in the Diagnostic register. In some cases, the relative impedances may only permit one of the shorts to be detected. In any case, when a short of any type is detected the general fault flag will go low and, if ESF is set to 1, the fault will be latched and the outputs will be disabled.

Fault Masking

Individual diagnostics, except VDD undervoltage, can be disabled by setting the corresponding bit in the Mask register. A VDD undervoltage fault cannot be disabled because the diagnostics and the output control depend on VDD to operate correctly. If a bit in the Mask register is set to one, then the corresponding diagnostic actions will be completely disabled. No fault states for the disabled diagnostic will be generated and no fault flags or Diagnostic register bits will be set. (For bit allocations, see the Mask register definition in the Serial Interface section.)

Note that when diagnostics are disabled, care must be taken to avoid potentially damaging conditions.

Serial interface

The three-wire synchronous serial interface, compatible with SPI, can be used to control all features of the A4910. A fourth wire can be used to provide diagnostic feedback and readback of the register contents.

The A4910 can be operated without the serial interface using the default settings and the phase control inputs; however, application specific configurations are only possible by setting the appropriate register bits through the serial interface. In addition to setting the configuration bits, the serial interface can also be used to control the bridge MOSFETs directly.

The serial interface timing requirements are specified in the Electrical Characteristics table, and illustrated in the Serial Interface Timing diagram (Figure 2). Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high, and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high allowing multiple SDI slave units to use common SDI, SCK and SDO connections. Each slave then requires an independent STRn connection.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the Diagnostic register is reset.

If there are more than 16 rising edges on SCK, or if STRn goes high, and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the Diagnostic register will not be reset and the FF bit will be set to indicate a data transfer error.

Diagnostic information or the contents of the configuration and control registers is output on the SDO terminal MSB first while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the Diagnostic register, is output as soon as STRn goes low.

Each of the configuration and control registers has a write bit, WR (bit 13), as the first bit after the register address. This bit must be set to 1 to write the subsequent bits into the selected register. If WR is set to 0, then the remaining data bits (bits 12 to 0) are ignored. The state of the WR bit also determines the data output on SDO. If WR is set to 1 then the Diagnostic register is

Table 4: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Configuration and Control Registers (Write)																
Configuration Register 0 (CONFIG0)	0	0	WR	BT5	BT4	BT3	BT2	BT1	BT0	DT6	DT5	DT4	DT3	DT2	DT1	DT0
			0	1	0	0	0	0	0	0	1	0	0	0	0	0
Configuration Register 1 (CONFIG1)	0	1	WR	CSB	ESF	DIAG1	DIAG0	DBM	–	VT6	VT5	VT4	VT3	VT2	VT1	VT0
			0	1	1	0	0	0	0	0	1	0	0	0	0	0
Mask Register	1	0	WR	–	TW	OT	VR	VA	VB	VC	AH	AL	BH	BL	CH	CL
			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Run Register	1	1	WR	–	–	–	–	–	–	–	AH	AL	BH	BL	CH	CL
			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Diagnostic Register (Read)																
Diagnostic Register	FF	POR	–	–	TW	OT	VR	VA	VB	VC	AH	AL	BH	BL	CH	CL
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

*Power-on reset value shown below each input register bit.

output. If WR is set to 0, then the contents of the register selected by the first two bits is output. In all cases, the first two bits output on SDO will always be the FF bit and the POR bit from the Diagnostic register.

Configuration and Control Registers

The serial data word is 16 bits, input MSB first. The first two bits are defined as the register address. This provides four writeable registers:

• The first two registers are used for configuration: one for blanking-time and dead-time programming, and one for system and diagnostic parameters.

• The third register is the fault mask register, providing the ability to disable individual diagnostics.

• The fourth register is the Run register, containing MOSFET control inputs.

Writing to any register when the WR bit is set to 1 will allow the Diagnostic register to be read at the SDO output.

Configuration Register 0 (Config0) contains a 7-bit number, DT[6..0], to set the dead time and a 6-bit number, BT[5..0], to set the fault blanking time.

DT[6..0] is a positive integer, n, which determines the dead time, t_{DEAD}, in system clock cycles, defined as:

$$t_{DEAD} = n \times 50 \text{ ns}$$

BT[5..0] is a positive integer, n, which determines the blank time, t_{BL}, in system clock cycles, defined as:

$$t_{BL} = n \times 100 \quad \text{(ns)}$$

The accuracy of t_{DEAD} and t_{BL} is defined by the system clock period as defined in the Electrical Characteristics table.

Configuration Register 1 (Config1) contains a 7-bit number, VT[6..0], to set the drain-source threshold voltage, V_{DSTH}, and six configuration bits, ESF, DIAG[1..0], and DBM.

VT[6..0] is a positive integer, n, which determines the drain-source threshold voltage, V_{DSTH}, in 25 mV increments, approximately defined as:

$$V_{DSTH} = n \times 25 \text{ mV} \quad (4)$$

CSB can be used to modify the bandwidth of the sense amplifiers as specified in the Electrical Characteristics table. It also has the effect of reducing the current consumption from VBB.

ESF is the Enable Stop On Fault bit that defines the action taken when a short is detected. See Diagnostics section in the Functional Description above for details of fault actions.

The DIAG[1..0] bits are set to select the output seen on the DIAG terminal. The default output is the general fault flag which is a low true signal that is active anytime a fault is present or a fault state has been latched. The other three outputs provide any external controller with the ability to read back the silicon temperature or the drain-source threshold voltage, or to measure the system clock frequency for calibration.

DBM is the Disable Bootstrap Management bit and should be set to 1 if bootstrap management is not required.

The Mask register contains a fault mask bit for each fault bit in the Diagnostic register. If a bit is set to 1 in the Mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated and no fault flags or Diagnostic register bits will be set.

The Run register contains 1 bit for each gate drive output. The first letter of the bit defines is the phase output (A, B, or C). The second letter defines high-side (H) or low-side (L) gate drive for each phase.

Diagnostic Register

There is one diagnostic register in addition to the three writeable registers. Each time a register is written with the WR bit set to 1, the Diagnostic register can be read, MSB first, on the serial output terminal, SDO (see Serial Timing Diagram, figure 2). The Diagnostic register contains fault flags for each fault condition, a general fault flag, and an overcurrent indicator. Whenever a fault occurs, the corresponding flag bit in the Diagnostic register will be set and latched. The fault flags in the Diagnostic register are only reset on the completion of a serial access or when the RESETn input is low for the reset pulse width, t_{RST}. Resetting the Diagnostic register only affects latched faults that are no longer present. For any static faults that are still present, for example overtemperature, the fault flag will remain set after the register reset.

At power-up or after a power-on reset, the FF bit and the POR bit are set and all other bits are reset. This indicates to the external controller that a power-on reset has taken place and all registers have been reset. Note that a power-on reset only occurs when the VDD supply rises above its undervoltage threshold. Power-on reset is not affected by the state of the VBB supply or VREG.

The first bit in the register is the Diagnostic register flag. This is high if any bits in the Diagnostic register are set or if a serial write error or parity error has occurred. When STRn goes low, to start a serial write, SDO comes out of its high-impedance state and outputs the serial register fault flag irrespective of the register address or state of the WR bits. This allows the main controller to poll the A4910 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated and SDO will go into its high-impedance state.

Serial Register Definition

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONFIG0	0	0	WR	BT5	BT4	BT3	BT2	BT1	BT0	DT6	DT5	DT4	DT3	DT2	DT1	DT0
			0	1	0	0	0	0	0	0	1	0	0	0	0	0
CONFIG1	0	1	WR	CSB	ESF	DIAG1	DIAG0	DBM	–	VT6	VT5	VT4	VT3	VT2	VT1	VT0
			0	1	1	0	0	0	0	0	1	0	0	0	0	0

Configuration Register 0 (Config0)

BT[5..0] Fault blanking time

Assumes 20 MHz clock

$t_{BL} = n \times 100$ ns

where n is a positive integer defined by BT[5..0]; for example, for the power-on-reset condition, BT[5..0] = [1 0 0 0 0 0], then t_{BL} = 3.2 µs. t_{BL} can be between 0 ns and 6.3 µs. The accuracy of t_{BL} is defined by the system clock period as defined in the Electrical Characteristics table.

DT[6..0] Dead time

Assumes 20 MHz clock

$t_{DEAD} = n \times 50$ ns

where where n is a positive integer defined by DT[6..0] and t_{DEAD} has a minimum value of 100 ns. For example, for the power-on reset condition, DT[6..0] = [0 1 0 0 0 0 0], t_{DEAD} = 1.6 µs. t_{DEAD} can be between 100 ns and 6.35µs. The accuracy of t_{DEAD} is defined by the system clock period as defined in the Electrical Characteristics table. A value of 1 or 2 in DT[6..0] sets the minimum dead time of 100 ns. A value of all 0s disables dead time.

Configuration Register 1 (Config1)

CSB Current sense bandwith

CSB	Current sense bandwith	Default
0	Reduced bandwidth	
1	Full bandwidth	D

ESF Enable stop on fault

ESF	Enable stop on fault	Default
0	Stop on fault disabled	
1	Stop on fault enabled	D

DIAG[0..1] Selects signal routed to DIAG output

DIAG1	DIAG0	Signal on DIAG terminal	Default
0	0	General Fault– low true	D
0	1	Clock / 409,600 (48.828 Hz Nominal)	
1	0	V_{DS} Threshold voltage	
1	1	Temperature	

DBM Disable bootstrap management

DBM	Disable Bootstrap Management	Default
0	Bootstrap management active	D
1	Bootstrap management disabled	

VT[6..0] V_{DS} Threshold

Typically: $V_{DSTH} = n \times 25$ mV

where n is a positive integer defined by VT[6..0]. For example, for the power-on reset condition, VT[6..0] = [0 1 0 0 0 0 0], V_{DSTH} = 800 mV. V_{DSTH} can be between 0 and 3.175 V.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mask	1	0	WR	–	TW	OT	VR	VA	VB	VC	AH	AL	BH	BL	CH	CL
			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Diagnostic	FF	POR	–	–	TW	OT	VR	VA	VB	VC	AH	AL	BH	BL	CH	CL
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mask Register

— —

— —

TW Temperature Warning

OT Overtemperature

VR VREG Undervoltage

VA Phase A boot capacitor fault

VB Phase B boot capacitor fault

VC Phase C boot capacitor fault

AH Phase A high-side V_{DS}

AL Phase A low-side V_{DS}

BH Phase B high-side V_{DS}

BL Phase B low-side V_{DS}

CH Phase C high-side V_{DS}

CL Phase C low-side V_{DS}

xx	Fault mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

Diagnostic Register

FF Diagnostic register flag

POR Power-On Reset

TW Temperature Warning

OT Overtemperature

VR Undervoltage on VREG

VA Phase A boot capacitor fault

VB Phase B boot capacitor fault

VC Phase C boot capacitor fault

AH V_{DS} fault detected on phase A high-side

AL V_{DS} fault detected on phase A low-side

BH V_{DS} fault detected on phase B high-side

BL V_{DS} fault detected on phase B low-side

CH V_{DS} fault detected on phase C high-side

CL V_{DS} fault detected on phase C low-side

xx	Fault mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

FF and POR are always output as the first two bits at the start of any serial transfer. The remaining diagnostic bits are only output if the WR bit in the incoming write is set to 1. If WR is set to 0, then the remaining bits will be the contents of the register selected by the first two bits on the SDI input.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Run	1	1	WR	–	–	–	–	–	–	–	AH	AL	BH	BL	CH	CL
			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Run Register

AH Phase A high-side control
AL Phase A low-side control
BH Phase B high-side control
BL Phase B low-side control
CH Phase C high-side control
CL Phase C low-side control

xH/L	MOSFET Control	Default
0	Corresponding gate drive controlled by external logic input	D
1	Corresponding gate drive high	

ORed with corresponding logic input

Application Information

Dead-Time Selection

The choice of power MOSFET and external series gate resistance determines the selection of the dead time. The dead time should be made long enough to ensure that one MOSFET has stopped conducting before the complementary MOSFET starts conducting. This should also account for the tolerances and variations of the MOSFET gate capacitance, the series gate resistance, and the on-resistance of the driver in the A4910.

Fault Blanking Time Selection

The fault blanking time should be set to avoid false short fault detection that is possible immediately after a MOSFET has been switched on. The length of time required will depend on the switching time of the MOSFET and the capacitance of the load attached to the bridge. The MOSFET switching time is dependent on the size of the MOSFET, the on-resistance of the gate drive, and the resistance between the gate drive output of the A4910 and the gate of the MOSFET. Other factors such as the load impedance, back EMF, and any switching transients also affect the settling time of the MOSFET drain-source voltage. The blanking time should be set so that it is just long enough to avoid these effects under all conditions. For highly dynamic systems, where there is a large load variation, improved short fault detection is possible by changing the blanking time between phase commutations, by using the serial interface. The new blanking time will take effect on the first off-to-on transition following the end of the serial transfer.

Bootstrap Capacitor Selection

CBOOT must be correctly sized to ensure that adequate gate drive is applied to high-side MOSFETs. If the selected value is too large, excessive time will be spent charging the capacitor and the maximum achievable duty cycle and PWM frequency will be reduced. If the selected value is too small, an unacceptably large voltage drop may be experienced when charge is transferred from CBOOT to the MOSFET gate.

To keep the voltage drop due to charge-sharing small, the charge in the bootstrap capacitor, Q_{BOOT}, should be much larger than Q_{GATE}, the charge required by the gate:

$$Q_{BOOT} >> Q_{GATE} \tag{5}$$

A factor of 20 is a reasonable value, so

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

or

$$C_{BOOT} = \frac{Q_{GATE} \times 20}{V_{BOOT}} \tag{6}$$

where V_{BOOT} is the voltage across the bootstrap capacitor.

The voltage drop, ΔV, across the bootstrap capacitor as the MOSFET is being turned on, can be approximated by:

$$\Delta V = \frac{Q_{GATE}}{C_{BOOT}} \tag{7}$$

so for a factor of 20, ΔV will be 5% of V_{BOOT}.

The maximum voltage across the bootstrap capacitor under normal operating conditions is V_{REG}(max). However, in some circumstances, the voltage may transiently reach 18 V—the clamp voltage of the Zener diode between the Cx terminal and the Sx terminal. In most applications with a good ceramic capacitor, the working voltage can be limited to 16 V.

Bootstrap Charging

It is good practice to ensure the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested. The time required to charge the capacitor, t_{CHARGE}, in µs, is approximated by:

$$t_{CHARGE} = \frac{C_{BOOT} \times \Delta V}{500} \tag{8}$$

where C_{BOOT} is the value of the bootstrap capacitor in nF and ΔV is the required voltage of the bootstrap capacitor. At power-up, and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, ΔV can be considered to be the full high-side drive voltage, 12 V. Otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the Sx terminal is pulled low and current flows from VREG through the internal bootstrap diode circuit to C_{BOOT}.

Bootstrap Charge Management

The A4910 provides automatic bootstrap capacitor charge management. The bootstrap capacitor voltage for each phase is continuously checked to ensure that it is above the bootstrap undervoltage threshold, V_{BOOTUV}. If the bootstrap capacitor voltage drops below this threshold, the A4910 will turn on the necessary low-side MOSFET until the bootstrap capacitor exceeds the undervoltage threshold plus the hysteresis, $V_{BOOTUV} + V_{BOOTUVhys}$. The minimum charge time is typically 7 µs, but may be longer for very large values of bootstrap capacitor (>1000 nF). If bootstrap capacitor voltage does not reach the threshold within approximately 200 µs, an undervoltage fault will be flagged.

In systems where the bootstrap voltage is managed by the controller, the bootstrap management in the A4910 can be disabled. The bootstrap voltage monitor remains active and will still indicate bootstrap faults.

VREG Capacitor Selection

The internal reference, VREG, supplies current for the low-side gate drive circuits and the charging current for the bootstrap capacitors. When a low-side MOSFET is turned on, the gate drive circuit will provide the high transient current to the gate that is necessary to turn on the MOSFET quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator, but instead must be supplied by an external capacitor connected to VREG.

The turn-on current for the high-side MOSFET is similar in value to that of the low-side MOSFET, but is mainly supplied by the bootstrap capacitor. However the bootstrap capacitor must then be recharged from the VREG regulator output. Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn on occurs. This means that the value of the capacitor connected between VREG and AGND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side MOSFET turn-on and a bootstrap capacitor recharge. For block commutation control (trapezoidal drive), where only one high-side and one low-side are switching during each PWM period, a minimum value of $20 \times C_{BOOT}$ is reasonable. For sinusoidal control schemes, a minimum value of $40 \times C_{BOOT}$ is recommended. The maximum working voltage of the VREG capacitor will never exceed V_{REG}, so it can be as low as 15 V. This capacitor should be placed as close as possible to the VREG terminal.

Supply Decoupling

Current spikes are likely to be present on all supplies because of the switching action of the circuit. As with all such circuits, the power supply connections should be decoupled with a ceramic capacitor, typically 100 nF, between the supply terminal and ground. These capacitors should be connected as close as possible to the device supply terminals VBB and VDD and the power ground terminal, PGND.

Power Dissipation

In applications where a high ambient temperature is expected, on-chip power dissipation may become a critical factor. Careful attention should be paid to ensure the operating conditions allow the A4910 to remain in a safe range of junction temperature.

The power consumed by the A4910, P_D, can be estimated by:

$$P_D = P_{BIAS} + P_{CPUMP} + P_{SWITCHING} \quad (9)$$

where

$$P_{BIAS} = V_{BB} \times I_{BB} \quad (10)$$

$$P_{CPUMP} = [(2 \times V_{BB}) - V_{REG}] \times I_{AV}, \quad \text{for } V_{BB} < 15\text{ V} \quad (11)$$

$$P_{CPUMP} = (V_{BB} - V_{REG}) \times I_{AV}, \quad \text{for } V_{BB} > 15\text{ V} \quad (12)$$

where $I_{AV} = Q_{GATE} \times n \times f_{PWM}$ (13)

and n is the number of MOSFETs switching during a PWM cycle

$$P_{SWITCHING} = Q_{GATE} \times V_{REG} \times n \times f_{PWM} \times \text{Ratio} \quad (14)$$

where:

$$\text{Ratio} = \frac{10}{R_{GATE} + 10} \quad (15)$$

Braking

The A4910 can be used to perform dynamic braking by switching all low-side MOSFETs on and all high-side MOSFETs off or, conversely, all low-side MOSFETs off and all high-side

MOSFETs on (COASTn high in either case). This will effectively short-circuit the back EMF of the motor, creating a braking torque. During braking, the load current can be approximated by:

$$I_{BRAKE} = \frac{V_{BEMF}}{R_L} \quad (16)$$

where V_{BEMF} is the voltage generated by the motor and R_L is the resistance of the phase winding.

Care must be taken during braking to ensure that the power MOSFET maximum ratings are not exceeded. Dynamic braking is equivalent to slow decay with synchronous rectification and all phases enabled.

The A4910 can also be used to perform regenerative braking. This is equivalent to reversing the motor commutation sequence or using fast decay with synchronous rectification. Note that phase commutation must continue for regenerative braking to operate and the supply must be capable of managing the reverse current—for example, by connecting a resistive load or dumping the current to a battery or capacitor.

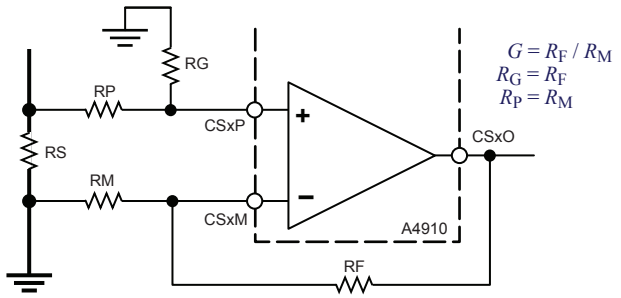


Figure 10: Basic current-sense amplifier configuration

Current-Sense Amplifier

The gain of the current-sense amplifier is set using external input and feedback resistors. Output offset zero point (output voltage corresponding to zero differential input voltage) can be adjusted by the connection of a suitable resistor network. Care must be taken to ensure that the input impedances seen from either end of the sense resistor are matched.

For the basic configuration shown in Figure 10, the two input resistors (RM and RP) have the same value, as do the feedback resistor (RF) between CSxM and CSxO and the ground reference resistor (RG) between CSxP and AGND. The gain of the sense amplifier, G, is determined by the values of RF and RM, and will be approximately:

$$G = \frac{R_F}{R_M} \quad (17)$$

If it is necessary to set the output offset zero point to a positive value (for example, to allow sensing of reverse currents) RG may be replaced by a three-resistor network of the type detailed in Figure 11. The values shown give a gain of 20 with the output offset zero point lifted to 250 mV.

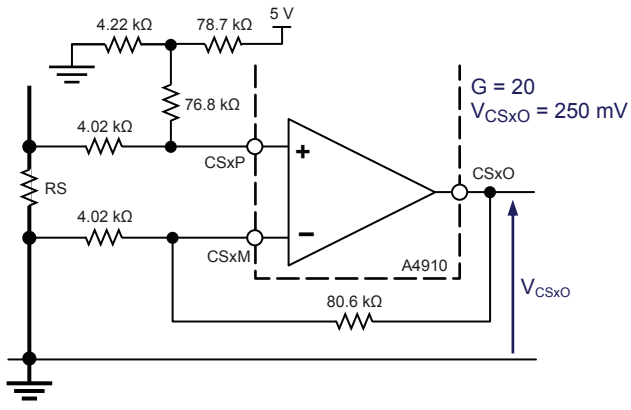


Figure 11: Typical current-sense amplifier configuration

Input/Output Structures

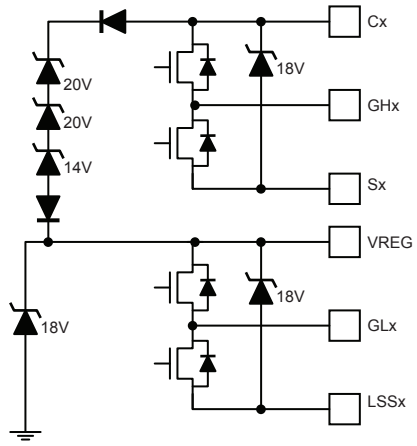


Figure 12a: Gate Drive Outputs

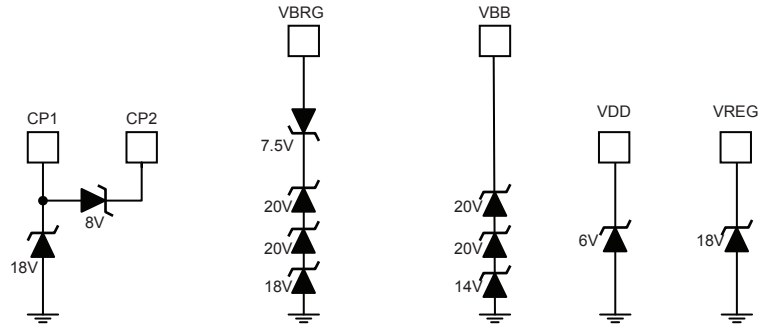


Figure 12b: Supplies

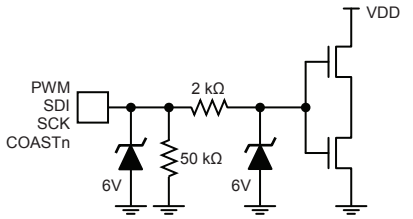


Figure 12c: xHI, xLO, SDI, SCK, COASTn Inputs

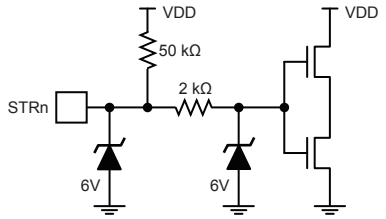


Figure 12d: STRn Input

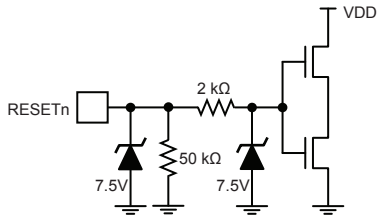


Figure 12e: RESETn Input

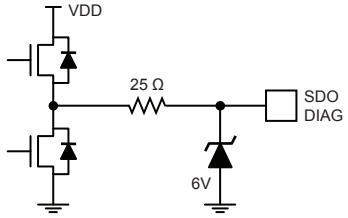


Figure 12f: Logic Outputs

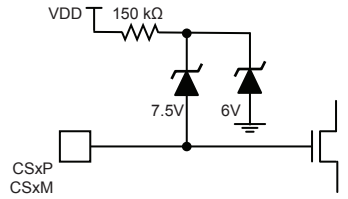


Figure 12g: Current Sense Amplifier Inputs

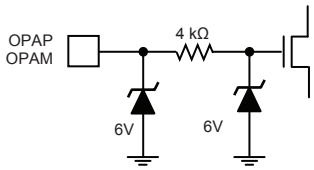


Figure 12h: Operational Amplifier Inputs

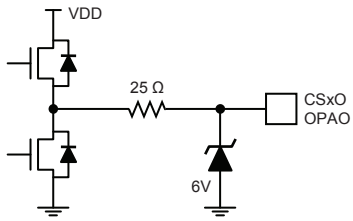


Figure 12i: Operational Amplifier and Current Sense Amplifier Outputs

Layout Recommendations

Careful consideration must be given to PCB layout when designing high-frequency, fast-switching, high-current circuits:

• The A4910 analog ground, AGND, and power ground, PGND, should be connected together at the package terminals. This common point should return separately to the negative side of the motor supply filtering capacitor. This will minimize the effect of switching noise on the device logic and analog reference.

• The exposed thermal pad should be connected to the common point of AGND and PGND.

• Minimize stray inductance by using short, wide copper traces at the drain and source terminals of all power MOSFETs. This includes motor lead connections, the input power bus, and the common source of the low-side power MOSFETs. This will minimize voltages induced by fast switching of large load currents.

• Consider the addition of small (100 nF) ceramic decoupling capacitors across the source and drain of the power MOSFETs to limit fast transient voltage spikes caused by PCB trace inductance.

• Keep the gate discharge return connections Sx and LSSx as short as possible. Any inductance on these traces will cause negative transitions on the corresponding A4910 terminals, which may exceed the absolute maximum ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these terminals with respect to AGND.

• Supply decoupling for VBB, VREG and VDD should be connected independently, close to the PGND terminal. The decoupling capacitors should also be connected as close as possible to the relevant supply terminal.

• Check the peak voltage excursion of the transients on the LSSx terminals with reference to the AGND terminal using a close-grounded (tip and barrel) probe. If the voltage at any LSSx terminal exceeds the absolute maximum in the datasheet, add additional clamping and/or capacitance between the LSSx terminal and the AGND terminal.

• Gate charge drive paths and gate discharge return paths may carry a large transient current pulse. Therefore the traces from GHx, GLx, Sx and LSSx (x = A, B or C) should be as short as possible to reduce inductance in the traces.

• Provide an independent connection from each LSSx terminal to the source of the corresponding low-side MOSFET in the power bridge. Connection of the LSSx terminals directly to the PGND terminal is not recommended as this may inject noise into sensitive functions such as the various voltage monitors.

• The inputs to the sense amplifiers, CSxP and CSxM, should take the form of independent traces and for best results should be matched in length and route.

• A low-cost diode can be placed in the connection to VBB to provide reverse-battery protection. In reverse-battery conditions, it is possible to use the body diodes of the power MOSFETs to clamp the reverse voltage to approximately 4 V. In this case, the additional diode in the VBB connection will prevent damage to the A4910 and the VBRG input will survive the reverse voltage.

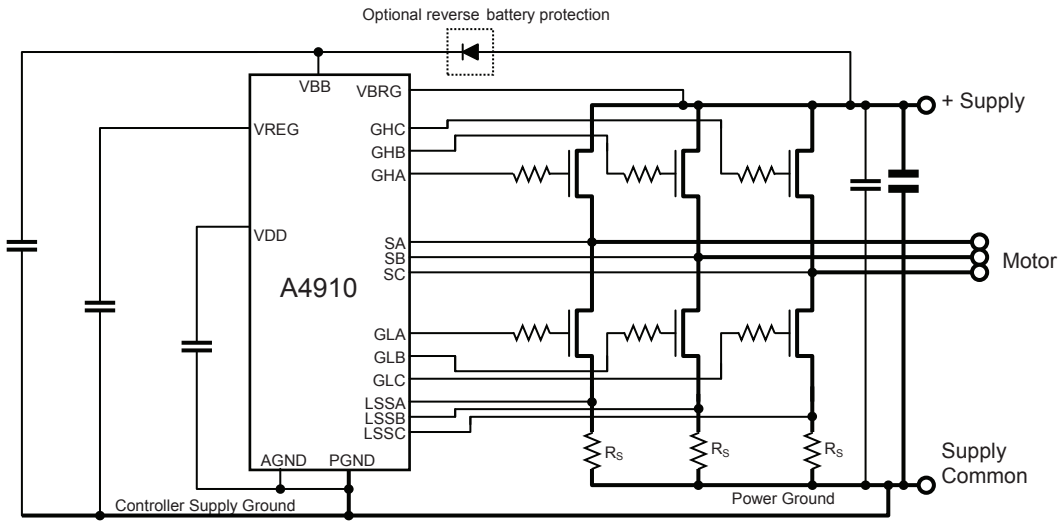
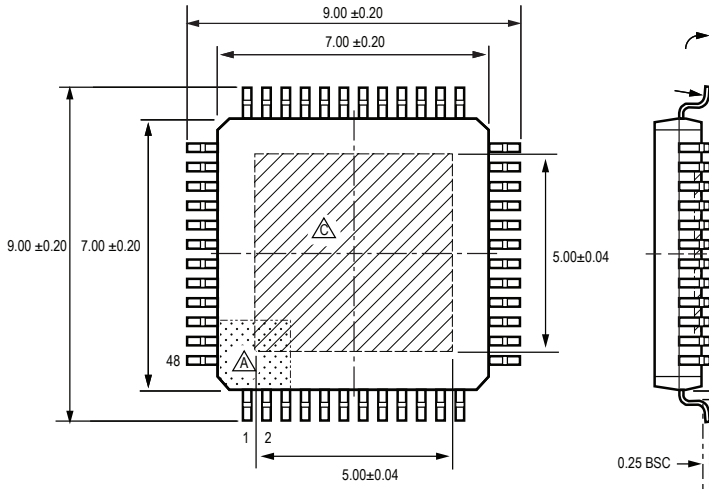
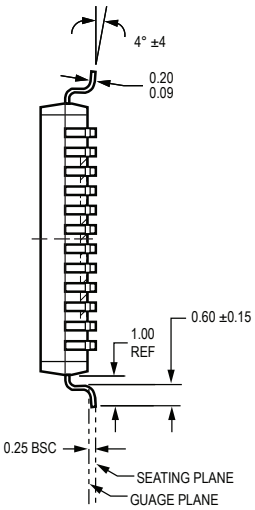
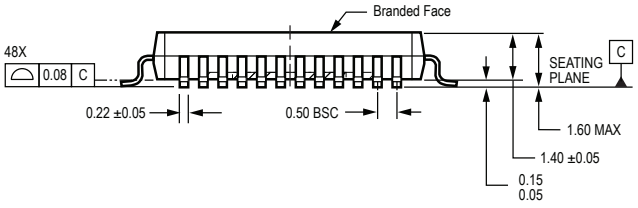


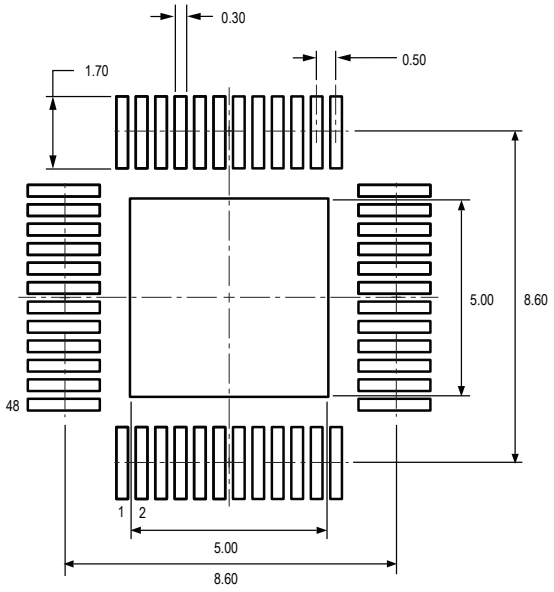
Figure 13. Supply Routing Suggestions

Package JP, 48-Pin LQFP
with Exposed Thermal Pad







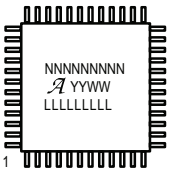


PCB Layout Reference View

Reference land pattern layout (reference IPC7351 QFP50P900X900X160-48M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

For Reference Only; not for tooling use (reference MS-026 BBCHD)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area
B Branding scale and appearance at supplier discretion
C Exposed thermal pad (bottom surface) ; exact dimensions may vary with device



B Standard Branding Reference View

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

Revision History

Number	Date	Description
–	January 24, 2013	Initial release
1	October 7, 2015	Change in t_{BL}
2	May 18, 2016	Updated V_{BB}, V_{REG}, Short-to-Battery, and Short-to-Ground test conditions, updated V_{BRG} Input Voltage min value, and removed footnote 1 from Electrical Characteristics table; corrected Figure 12c.

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