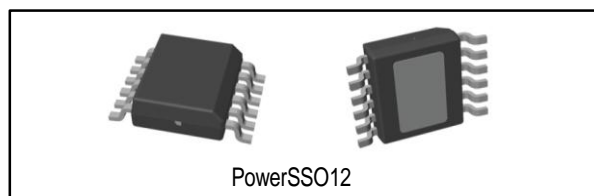


Single high-side switch

Datasheet - production data



Features

$R_{DS(on)}$	I_{out}	V_{CC}
0.060 Ω	2.5 A	65 V

- 8 V to 60 V operating voltage range
- Minimum output current limitation: 2.6 A
- Non-dissipative short-circuit protection (cut-off)
- Programmable cut-off delay time using external capacitor
- Diagnostic signalization for: open load in off-state, cut-off and junction thermal shutdown
- Fast demagnetization of inductive load
- Ground disconnection protection
- V_{CC} disconnection protection
- Undervoltage lock-out
- Designed to meet IEC 61131-2
- PSSO12 package

Applications

- Programmable logic control

- Industrial PC peripheral input/output
- Numerical control machines
- SIL applications

Description

The IPS160H is a monolithic device which can drive capacitive, resistive or inductive loads with one side connected to ground; it is specifically designed to match safety integrity level (SIL) applications.

Built-in thermal shutdown protects the chip against overtemperature and short-circuit. In order to minimize the power dissipation when the output is shorted, a non-dissipative short-circuit protection (cut-off) is implemented, it limits both the output average current value and, consequently, the device overheating. The DIAG common diagnostic pin reports the thermal shutdown, open load in off-state and cut-off.

Cut-off delay time can be programmed by an external capacitor.

Table 1: Device summary

Order code	Package	Packing
IPS160H	PowerSSO12	Tube
IPS160HTR	PowerSSO12	Tape and reel

Contents

1	Block diagram.....	5
2	Pin description	6
	2.1 IN	6
	2.2 OUT	6
	2.3 DIAG	7
	2.4 CoD.....	7
	2.5 GND	7
	2.6 VCC	7
3	Absolute maximum ratings.....	8
4	Electrical characteristics	9
5	Output logic	12
6	Protection and diagnostic.....	13
	6.1 Undervoltage lock-out	13
	6.2 Overtemperature	13
	6.3 Cut-off	13
	6.4 Open load in off-state.....	14
	6.5 VCC disconnection protection	16
	6.6 GND disconnection protection.....	17
7	Active clamp	18
8	Package information	21
	8.1 PowerSSO12 package information	22
9	Revision history	25

List of tables

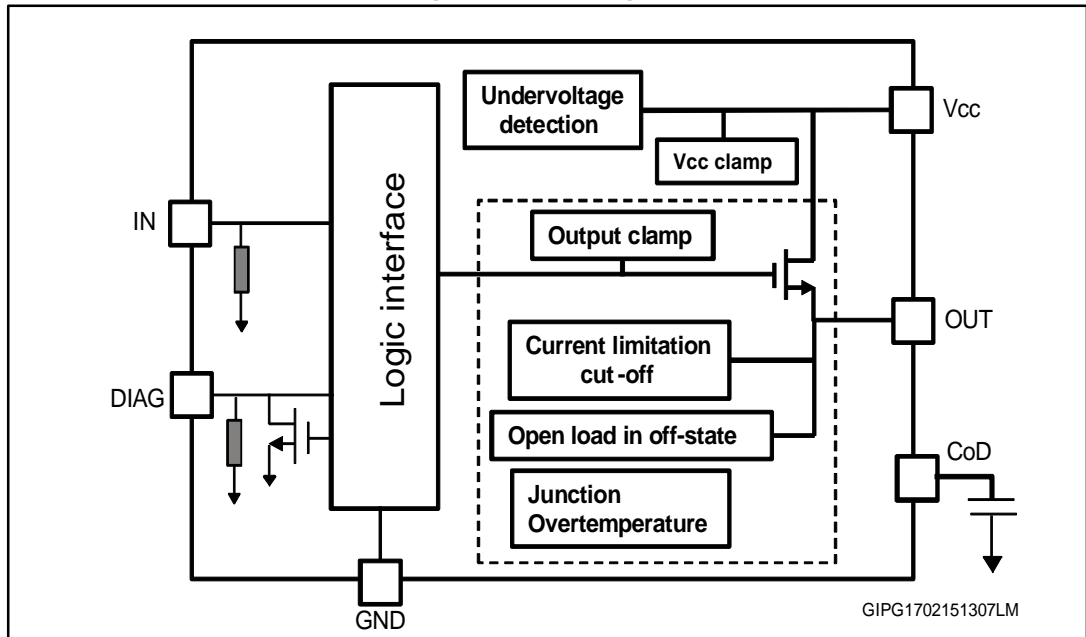
Table 1: Device summary	1
Table 2: Pin configuration	6
Table 3: Absolute maximum ratings	8
Table 4: Thermal data.....	8
Table 5: Supply	9
Table 6: Output stage	9
Table 7: Switching (VCC = 24 V; 125 °C > TJ > -40 °C, RLOAD = 48 Ω).....	9
Table 8: Logic inputs.....	10
Table 9: Protection and diagnostic	10
Table 10: Output stage truth table	12
Table 11: Minimum cut-off delay for TAMB less than -20 °C	14
Table 12: PowerSSO12 package mechanical data	23
Table 13: Document revision history	25

List of figures

Figure 1: Block diagram	5
Figure 2: Pin connection (top view)	6
Figure 3: trise and tfall	10
Figure 4: tPD(L-H) and tPD(H-L)	10
Figure 5: Current limitation and cut-off	14
Figure 6: Open load off-state	15
Figure 7: VCC disconnection	16
Figure 8: GND disconnection.....	17
Figure 9: Active clamp equivalent principle schematic	18
Figure 10: Fast demag waveforms	19
Figure 11: Typical demagnetization energy (single pulse) at VCC = 24 V and TAMB = 125 °C	20
Figure 12: PowerSSO12 package outline.....	22
Figure 13: PowerSSO12 recommended footprint.....	24

1 Block diagram

Figure 1: Block diagram



2 Pin description

Figure 2: Pin connection (top view)

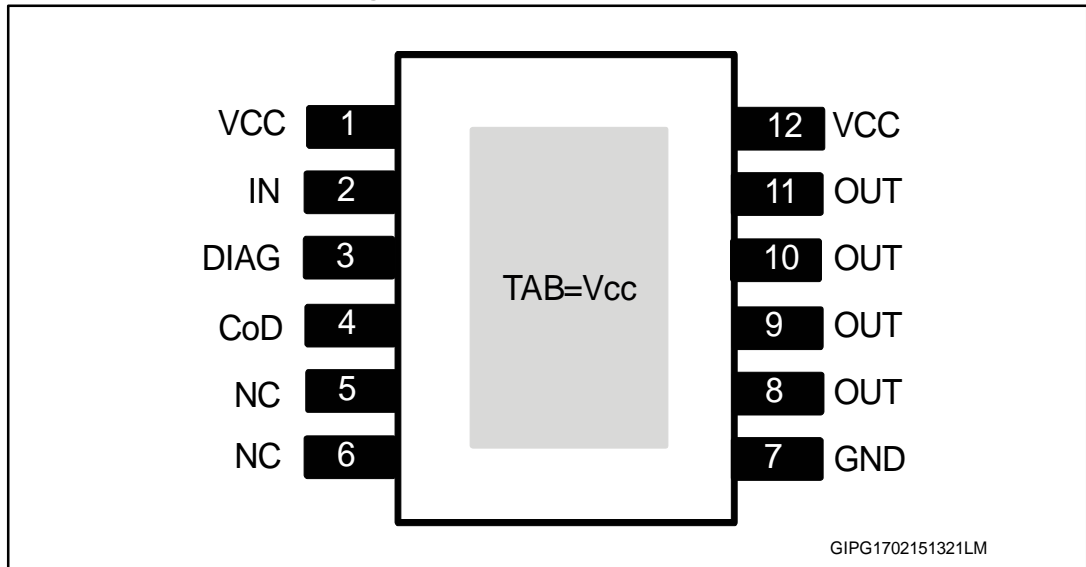


Table 2: Pin configuration

Number	Name	Function	Type
1, 12, TAB	VCC	Device supply voltage	Supply
2	IN	Channel input	Input
3	DIAG	Common diagnostic pin both for thermal shutdown, cut-off and open load	Output open drain
4	CoD	Cut-off delay pin, cannot be left floating. Connected to GND by 1 kΩ resistor to disable the cut-off function. Connect to a C _{CoD} capacitor to set the cut-off delay see Table 9: "Protection and diagnostic"	Input
5, 6	NC	Not connected	
7	GND	Device ground	Ground
8, 9, 10, 11	OUT	Channel power stage output	Output

2.1 IN

This pin drives the output stage to pin OUT. IN pin has internal weak pull-down resistors, see [Table 8: "Logic inputs"](#).

2.2 OUT

Output power transistor is in high-side configuration, with active clamp for fast demagnetization.

2.3 DIAG

This pin is used for diagnostic purpose and it is internally wired to an open drain transistor. The open drain transistor is turned on in case of junction thermal shutdown, cut-off, or open load in off-state.

2.4 CoD

This pin cannot be left floating and can be used to program the cut-off delay time t_{coff} , see [Table 9: "Protection and diagnostic"](#) through an external capacitor (C_{CoD}). The cut-off function can be completely disabled connecting the CoD pin to GND through 1 k Ω resistor: in this condition the output channel remains on in limitation condition, supplying the current to the load until the input is forced LOW or the thermal shutdown threshold is triggered or t_{coff} time elapses.

2.5 GND

IC ground.

2.6 VCC

IC supply voltage.

3 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	-0.3 to 65	V
V _{OUT}	Output channel voltage	V _{CC} -V _{clamp} to V _{CC} +0.3	V
I _{IN}	Input current	-10 to +10	mA
V _{IN}	IN voltage	V _{CC}	V
V _{COD}	Output cut-off voltage pin	5.5	V
I _{COD}	Input current on cut-off pin	-1 to +10	mA
V _{DIAG}	Fault voltage	V _{CC}	V
I _{DIAG}	Fault current	-5 to +10	mA
I _{CC} ⁽¹⁾	Maximum DC reverse current flowing through the IC from GND to V _{CC}	-250	mA
I _{OUT}	Output stage current	Internally limited	A
-I _{OUT} ⁽¹⁾	Maximum DC reverse current flowing through the IC from OUT to V _{CC}	5	
E _{AS} ⁽¹⁾	Single pulse avalanche energy (T _{AMB} = 125 °C, V _{CC} = 24 V, I _{load} = 1.15 H load = 24 Ohm)	800	mJ
P _{TOT}	Power dissipation at T _C = 25 °C ⁽²⁾	Internally limited	W
T _{STG}	Storage temperature range	-55 to 150	°C
T _J	Junction temperature	-40 to 150	

Notes:

⁽¹⁾Verified on application board with R_{th(ja)} = 49 °C/W

⁽²⁾(T_{JSD(MAX)}-T_C)/ R_{th(JA)}



Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
R _{th(JC)}	Thermal resistance junction-case	1	°C/W
R _{th(JA)}	Thermal resistance junction-ambient	49	



Package mounted on a 2-layer application board with Cu thickness = 35 µm, total dissipation area = 1.5 cm² connected by 6 vias.

4 Electrical characteristics

(8 V < V_{CC} < 60 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 5: Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Supply voltage		V _{UVON}		60	
V _{UVON}	Undervoltage on threshold		6.9		8	
V _{UVOFF}	Undervoltage off threshold		6.5		7.8	
V _{UVH}	Undervoltage hysteresis		0.15	0.5		
I _S	Supply current in off-state	V _{CC} = 24 V		300	500	μA
		V _{CC} = 60 V		350	600	
	Supply current in on-state	V _{CC} = 24 V		1	1.4	mA
		V _{CC} = 60 V		1.4	1.8	
I _{LGN}	GND disconnection output current	V _{GND} = V _{IN} = V _{CC} V _{OUT} = 0 V			1	mA

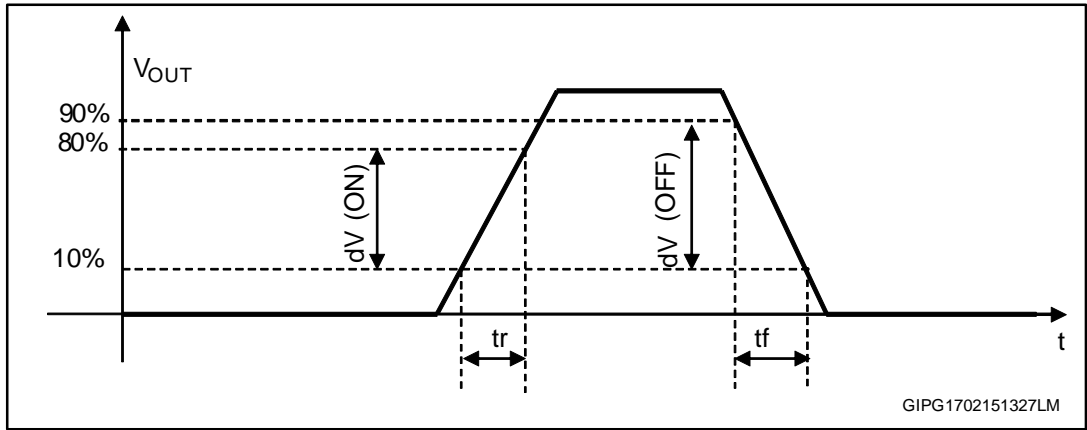
Table 6: Output stage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R _{DS(on)}	On-state resistance	V _{CC} = 24 V I _{OUT} = 1 A @ T _J = 25 °C		60		mΩ
		V _{CC} = 24 V I _{OUT} = 1 A @ T _J = 125 °C			120	
V _{OUT(OFF)}	Off-state output voltage	V _{IN} = 0 V and I _{OUT} = 0 A			2	V
I _{OUT(OFF)}	Off-state output current	V _{CC} = 24 V, V _{IN} = 0 V, V _{OUT} = 0 V			3	μA
		V _{CC} = 60 V, V _{IN} = 0 V, V _{OUT} = 0 V			10	
I _{OUT(OFF-min)}	Off-state output current	V _{IN} = 0 V, V _{OUT} = 4 V	-35		0	

Table 7: Switching (V_{CC} = 24 V; 125 °C > T_J > -40 °C, R_{LOAD} = 48 Ω)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _r	Rise time	I _{OUT} = 0.5 A		10		μs
t _f	Fall time			10		
t _{PD(H-L)}	Propagation delay time off			20		
t _{PD(L-H)}	Propagation delay time on			30		

Figure 3: trise and tfall



GIPG1702151327LM

Figure 4: $t_{PD(L-H)}$ and $t_{PD(H-L)}$

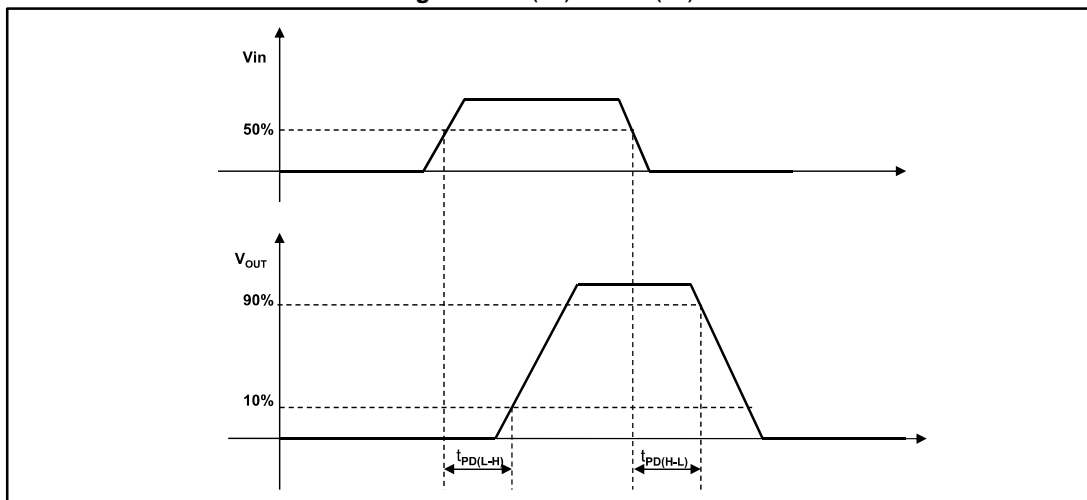


Table 8: Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.8	V
V_{IH}	Input high level voltage		2.2			
$V_{I(HYST)}$	Input hysteresis voltage			0.4		
I_{IN}	Input current	$V_{CC} = V_{IN} = 36\text{ V}$			200	μA
		$V_{CC} = V_{IN} = 60\text{ V}$			550	

Table 9: Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{clamp}	V_{CC} active clamp	$I_{CC} = 10\text{ mA}$	65.5	68.5	71.5	V
V_{demag}	Demagnetization voltage	$I_{OUT} = 0.5\text{ A}$; load = 1 mH	$V_{CC} - 71.5$	$V_{CC} - 68.5$	$V_{CC} - 65.5$	
V_{OLoff}	Open load (off-state) or short to V_{CC} detection threshold		2		4	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{BKT}	Open load blanking time				200	μs
V_{DIAG}	Voltage drop on DIAG	$I_{DIAG} = 4 \text{ mA}$			1	V
I_{DIAG}	DIAG pin leakage current	$V_{CC} \leq 36 \text{ V}$			110	μA
		$36 \text{ V} < V_{CC} \leq 60 \text{ V}$			180	
I_{LIM}	Output current limitation	$V_{CC} \leq 32 \text{ V}$, $R_{LOAD} \leq 10 \text{ m}\Omega$	2.6		4.3	A
t_{coff}	Cut-off current delay time	Programmable by the external capacitor on CoD pin. Cut-off is disabled when CoD pin is connected to GND through 1 k Ω resistor. $T_J < T_{JSD}$	$50 \times C_{COD}[\text{nf}] \pm 35\%^{(1)}$			μs
t_{res}	Output stage restart delay time	$T_J < T_{JSD}$	$32 \times t_{coff} [\mu s] \pm 40\%$			
T_{JSD}	Junction temperature shutdown		150	170	190	$^{\circ}C$
T_{JHYST}	Junction temperature thermal hysteresis			15		

Notes:

⁽¹⁾The formula is guaranteed in the range $10 \text{ nF} \leq C_{COD} \leq 100 \text{ nF}$.

5 Output logic

Table 10: Output stage truth table

Operation	IN	OUT	DIAG
Normal	L	L	H
	H	H	H
Cut-off	L	L	L
	H	L	L
Overtemperature	L	L	L
	H	L	L
Open load	L	H (external pull-up resistor is used)	L (external pull-up resistor is used)
	H	H	H
UVLO	X	L	X
	X	L	X

6 Protection and diagnostic

The IC integrates several protections to ease the design of a robust application.

6.1 Undervoltage lock-out

The device turns off if the supply voltage falls below the turn-off threshold ($V_{UV(off)}$). Normal operation restarts after V_{CC} exceeds the turn-on threshold ($V_{UV(on)}$). Turn-on and turn-off thresholds are defined in [Table 5: "Supply"](#).

6.2 Overtemperature

The output stage turns off when its internal junction temperature (T_J) exceeds the shutdown threshold T_{JSD} . Normal operation restarts when T_J comes back below the reset threshold ($T_{JSD} - T_{JHYST}$), see [Table 9: "Protection and diagnostic"](#). The internal fault signal is set when the channel is off due to thermal protection and it is reset when the junction triggers the reset threshold. This same behavior is reported on DIAG pin.

6.3 Cut-off

The output current of the power stage is internally limited at the fixed I_{LIM} threshold.

The IPS160H implements the cut-off feature which limits the duration of the current limitation condition.

The duration of the current limitation condition (t_{coff}) can be set by a capacitor (C_{CoD}) placed between CoD and GND pins. The design rule for C_{CoD} is:

$$t_{coff[us]} \pm 35\% = 50 \times C_{cod[nF]}$$

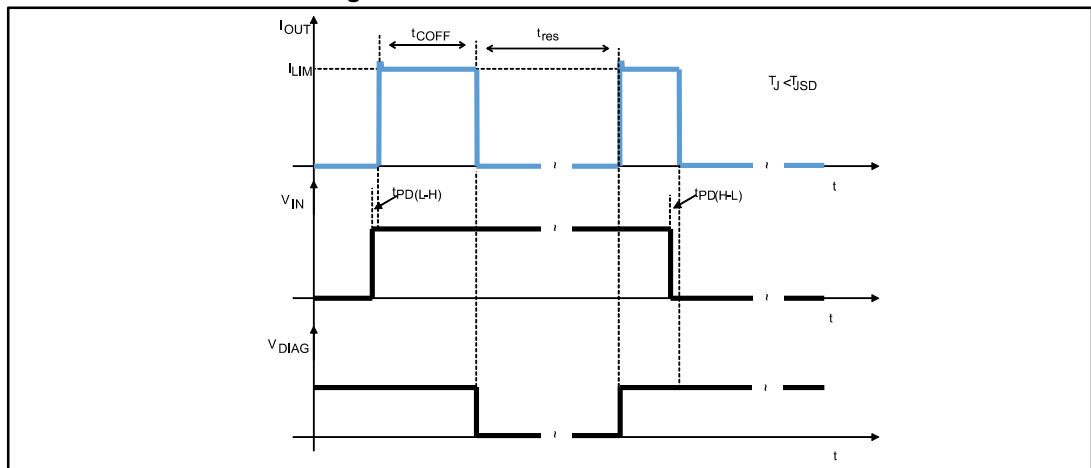
The drift of $\pm 35\%$ is guaranteed in the range of $10 \text{ nF} < C_{cod} < 100 \text{ nF}$; lower capacitance than 10 nF can be used.

If I_{LIM} threshold is triggered, the output stage remains in the current limitation condition ($I_{OUT} = I_{LIM}$) no longer than t_{coff} . If t_{coff} elapses, the output stage turns off and restarts after the t_{res} restart time.

Thermal shutdown protection has higher priority than cut-off:

- IC is forced off if T_{JSD} is triggered before t_{coff} elapses
- if T_{JSD} is triggered, IC is maintained off even after the t_{res} has elapsed and until the T_J decreases below $T_{JSD} - T_{JHYST}$

Figure 5: Current limitation and cut-off



The fault condition is reported on the DIAG pin. The internal cut-off flag signal is latched at output switch-off and released after the time t_{res} , the same behavior is reported on DIAG pin.

The status of the DIAG is independent on the IN pin status.

If CoD pin is connected to GND through 1 kΩ resistor (cut-off feature disabled), when the output channel triggers the limitation threshold, it remains on, in current limitation condition, until the input becomes LOW or the thermal protection threshold is triggered.

In case of low ambient temperature conditions ($T_{AMB} < -20\text{ °C}$) and high supply voltage ($V_{CC} > 36\text{ V}$) the cut-off function needs activating in order to avoid IC permanent damages. The following table reports the suggested cut-off delay for the different operating voltage.

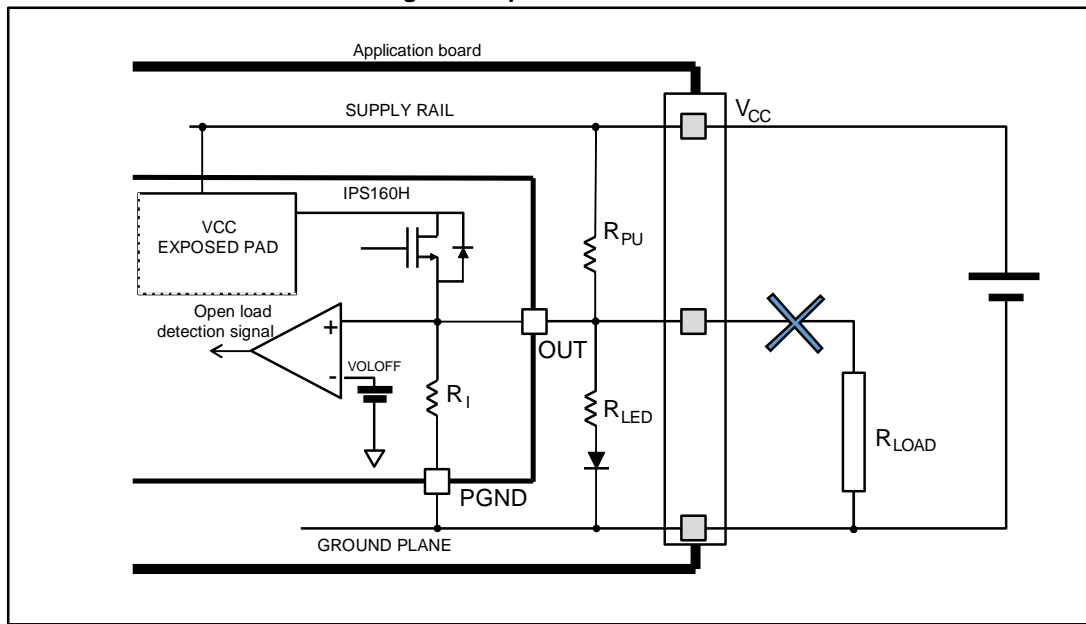
Table 11: Minimum cut-off delay for T_{AMB} less than -20 °C

V_{CC} [V]	Cut-off delay [μs]	Cut-off capacitance [nF]
36-48	100	2.2
48-60	50	1

6.4 Open load in off-state

The IPS160H provides the open load detection feature which detects if the load is disconnected from the OUT pin. This feature can be activated by a resistor (R_{PU}) between OUT and VCC pins.

Figure 6: Open load off-state



In case of wire break and during the OFF state ($I_N = \text{low}$), the output voltage V_{OUT} rises according to the partitioning between the external pull-up resistor and the internal resistance of the IC ($R_I = 115 \text{ k}\Omega$).

The effect of the LED (if any) on the output pin has to be considered as well. In case of wire break and during the ON state ($I_N = \text{high}$), the output voltage V_{OUT} is pulled up to V_{CC} by the low resistive integrated switch. If the load is not connected, in order to guarantee the correct open load signalization it must result:

$$V_{OUT} > V_{OLoff(max)}$$

Referring to the circuit in figure 6:

$$V_{OUT} = V_{CC} - R_{PU} \times I_{PU} = V_{CC} - R_{PU} \times (I_{RI} + I_{LED} + I_{RL})$$

therefore:

$$R_{PU} < \frac{V_{CC(min)} - V_{OLoff(max)}}{\left(\frac{V_{OLoff(max)} - V_{LED}}{R_I} + \frac{V_{OLoff(max)} - V_{LED}}{R_{LED}}\right)}$$

If the load is connected, in order to avoid any false signalization of the open load, it must result as follows:

$$V_{OUT} < V_{OLoff(min)}$$

By taking into account the circuit in figure 6:

$$V_{OUT} = V_{CC} - R_{PU} \times I_{PU} = V_{CC} - R_{PU} \times \left(\frac{V_{OUT}}{R_I} + \frac{V_{OUT} - V_{LED}}{R_{LED}} + \frac{V_{OUT}}{R_L}\right)$$

so:

$$R_{PU} > \frac{V_{CC(max)} - V_{OLoff(min)}}{\left(\frac{V_{OLoff(min)}}{R_I} + \frac{V_{OLoff(min)} - V_{LED}}{R_{LED}} + \frac{V_{OLoff(min)}}{R_L}\right)}$$

The fault condition is reported on the DIAG pin and the fault reset occurs when load is reconnected.

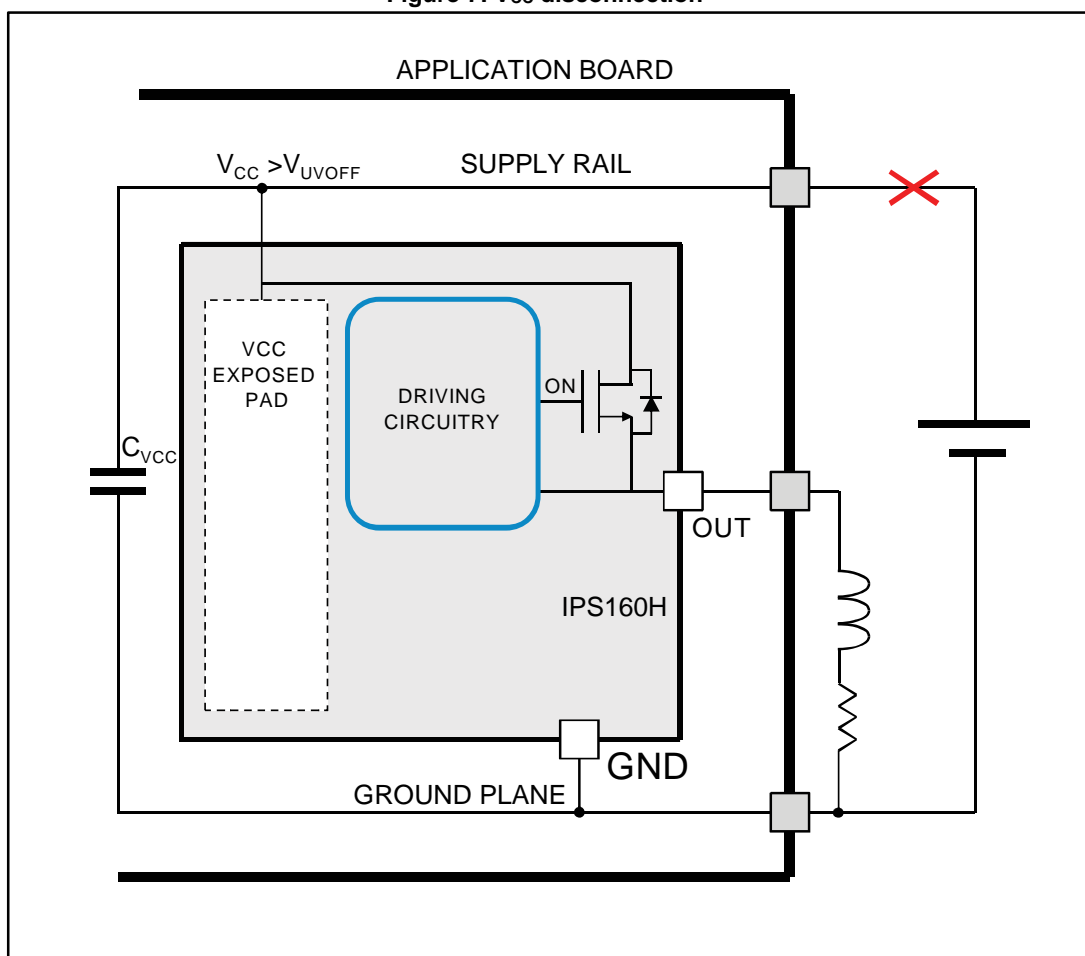
If the channel is switched on by I_N pin, the fault condition is no longer detected.

When inductive load is driven, some ringing of the output voltage may be observed at the end of the demagnetization. In fact, the load is completely demagnetized when $I_{LOAD} = 0$ A and the OUT pin remains floating until next turn-on. In order to avoid a fake signalization of the open load event driving inductive loads, the open load signal is masked for t_{BKT} . So, the open load is reported on the DIAG pin with a delay of t_{BKT} and if the open load event is triggered for more than t_{BKT} .

6.5 V_{CC} disconnection protection

The IC is protected despite the V_{CC} disconnection event. This event is intended as the disconnection of the V_{CC} wire from the application board, see figure below. When this condition happens, the IC continues working normally until the voltage on the V_{CC} pin is $\geq V_{UV(OFF)}$. Once the $V_{UV(OFF)}$ is triggered, the output channel is turned off independently on the input status. In case of inductive load, if the V_{CC} is disconnected while the output channel is still active, the IC allows the discharge of the energy still stored in the inductor through the integrated power switch.

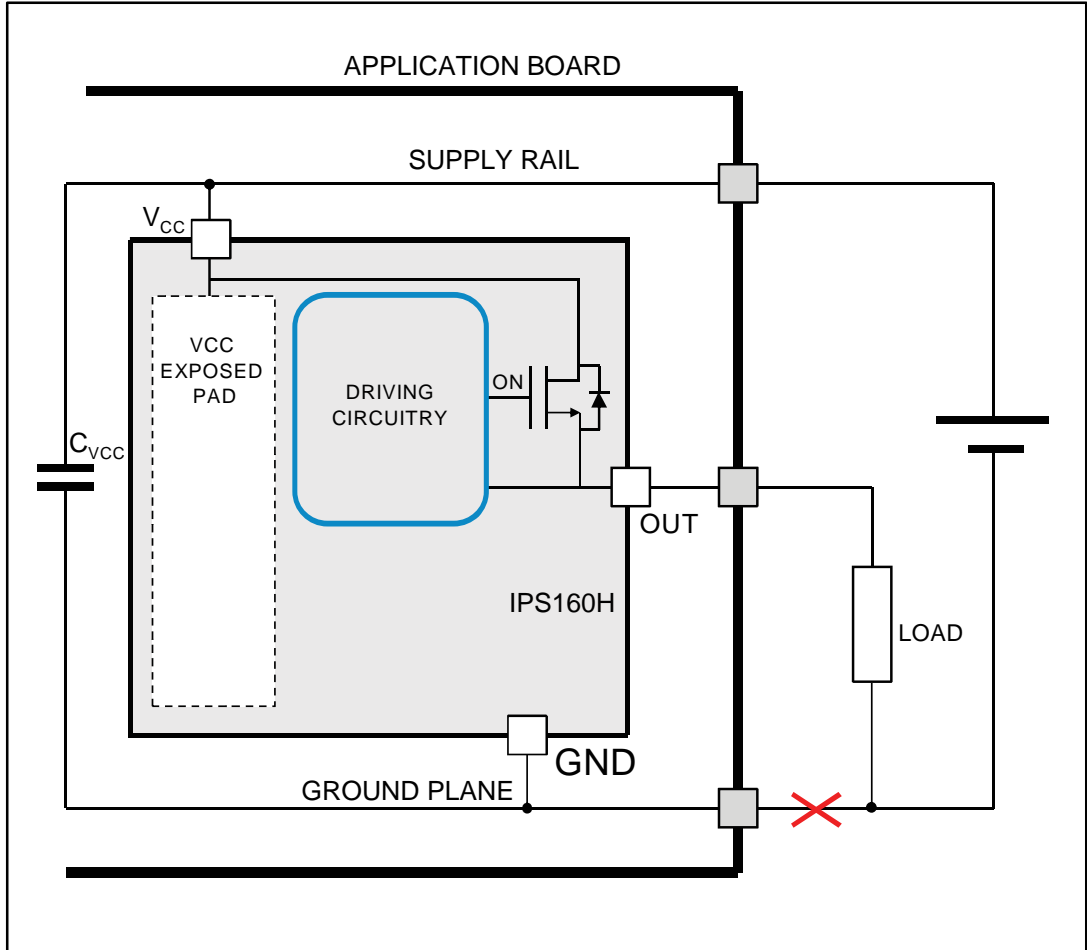
Figure 7: V_{CC} disconnection



6.6 GND disconnection protection

GND disconnection is intended as the disconnection event of the application ground, see figure below. When this event happens, the IC continues working normally until the voltage between V_{CC} and GND pins of the IC results $\geq V_{UVOFF}$. The voltage on GND pin of the IC rises up to the supply rail voltage level. In case of GND disconnection event, a current (I_{LGND}) flows through OUT pin. *Table 8: "Logic inputs"* reports $I_{OUT} = I_{LGND}$ for the worst case of GND disconnection event in case of output shorted to ground.

Figure 8: GND disconnection



7 Active clamp

Active clamp is also known as fast demagnetization of inductive loads or fast current decay. When a high-side driver turns off an inductance, an undervoltage is detected on output.

The OUT pin is pulled down to V_{demag} . The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at about V_{demag} until the load energy has been dissipated. The energy is dissipated both in IC internal switch and in load resistance.

Figure 9: Active clamp equivalent principle schematic

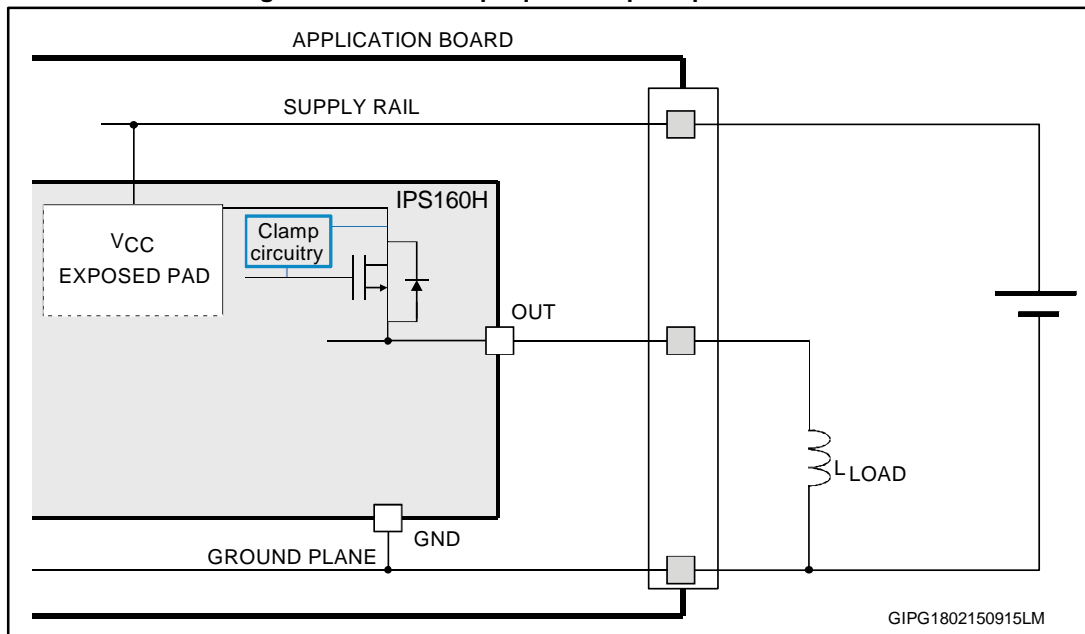
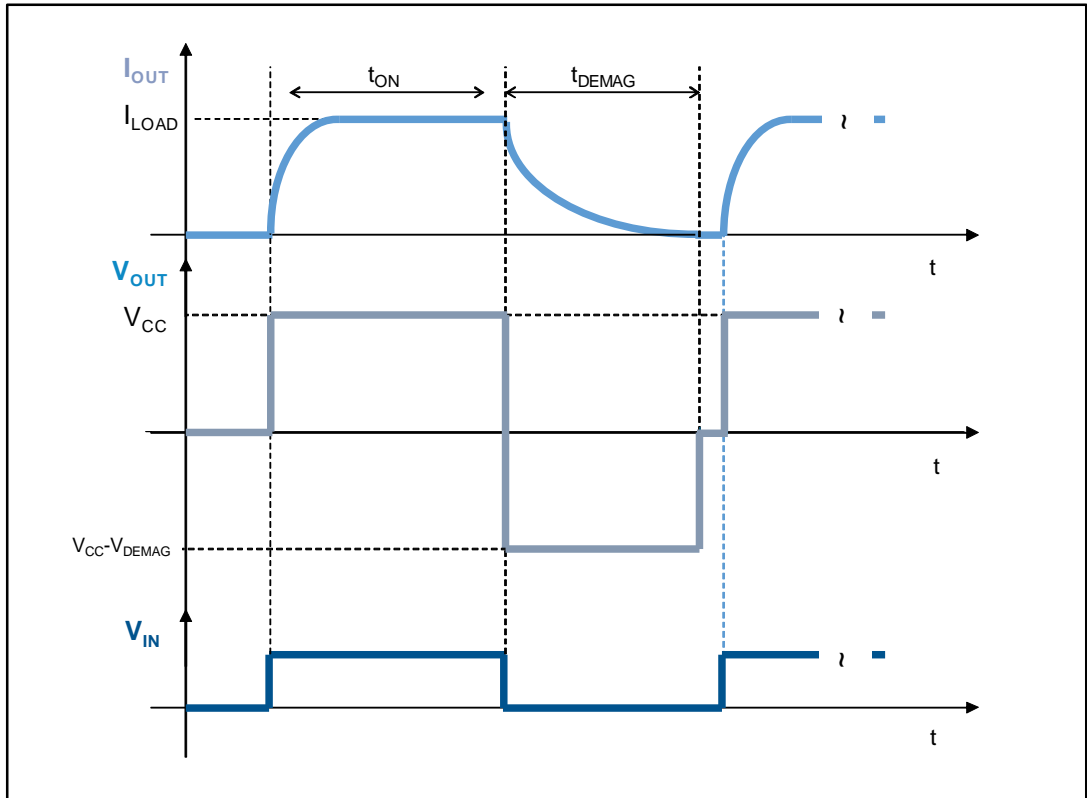
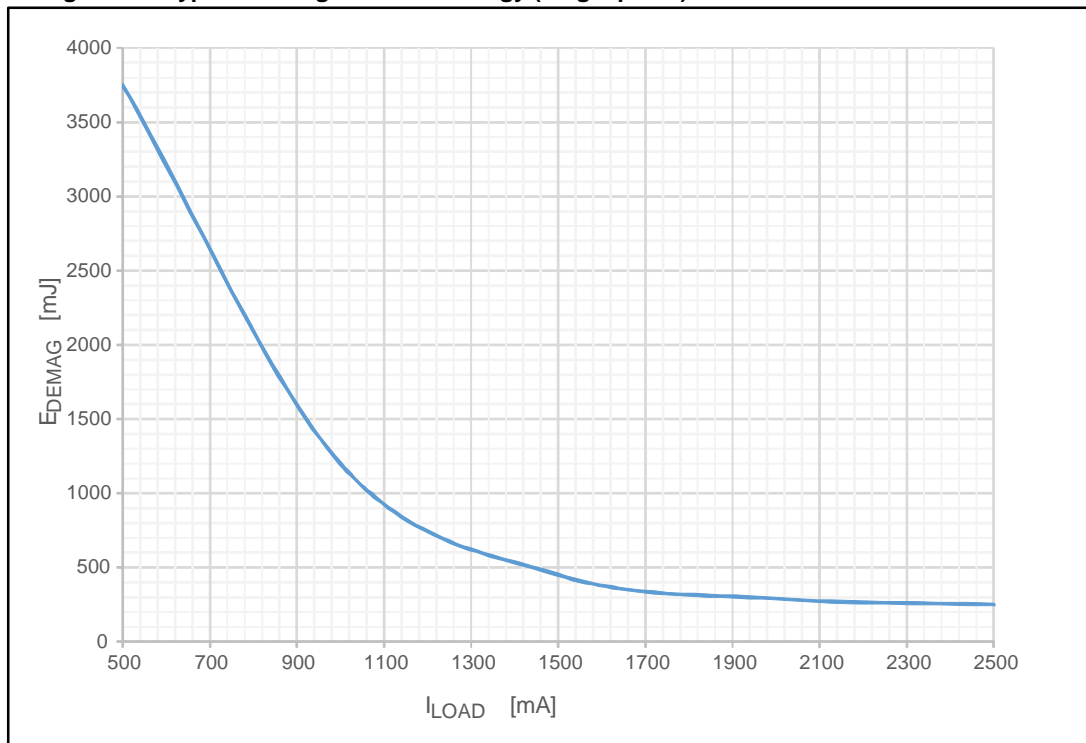


Figure 10: Fast demag waveforms



The demagnetization of inductive load causes a huge electrical and thermal stress to the IC. The curve plotted below shows the maximum demagnetization energy that the IC can support in a single demagnetization pulse with $V_{CC} = 24\text{ V}$ and $T_{AMB} = 125\text{ }^\circ\text{C}$. If higher demagnetization energy is required then an external free-wheeling Schottky diode has to be connected between OUT (cathode) and GND (anode) pins. Note that in this case the fast demagnetization is inhibited.

Figure 11: Typical demagnetization energy (single pulse) at $V_{CC} = 24\text{ V}$ and $T_{AMB} = 125\text{ °C}$



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 PowerSSO12 package information

Figure 12: PowerSSO12 package outline

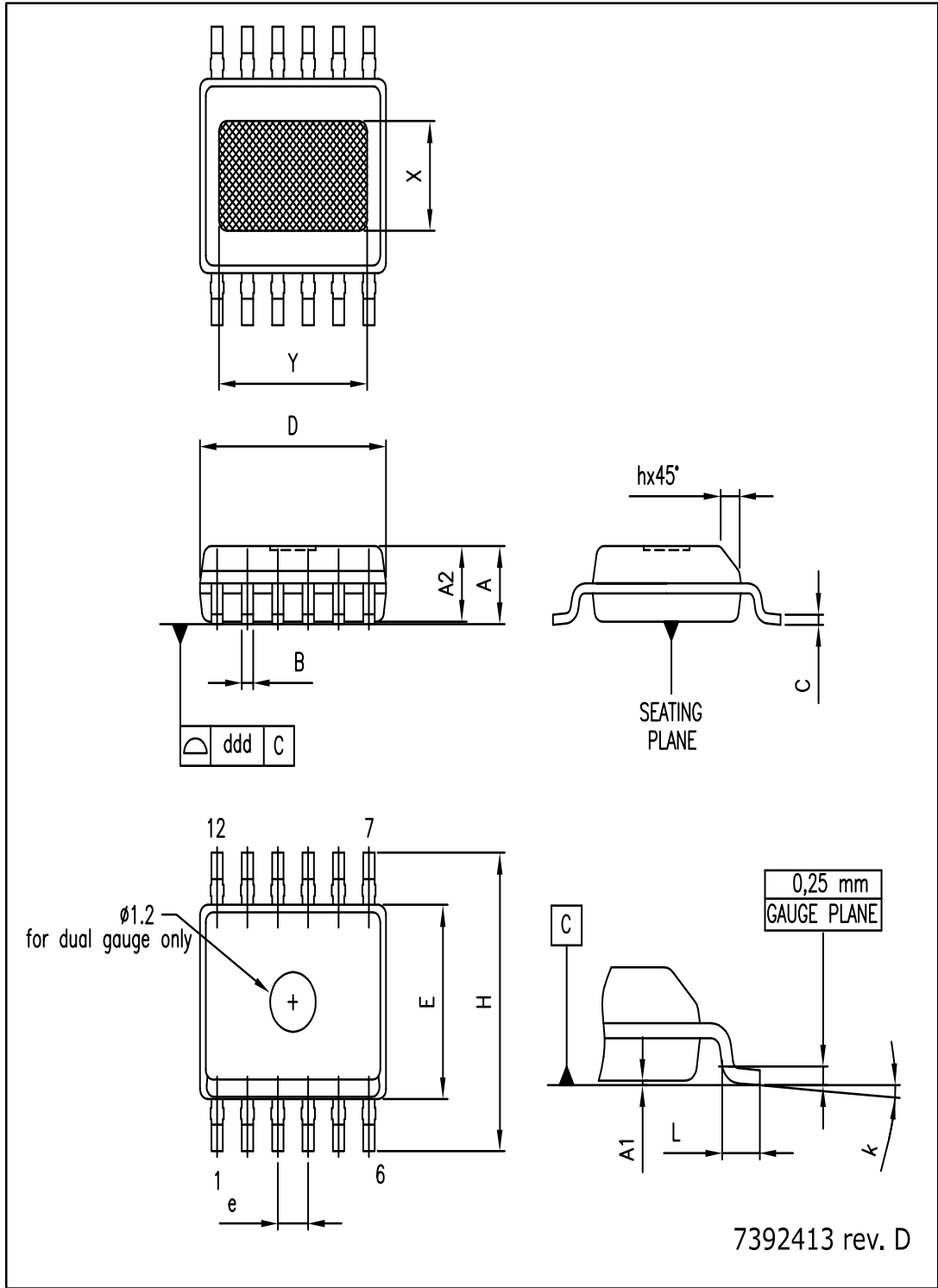


Table 12: PowerSSO12 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.250		1.700
A1	0.000		0.100
A2	1.100		1.600
B	0.230		0.410
C	0.190		0.250
D	4.800		5000
E	3.800		4000
e		0.800	
H	5800		6.200
h	0.250		0.55
L	0.400		0.1270
k	0d		8d
X	1.900		2500
Y	3.600		4.200
ddd			0.100



Dimension D doesn't include mold flash protrusions or gate burrs. Mold flash protrusions or gate burrs don't exceed 0.15 mm in total both side.

9 Revision history

Table 13: Document revision history

Date	Revision	Changes
19-Mar-2015	1	Initial release.
04-Nov-2015	2	Minor text changes throughout the document. Added figure 7 titled "V _{CC} disconnection", figure 10 titled: "Fast demag waveforms" and figure 11 titled "Typical demagnetization energy (single pulse) at V _{CC} = 24 V and T _{AMB} = 125 °C.
11-May-2016	3	Updated tables titled: "Supply", "Switching (V _{CC} = 24 V; 125 °C > T _J > -40 °C, R _{LOAD} = 48 Ω)" and "Protection diagnostic". Changed figures titled: "t _{PD(L-H)} and t _{PD(H-L)} " and "Current limitation and cut-off".
20-May-2016	4	Document status promoted from preliminary to production data.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved