EVB71112

868/915MHz Receiver
Evaluation Board Description

Features

- ❑ Double superhet architecture for high degree of image rejection
- ❑ FSK for digital data and FM reception for analog signal transmission
- ❑ FSK/FM demodulation with phase-coincidence demodulator
- ❑ Low current consumption in active mode and very low standby current
- ❑ Switchable LNA gain for improved dynamic range
- ❑ RSSI allows signal strength indication and ASK detection
- ❑ Surface mount package LQFP32

Ordering Information

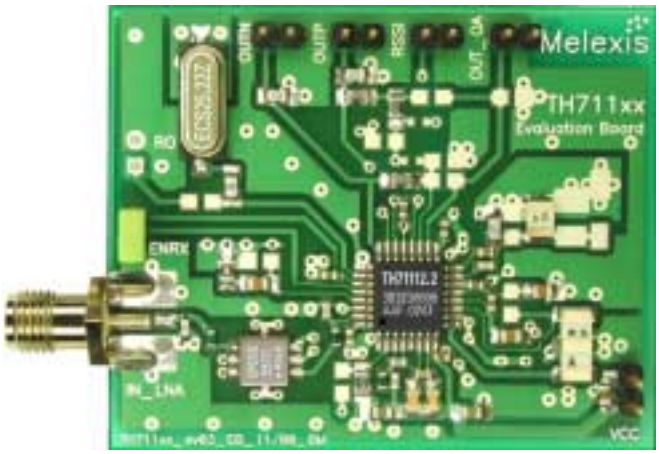
Part No.

EVB71112-868-FSK
EVB71112-868-ASK
EVB71112-915-FSK
EVB71112-915-ASK

Application Examples

- ❑ General digital and analog 868 MHz or 915 MHz ISM band usage
- ❑ Low-power telemetry
- ❑ Alarm and security systems
- ❑ Remote Keyless Entry (RKE)
- ❑ Tire Pressure Monitoring System (TPMS)
- ❑ Garage door openers
- ❑ Home automation
- ❑ Pagers

Evaluation Board



General Description

The TH71112 FSK/FM/ASK double-conversion superheterodyne receiver IC is designed for applications in the European 868 MHz industrial-scientific-medical (ISM) band, according to the EN 300 220 telecommunications standard. It can also be used for any other system with carrier frequencies ranging from 800 MHz to 930 MHz (e.g. for applications in the US 915 MHz ISM band).

Document Content

1 Theory of Operation 3
1.1 General 3
1.2 Technical Data Overview 3
1.3 Block Diagram 4
1.4 Mode Configurations 4
1.5 LNA GAIN Control 4
1.6 Frequency Planning 5
1.6.1 Selected Frequency Plans 5
2 FSK Application Circuits 6
2.1 PCB Top View for FSK Reception 7
2.2 Board Component Values for FSK (Fig. 2) 8
3 ASK Application Circuits 9
3.1 PCB Top View for ASK Reception 10
3.2 Board Component Values for ASK (Fig. 3) 11
4 Package Dimensions 12
5 Reliability Information 13
6 ESD Precautions 13
7 Disclaimer 14

1 Theory of Operation

1.1 General

With the TH71112 receiver chip, various circuit configurations can be arranged in order to meet a number of different customer requirements. For FM/FSK reception the IF tank used in the phase coincidence demodulator can be constituted either by a ceramic resonator or an LC tank (optionally with a varactor diode to create an AFC circuit). In ASK configuration, the RSSI signal is feed to an ASK detector, which is constituted by the operational amplifier.

Demodulation	Type of receiver
FM / FSK	narrow-band RX with ceramic demodulation tank
FM / FSK	wide-band RX with LC demodulation tank
ASK	RX with RSSI-based demodulation

The superheterodyne configuration is double conversion where MIX1 and MIX2 are driven by the internal local oscillator signals LO1 and LO2, respectively. This allows a high degree of image rejection, achieved in conjunction with an RF front-end filter. Efficient RF front-end filtering is realized by using a SAW, ceramic or helix filter in front of the LNA and by adding an LC filter at the LNA output.

A single-conversion variant, called TH71111, is also available. Both Receiver ICs have the same die. At the TH71111 the second mixer MIX2 operates as an amplifier.

The TH71112 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) for generation of the first and second local oscillator signals LO1 and LO2
- Parts of the PLL SYNTH are the high-frequency VCO1, the feedback dividers DIV_16 and DIV_2, a phase-frequency detector (PFD) with charge pump (CP) and a crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (IF1)
- Second mixer (MIX2) for down-conversion of the IF1 to the second IF (IF2)
- IF amplifier (IFA) to amplify and limit the IF2 signal and for RSSI generation
- Phase coincidence demodulator (DEMOD) with third mixer (MIX3) to demodulate the IF signal
- Operational amplifier (OA) for data slicing, filtering and ASK detection
- Bias circuitry for bandgap biasing and circuit shutdown

1.2 Technical Data Overview

- ❑ Input frequency range: 800 MHz to 930 MHz
- ❑ Power supply range: 2.3 V to 5.5 V @ ASK
- ❑ Temperature range: -40 °C to +85 °C
- ❑ Standby current: 50 nA
- ❑ Operating current: 7.5 mA at low gain mode
  9.2 mA at high gain mode
- ❑ Sensitivity: -109 dBm [1] with 40 kHz IF filter BW
- ❑ Sensitivity: -102 dBm [2] with 150 kHz IF filter BW
- ❑ Range of first IF1: 10 MHz to 80 MHz
- ❑ Range of second IF2: 400 kHz to 22 MHz
- ❑ Maximum data rate: 80 kbit/s NRZ
- ❑ Maximum input level: -10 dBm at ASK
  0 dBm at FSK
- ❑ Image rejection: > 65 dB (e.g. with SAW front-end filter and at 10.7 MHz IF2)
- ❑ Spurious emission: < -70 dBm
- ❑ Input frequency acceptance: ±50 kHz (with AFC option)
- ❑ RSSI range: 70 dB
- ❑ Frequency deviation range: ±4 kHz to ±120 kHz
- ❑ Maximum analog modulation frequency: 15 kHz

1) at ± 8 kHz FSK deviation, BER = $3 \cdot 10^{-3}$, phase-coincidence demodulation and SAW front-end filter loss
2) at ± 50 kHz FSK deviation, BER = $3 \cdot 10^{-3}$, phase-coincidence demodulation and SAW front-end filter loss

For more detailed information, please refer to the latest TH71112 data sheet revision.

1.3 Block Diagram

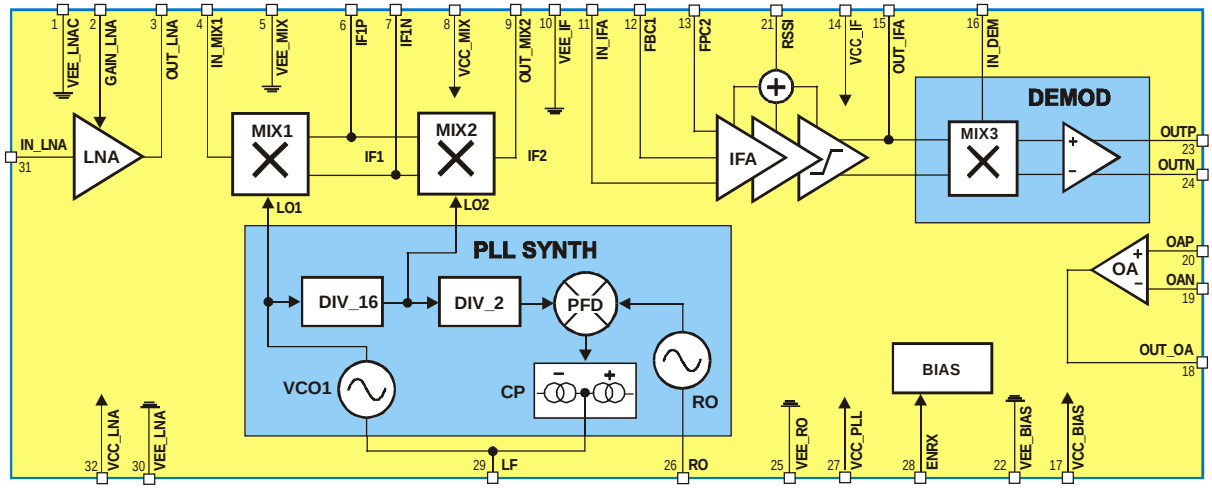


Fig. 1: TH71112 block diagram

1.4 Mode Configurations

ENRX	Mode	Description
0	RX standby	RX disabled
1	RX active	RX enable

Note: ENRX are pulled down internally

1.5 LNA GAIN Control

V_{GAIN_LNA}	Mode	Description
< 0.8 V	HIGH GAIN	LNA set to high gain
> 1.4 V	LOW GAIN	LNA set to low gain

Note: hysteresis between gain modes to ensure stability

1.6 Frequency Planning

Frequency planning is straightforward for single-conversion applications because there is only one IF that might be chosen, and then the only possible choice is low-side or high-side injection of the LO signal (which is now the one and only LO signal in the receiver).

The receiver's double-conversion architecture requires careful frequency planning. Besides the desired RF input signal, there are a number of spurious signals that may cause an undesired response at the output. Among them are the image of the RF signal (that must be suppressed by the RF front-end filter), spurious signals injected to the first IF (IF1) and their images which could be mixed down to the same second IF (IF2) as the desired RF signal (they must be suppressed by the LC filter at IF1 and/or by low-crosstalk design).

By configuring the TH71112 for double conversion and using its internal PLL synthesizer with fixed feedback divider ratios of N1 = 16 (DIV_16) and N2 = 2 (DIV_2), four types of down-conversion are possible: low-side injection of LO1 and LO2 (**low-low**), LO1 low-side and LO2 high-side (**low-high**), LO1 high-side and LO2 low-side (**high-low**) or LO1 and LO2 high-side (**high-high**). The following table summarizes some equations that are useful to calculate the crystal reference frequency (REF), the first IF (IF1) and the VCO1 or first LO frequency (LO1), respectively, for a given RF and second IF (IF2).

Injection type	high-high	low-low	high-low	low-high
REF	(RF – IF2)/30	(RF – IF2)/34	(RF + IF2)/30	(RF + IF2)/34
LO1	32•REF	32•REF	32•REF	32•REF
IF1	LO1 – RF	RF – LO1	LO1 – RF	RF – LO1
LO2	2•REF	2•REF	2•REF	2•REF
IF2	LO2 – IF1	IF1 – LO2	IF1 – LO2	LO2 – IF1

1.6.1 Selected Frequency Plans

The following table depicts crystal, LO and image signals considering the examples of 868.3 MHz and 915 MHz RF reception at IF2 = 10.7 MHz.

Signal type	RF = 868.3 MHz	RF = 868.3 MHz	RF = 868.3 MHz	RF = 868.3 MHz	RF = 915 MHz	RF = 915 MHz	RF = 915 MHz	RF = 915 MHz
Injection type	high-high	**low-low**	high-low	low-high	high-high	**low-low**	high-low	low-high
REF / MHz	28.58667	**25.22353**	29.3	25.85294	30.14333	**26.59706**	30.85667	27.22647
LO1 / MHz	914.77333	**807.15294**	937.6	827.29412	964.58667	**851.10588**	987.41333	871.24706
IF1 / MHz	46.47333	**61.14706**	69.3	41.00588	49.58667	**63.89412**	72.41333	43.75294
LO2 / MHz	57.17333	**50.44706**	58.6	51.70588	60.28667	**53.19412**	61.71333	54.45294
RF image/MHz	961.24667	**746.00588**	1006.9	786.28824	1014.17	**787.21176**	1059.83	827.49412
IF1 image/MHz	67.87333	**39.74706**	47.9	62.40588	70.98667	**42.49412**	51.01333	65.15294

The selection of the reference crystal frequency is based on some assumptions. As for example: the first IF and the image frequencies should not be in a radio band where strong interfering signals might occur (because they could represent parasitic receiving signals), the LO1 signal should be in the range of 800 MHz to 930 MHz (because this is the optimum frequency range of the VCO1). Furthermore the first IF should be as high as possible to achieve highest RF image rejection. The columns in bold depict the selected frequency plans to receive at 868.3 MHz and 915 MHz, respectively.

2 FSK Application Circuits

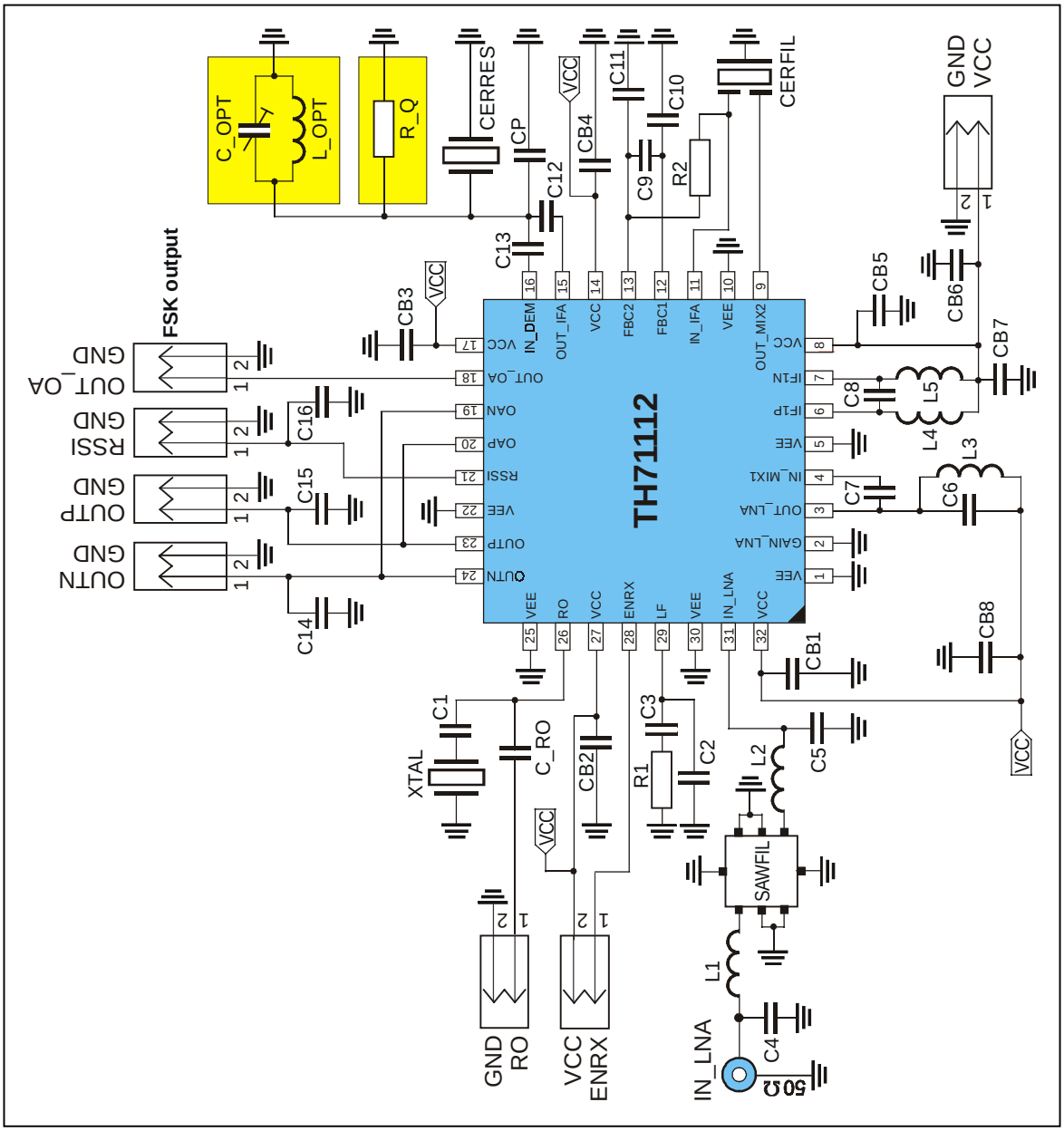
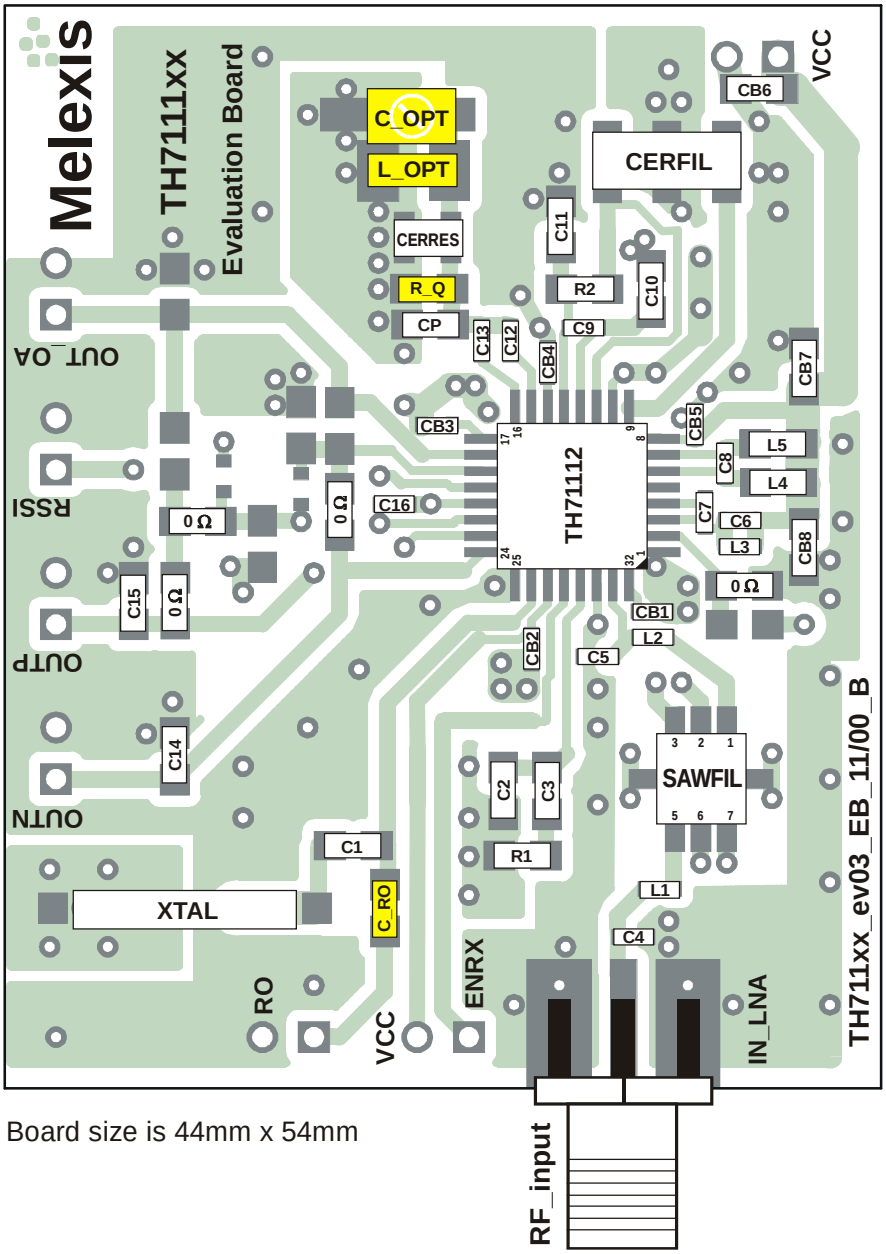


Fig. 2: Circuit diagram for FSK reception

2.1 PCB Top View for FSK Reception

Board layout data in Gerber format is available



Board size is 44mm x 54mm

2.2 Board Component Values for FSK (Fig. 2)

Part	Size	Value @ 868.3 MHz	Value @ 915 MHz	Tolerance	Description
C1	0805	15 pF	15 pF	±10%	crystal series capacitor
C2	0805	NIP	NIP	±10%	optional loop filter capacitor
C3	0805	1 nF	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	NIP	±5%	capacitor to match to SAW filter input
C5	0603	2.7 pF	NIP	±5%	capacitor to match to SAW filter output
C6	0603	NIP	NIP	±5%	LNA output tank capacitor
C7	0603	1.2 pF	0.47 pF	±5%	MIX1 input matching capacitor
C8	0603	22 pF	22 pF	±5%	IF1 tank capacitor
C9	0805	33 nF	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	1 nF	±10%	IFA feedback capacitor
C12	0603	1.5 pF	1.5 pF	±5%	DEMOD phase-shift capacitor
C13	0603	680 pF	680 pF	±10%	DEMOD coupling capacitor
CP	0805	10 – 12 pF	10 –12 pF	±5%	CERRES tuning capacitor
C14	0805	10 – 47 pF	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C15	0805	10 – 47 pF	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C16	0603	1.5 nF	1.5 nF	±10%	RSSI output low-pass capacitor
CB1 to CB5 CB7 to CB8	0603	330 pF	330 pF	±10%	blocking capacitor for VCC
CB6	0805	33 nF	33 nF	±10%	blocking capacitor for VCC
R1	0805	10 kΩ	10 kΩ	±10%	loop filter resistor
R2	0805	390 Ω	390 Ω	±5%	CERFIL output matching resistor
L1	0603	12 nH	18 nH	±5%	Inductor, to match SAW filter
L2	0603	12 nH	C=220 pF	±5%	Inductor (capacitor), to match SAW filter
L3	0603	6.8 nH	6.8 nH	±5%	LNA output tank inductor
L4	0805	100 nH	100 nH	±5%	IF1 tank inductor
L5	0805	100 nH	100 nH	±5%	IF1 tank inductor
L_OPT	1006	NIP	NIP	±5%	demodulator phase shift inductor, **only required at FSK/FM with LC resonator**
C_OPT	3mm	NIP	NIP	±5%	demodulator phase shift capacitor, **only required at FSK/FM with LC resonator**
R_Q	0805	NIP	NIP	±5%	optional lower-Q resistor, **only required at FSK/FM with LC resonator**
C_RO	0805	330 pF	330 pF	±5%	optional capacitor **to couple external RO signal**
XTAL	HC49 SMD	25.22353 MHz @ RF = 868.3 MHz	26.59706 MHz @ RF = 915 MHz	±25ppm calibr. ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\,max}$ = 7 pF, $R_{m,\,max}$ = 50 Ω
SAWFIL	QCC8C	B3570 (f_0 = 868.30 MHz)		B_{3dB} = 1.7 MHz	low-loss SAW filter from EPCOS
			B3569 (f_0 = 914.50MHz)	B_{3dB} = 25 MHz	
CERFIL	Leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	
CERRES	SMD type	CDACV10.7MG18-A Murata	CDACV10.7MG18-A Murata		ceramic demodulator tank, **not required at FSK/FM with LC resonator**

NIP – not in place, may be used optionally

3 ASK Application Circuits

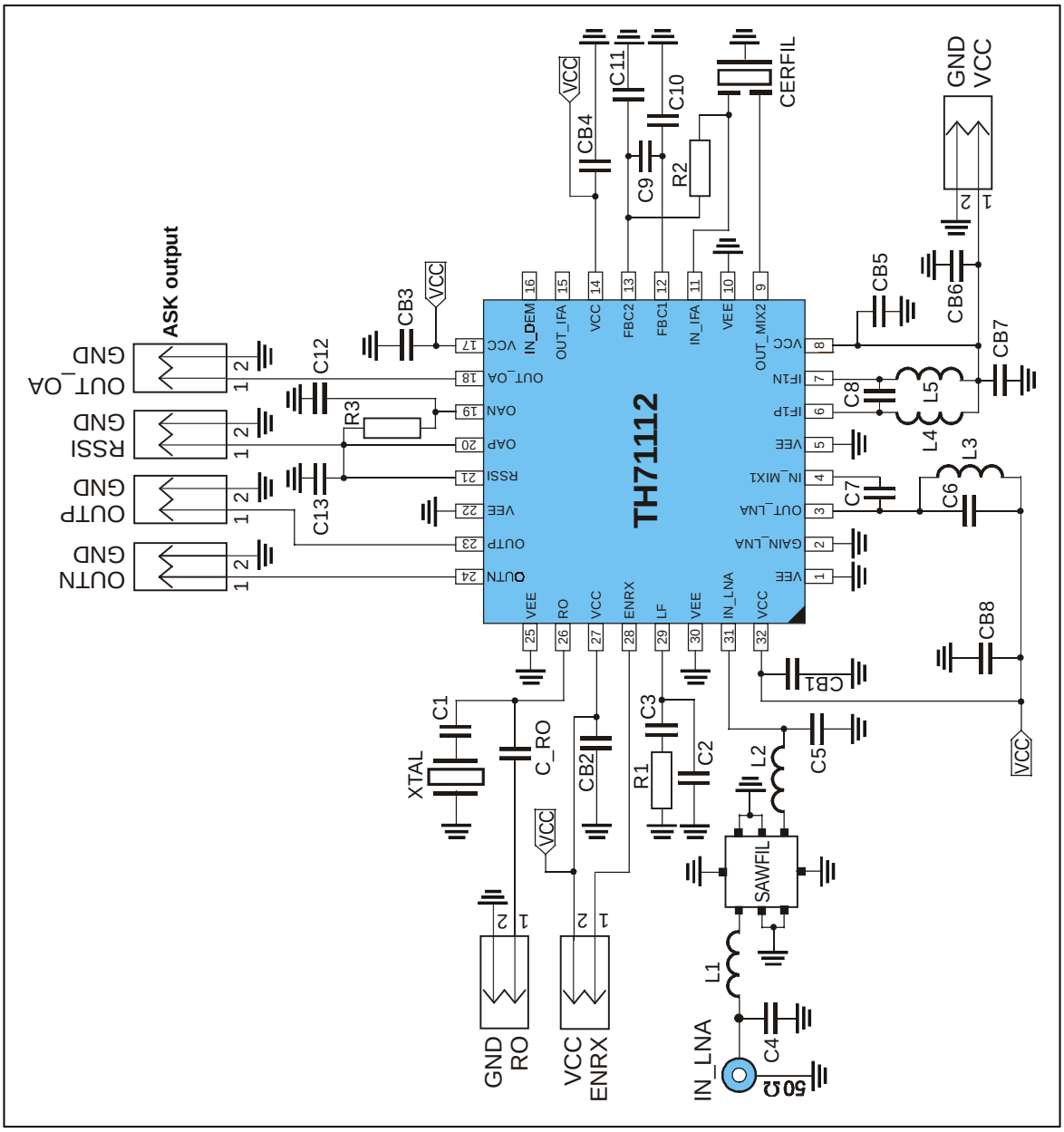
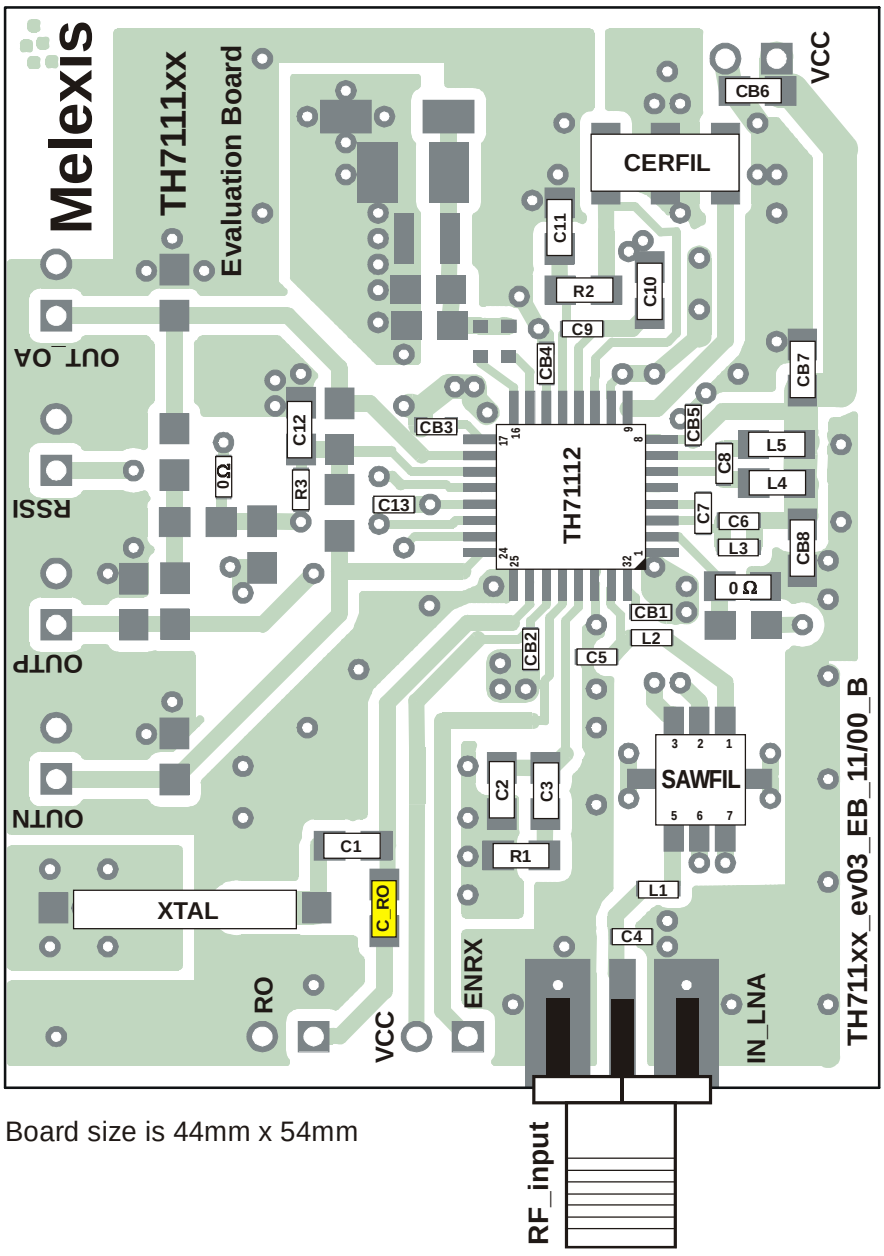


Fig. 3: Circuit diagram for ASK reception

3.1 PCB Top View for ASK Reception

Board layout data in Gerber format is available



Board size is 44mm x 54mm

3.2 Board Component Values for ASK (Fig. 3)

Part	Size	Value @ 868.3 MHz	Value @ 915 MHz	Tolerance	Description
C1	0805	15 pF	15 pF	±10%	crystal series capacitor
C2	0805	NIP	NIP	±10%	optional loop filter capacitor
C3	0805	1 nF	1 nF	±10%	loop filter capacitor
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C10	0603	1 nF	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	1 nF	±10%	IFA feedback capacitor
C12	0805	1 nF to 100 nF	1 nF to 100 nF	±10%	ASK data slicer capacitor, depending on data rate
C13	0603	1.5 nF	1.5 nF	±10%	RSSI output low-pass capacitor
CB1 to CB5 CB7 to CB8	0603	330 pF	330 pF	±10%	blocking capacitor for VCC
CB6	0805	33 nF	33 nF	±10%	blocking capacitor for VCC
R1	0805	10 kΩ	10 kΩ	±10%	loop filter resistor
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			B3569 (f_0 = 914.50MHz)	B_{3dB} = 25 MHz	
CERFIL	Leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filters from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	

NIP – not in place, may be used optionally

4 Package Dimensions

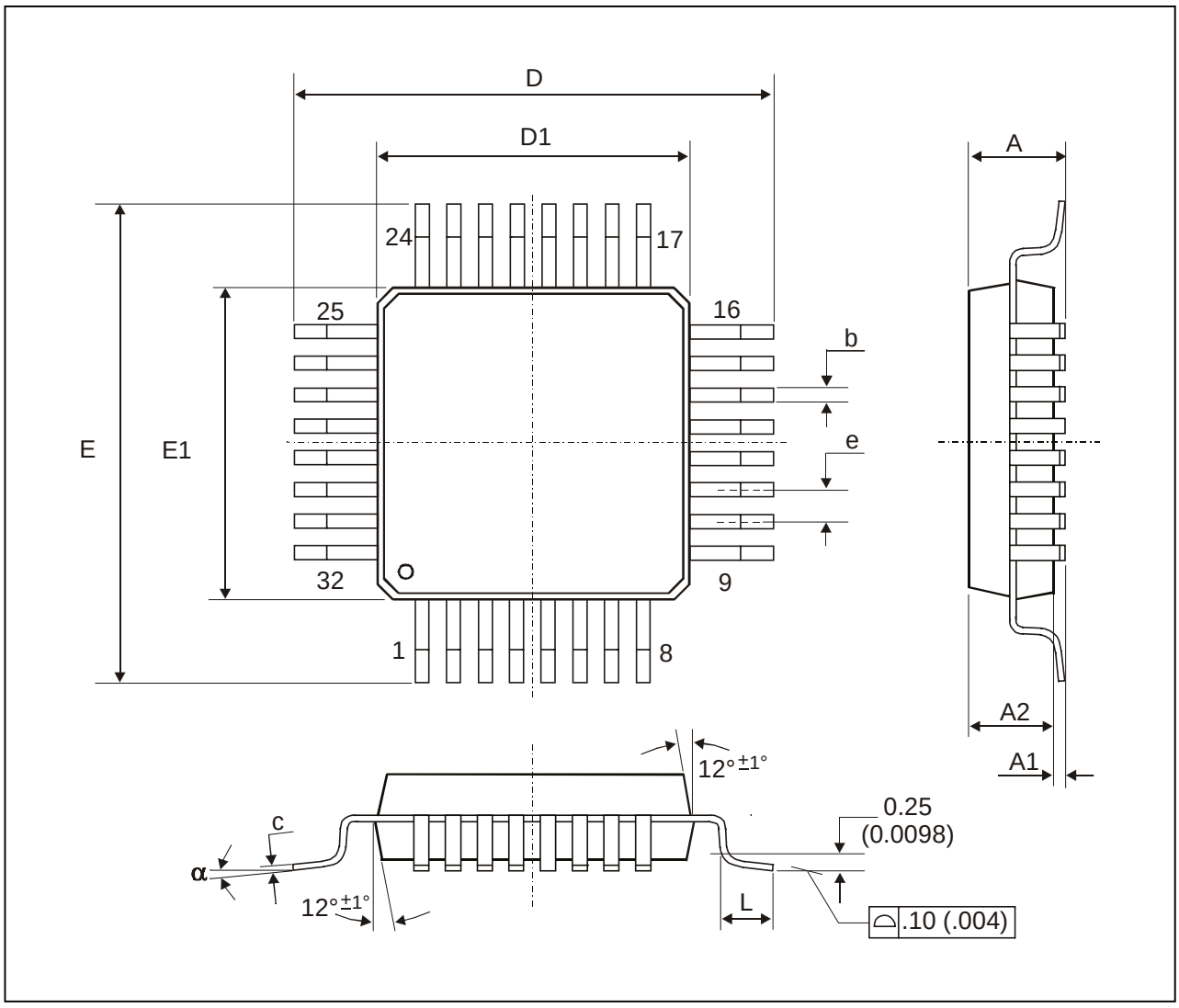

Fig. 4: LQFP32 (Low profile Quad Flat Package)

All Dimension in mm, coplanarity < 0.1mm										
	E1, D1	**E, D**	**A**	**A1**	**A2**	**e**	**b**	**c**	**L**	**α**
min	7.00	9.00	1.40	0.05	1.35	0.8	0.30	0.09	0.45	0°
max			1.60	0.15	1.45		0.45	0.20	0.75	7°
All Dimension in inch, coplanarity < 0.004”										
min	0.276	0.354	0.055	0.002	0.053	0.031	0.012	0.0035	0.018	0°
max			0.063	0.006	0.057		0.018	0.0079	0.030	7°

5 Reliability Information

Melexis devices are classified and qualified regarding suitability for infrared, vapor phase and wave soldering with usual (63/37 SnPb-) solder (melting point at 183degC).
The following test methods are applied:

- IPC/JEDEC J-STD-020A (issue April 1999)
  Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices
- CECC00802 (issue 1994)
  Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- MIL 883 Method 2003 / JEDEC-STD-22 Test Method B102
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

For more information on manufacturability/solderability see quality page at our website:
http://www.melexis.com/

6 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

7 Disclaimer

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