# N681386/87

## Single Programmable Extended Codec/SLCC

nuvoTon

## 1. DESCRIPTION

The N681386/87, implements a single channel FXS telephone line interface optimized for short loop applications. It integrates SLCC (Subscriber Line Control Circuit) functionality with a programmable CODEC and a DC/DC controller. The SLCC supports internal ringing up to 90 $V_{PK}$ (5 REN at 4k ft) ideal for Customer Premise Equipment (CPE). The CODEC can be configured for µ-law, A-law or 16-bit linear PCM encoding. It also supports a comprehensive set of signaling capabilities required to supervise and control the telephone lines. These include tone generation, ring tones, DTMF detection/ generation as well as FSK generation. An on-chip Pulse Width Modulation (PWM) driver allows control of an inductor based DC/DC converter. Programmable impedance and trans-hybrid balancing allow for worldwide deployment.

## 2. FEATURES

- Complete BORSCHT functions
- Internal balanced and unbalanced ringing up to 90 $V_{PK}$ (5 REN up to 4k ft)
- Integrated Power Management Options
    - Integrated DC/DC controller regulates battery voltage to minimize power dissipation in all operating modes
    - Programmable external battery switching
- Programmable linefeed characteristics
    - Ringing Frequency, Amplitude, and Cadence
    - Trapezoidal and Sinusoidal waveforms
    - Two wire AC impedance, and trans-hybrid balance
    - Constant Current feed (20 to 41) mA
    - Ring Trip and Loop Closure Thresholds
    - Ground Key Detection
- Programmable signal generation and detection
    - DTMF generation/ detection and Tone generation
    - Frequency Shift Keying (FSK) Enhanced Caller ID generation (Type I and Type II)
- Loop test and diagnostics support
    - Integrated loopback modes
    - Real-time linefeed monitoring
    - On-chip temperature sensor
    - Line Card Diagnostics Support
- Digital interfaces
    - PCM: G.711 µ-Law, A-Law and 16-bit linear
    - GCI and SPI bus
    - Programmable audio path gains
- Both PCM Master and Slave modes supported
- On-chip PLL for flexible clocking options including 1.0 MHz and 2.0 MHz BCLK operation
- Operating voltage: 3.3V
- Narrowband Codec (N681386)
- Wideband and Narrowband codec (N681387)
- Optional integrated (N681622) or discrete Subscriber Line Feed Circuit

## APPLICATIONS

- Residential VoIP Gateways / Routers/ IP-PBX
- Fiber to the Premise/Home (FTTP/H)
- Wireless Local Loop
- Optical Network Terminals (ONT)
- Analog Telephone Adapter (ATA)
- Voice enabled DSL/Cable Modems
- Integrated Access Devices
- Set Top Boxes

### Ordering Information

| Part Number | Temp Range (°C) | Package | Package Material |
|---|---|---|---|
| N681386DG<br>N681387DG | -40 to 85 | 48-LQFP | Pb-Free |
| N681386YG<br>N681387YG | -40 to 85 | 48-QFN | Pb-Free |
| N681622YG | -40 to 85 | 20-QFN | Pb-Free |

## ! WARNING !

**HIGH VOLTAGE WARNING**
**USE EXTREME CAUTION**

High voltage sources could cause serious injury or death if not used in accordance with design and/or user specifications, if they are used by untrained or unqualified personnel. Before testing Nuvoton's products read and understand all instructions, and safety procedures as in industry standard safe practices.

## 3. PIN CONFIGURATION

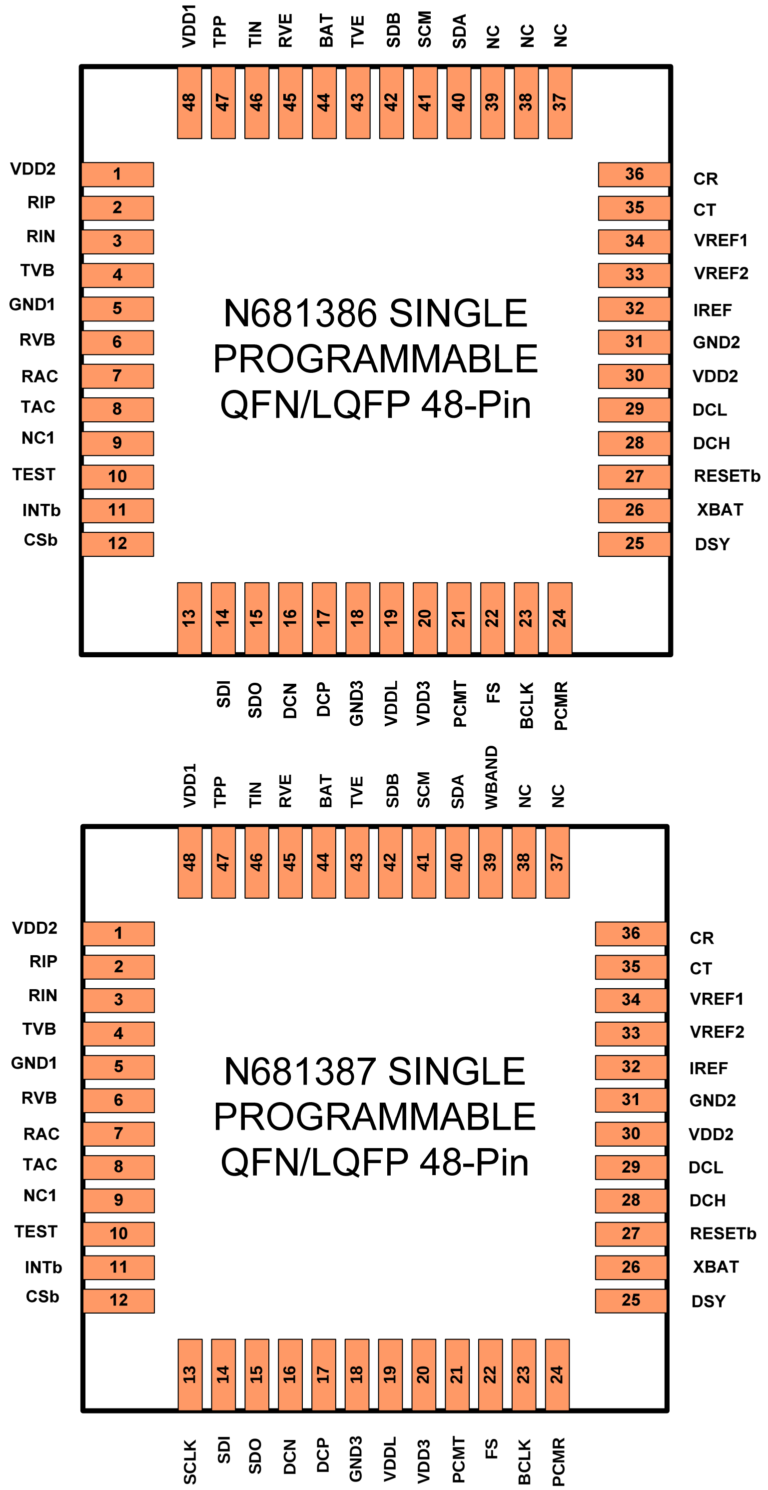

Figure 1: N681386/87 Pin Configuration

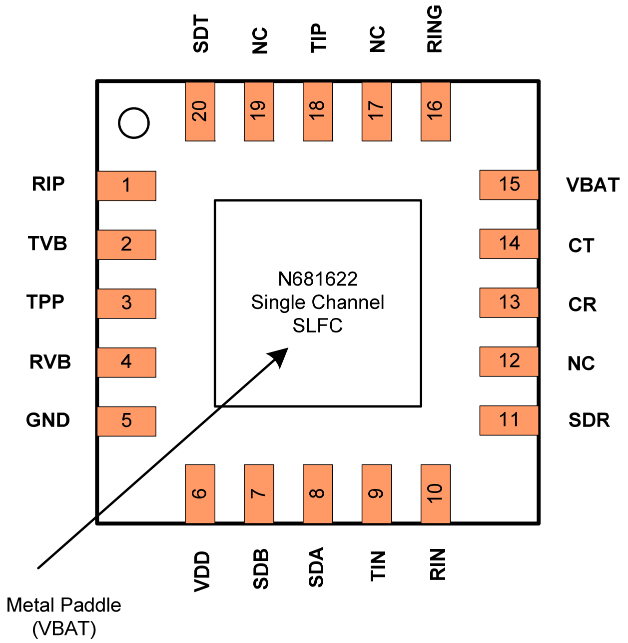

Figure 2: N681622 Subscriber Line Feed Circuit (SLFC) Pin Configuration

## 4. PIN DESCRIPTION

### 4.1. N681386/87 Pin Description

| Pin Name | Pin No. | Functionality | A/D | Pin Type |
|---|---|---|---|---|
| VDD1 | 1 | Line-driver 3.3 V supply | A | P |
| RIP | 2 | Positive RING Driver current source & Voltage sense | A | I/O |
| RIN | 3 | Negative RING Driver current source | A | O |
| TVB | 4 | Positive TIP Driver Base Voltage Control | A | O |
| GND | 5 | Line-driver ground supply | A | G |
| RVB | 6 | Positive RING Driver Base Voltage Control | A | O |
| RAC | 7 | RING Voice Band Input | A | I |
| TAC | 8 | TIP Voice Band Input | A | I |
| NC | 9 | No connect | | |
| TEST | 10 | For internal testing only. Needs to be tied to ground during normal operation | D | I |
| INTb | 11 | Interrupt. Maskable interrupt. Open drain output for wired-or operation | D | O |
| CSb | 12 | Chip Select. When inactive, SCLK and SDI are ignored and SDO is high impedance. When active, serial port is operational | D | I |
| SCLK | 13 | Serial port bit clock. Controls serial data on SDO and latches data on SDI | D | I |
| SDI | 14 | Serial port data in. Serial port control data | D | I |
| SDO | 15 | Serial port data out. Serial port control data | D | O |
| DCN | 16 | DC/DC converter Control for external NPN BJT | D | O |
| DCP | 17 | DC/DC Converter Control for external PNP BJT | D | O |
| GND3 | 18 | Logic I/O ground supply | D | G |
| VDDL | 19 | Logic supply voltage. This pin should not be connected up to an external supply. Use only as shown in application diagram. | D | I/O |
| VDD3 | 20 | 3.3 V Logic I/O supply | D | P |
| PCMT | 21 | Serial PCM Transmit data | D | O |
| FS | 22 | 8 or 16 kHz Frame Sync | D | I/O |
| BCLK | 23 | PCM Bit Clock. Also used as internal PLL reference clock | D | I |
| PCMR | 24 | Serial PCM Receive data | D | I |
| DSY | 25 | SPI Daisy Chain Enable | D | I |
| XBAT | 26 | External Battery Supply Enable. Disables DC/DC Controller when set high | D | I |
| RESETb | 27 | Reset. Active Low. Hardware reset used to place all control registers in default state. | D | I |

| Pin Name | Pin No. | Functionality | A/D | Pin Type |
|---|---|---|---|---|
| DCH | 28 | DC/DC Converter Current Sense Higher input Voltage | A | I |
| DCL | 29 | DC/DC Converter Current Sense Lower input Voltage | A | I |
| VDD2 | 30 | 3.3 V Analog AC path and reference Supply Voltage | A | P |
| GND2 | 31 | Analog AC path and reference Supply ground | A | P |
| IREF | 32 | Current Reference | A | I/O |
| VREF2 | 33 | Precision Reference Voltage | A | I/O |
| VREF1 | 34 | Mid Supply Reference Voltage | A | I/O |
| CT | 35 | External Capacitor TIP | A | I/O |
| CR | 36 | External Capacitor RING | A | I/O |
| NC | 37 | No Connect | | |
| NC | 38 | No Connect | | |
| WBAND | 39 | Wideband enable (only on N681387) | D | I |
| SDA | 40 | Subscriber Loop Differential sense signal A from linefeed circuit | A | I |
| SCM | 41 | Subscriber Common Mode sense signal from linefeed circuit | A | I |
| SDB | 42 | Subscriber Loop Differential sense signal B from linefeed circuit | A | I |
| TVE | 43 | TIP line-driver emitter voltage sense | A | I |
| BAT | 44 | Battery voltage monitoring | A | I |
| RVE | 45 | RING line-driver emitter voltage sense | A | I |
| TIN | 46 | Negative TIP Driver current source | A | O |
| TPP | 47 | Positive TIP Driver current source & Voltage sense | A | I/O |
| VDD1 | 48 | Line-driver 3.3 V supply | A | P |

Table 1: N681386/87 Pin Description

| | |
|---|---|
| **A** | Analog |
| **D** | Digital |
| **G** | Ground |

| | |
|---|---|
| **O** | Output |
| **I** | Input |
| **P** | Power |

### 4.2. N681622 Pin Description

| Pin Name | Pin No. | Functionality | Type | Pin Type |
|---|---|---|---|---|
| RIP | 1 | Ring Driver Pull up Current from 34.8 Ohm resistor | LV | I/O |
| TVB | 2 | Tip Pull-Up Driver control voltage | LV | I |
| TPP | 3 | Tip Driver Pull up Current from 34.8 Ohm resistor | LV | I/O |
| RVB | 4 | Ring Pull-Up Driver control voltage | LV | I |
| GND | 5 | Supply ground (0V) | LV | G |
| VDD | 6 | 3.3V Supply | LV | P |
| SDB | 7 | Subscriber differential signal B | LV | O |
| SDA | 8 | Subscriber differential signal A | LV | O |
| TIN | 9 | Tip DC Pull-Down current | LV | I |
| RIN | 10 | Ring DC Pull-Down current | LV | I |
| SDR | 11 | Subscriber differential Ring input | HV | I/O |
| NC | 12 | Not connected | | |
| CR | 13 | Ring Pull-Down filter capacitor | HV | I/O |
| CT | 14 | Tip Pull-Down filter capacitor | HV | I/O |
| VBAT | 15 | Battery Supply Voltage | HV | P |
| RING | 16 | Ring terminal | HV | O |
| NC | 17 | Not connected | | |
| TIP | 18 | Tip terminal | HV | O |
| NC | 19 | Not connected | | |
| SDT | 20 | Subscriber differential Tip input | HV | I/O |

Table 2: N681622 Pin Description

| | |
|---|---|
| **LV** | Low Voltage |
| **HV** | High Voltage |
| **G** | Ground |

| | |
|---|---|
| **O** | Output |
| **I** | Input |
| **P** | Power |

## 5. BLOCK DIAGRAM

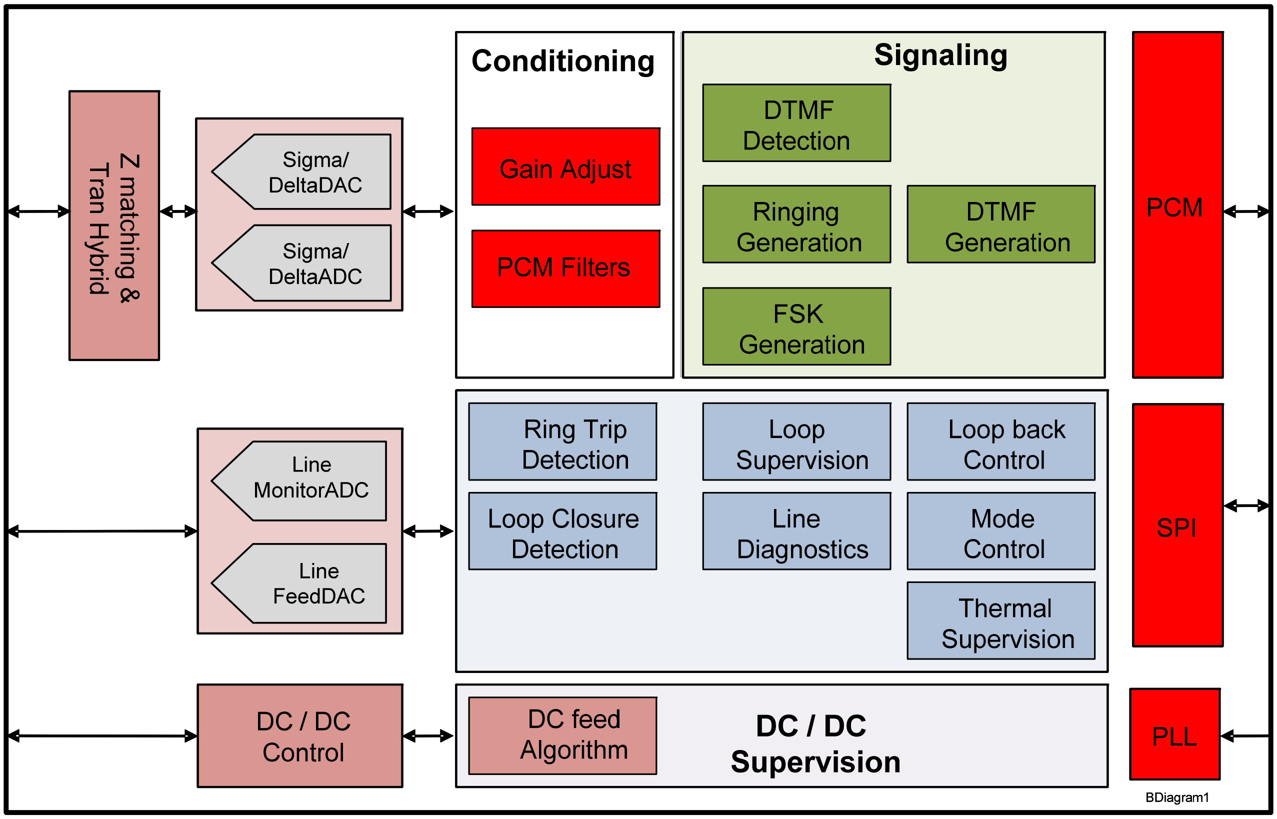

Figure 3: N681386/87 Block Diagram

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## 9. ABSOLUTE MAXIMUM RATINGS

### 9.1. Single Programmable Extended Codec/SLCC (N681386/87)

| Condition | Value |
|---|---|
| Junction temperature | 150$^0$C |
| Storage temperature range | -65$^0$C to +150$^0$C |
| LQFP-48 Thermal Resistance, typical | 76 $^o$C/W |
| QFN-48 Thermal Resistance, typical | 27.1 $^o$C/W |
| Voltage applied to any pin | ($V_{SS}$ - 0.3V) to ($V_{DD}$ + 0.3V) |
| Input current applied to any digital input pin | +/- 10 mA |
| ESD (Human Body Model) | 2000 V |
| $V_{DD}$ - $V_{SS}$ | -0.5V to +3.63V |
| Power Dissipation | 0.7W |

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

### 9.2. Subscriber Line Feed Circuit (N681622)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| VDD Supply Voltage | VDD | -0.5 - 5 | V |
| VBAT Supply Voltage | VBAT | -104 | V |
| Input Voltage HV IO | VINHV | (VBAT-0.3) to (VDD+0.3) | V |
| Input Voltage LV IO | VINLV | -0.3 to (VDD+0.3) | V |
| ESD, HBM | | JESD22 Class 1C | V |
| Operating Temperature ** | TA | -40 - 100 | C |
| Storage Temperature | TS | -40 - 150 | C |
| Thermal Resistance QFN20 | Rthja | 45 | C/W |
| Power Dissipation | Pmax | 0.9 | W |

** When the dice temperature reaches over 130°C, the device reliability may be adversely affected.

## 10. OPERATING CONDITIONS

### 10.1. Single Programmable Extended Codec/SLCC (N681386/87)

| Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Industrial operating temperature | TA | -40 | | +85 | C |
| Supply voltage ($V_{DD}$) | VDD | 3.13 | | 3.47 | V |
| Ground voltage ($V_{SS}$) | VSS | | 0 | | V |

***Note***: *Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.*

### 10.2. Subscriber Line Feed Circuit (N681622)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Industrial operating temperature | TA | -40 | | 85 | C |
| Supply voltage ($V_{DD}$) | VDD | 3.13 | 3.3 | 3.47 | V |
| VBAT Supply Voltage | VBAT | -100 | - | -9 | V |

# 11. ELECTRICAL CHARACTERISTICS

## 11.1. GENERAL PARAMETERS (N681386/87)

$V_{DD}$=3.13 V to 3.47 V; $V_{SS}$=0 V; $T_A$ = -40$^0$C to +85$^0$C;

| Symbol | Parameters | Conditions | Min (2) | Typ (1) | Max (2) | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Logic Input LOW Voltage | | -0.3 | -- | 0.8 | V |
| $V_{IH}$ | Logic Input HIGH Voltage | | 2 | -- | 3.6 | V |
| $V_T$ | Threshold point | | | 1.41 | | V |
| $V_{OL}$ | Logic Output LOW Voltage | INTB,FS,PCMT,SDO: $I_{OL}$ = 4 mA<br>DCP, DCN: $I_{OL}$ = 16 mA | -- | -- | 0.4 | V |
| $V_{OH}$ | Logic Output HIGH Voltage | FS,PCMT,SDO: $I_{OH}$ = 4mA<br>DCP, DCN: $I_{OH}$ = 16 mA | 2.4 | -- | | V |
| $I_{IL}$ | Input HIGH & LOW Leakage Current | $V_{SS}$<$V_{IN}$<$V_{DD}$<br>No pull-up or pull-down | -- | -- | +/-10 | uA |
| $I_{OZ}$ | Tri-state Leakage Current | $V_{SS}$<$V_O$<$V_{DD}$<br>High Z State | -- | -- | +/-10 | uA |
| $C_{IN}$ | Digital Input Capacitance | | -- | 3 | -- | pF |
| $C_{OUT}$ | Digital Output Capacitance | $V_O$ High Z | -- | 3 | -- | pF |

*1. Typical values: TA = 25°C , VDD = 3.3 V*
*2. All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.*

## 11.2. SUPPLY PARAMETERS DISCRETE SOLUTION (N681386/87 AND DISCRETE LINE DRIVER)

$V_{DD}$=3.13 V to 3.47 V; $V_{SS}$=0 V; $T_A$=-40$^0$C to +85$^0$C;

| Symbol | Parameters | Conditions | Min | Typ (1) | Max (2) | Units |
|---|---|---|---|---|---|---|
| $I_{PD}$ | Total Power Down Supply Current | RESETb = 0V, Vdd1..Vdd3<br>FS=BCLK=0V | | 12 | 100 | uA |
| $I_{SB}$ | Total Standby Supply Current | RESETb = VDD, VDD1 .. VDD3<br>FS=BCLK=0V, Line state Open | | 8.0 | 11.3 | mA |
| $I_{VDD}$ | Total Supply Current for all supplies @3.3V (linefeed states) | Open (ADC and DAC disabled) | | 21 | | mA |
| | | Forward/Reverse Active $I_{LIM}$=20 mA | | 66 | | mA |
| | | Forward/Reverse ON-HOOK Transmission | | 45 | | mA |
| | | Forward/Reverse Idle (ADC and DAC disabled) | | 29 | | mA |
| | | TIP/RING Open | | 28 | | mA |
| | | Ringing, Sine wave, REN=1, $V_{PK}$=56 V | | 50 | | mA |
| $I_{VBAT}$ | Total Battery Supply | Open, VBAT = 72V | | 0.72 | | mA |

| Symbol | Parameters | Conditions | Min | Typ (1) | Max (2) | Units |
|---|---|---|---|---|---|---|
| | Current | Forward/Reverse Active $I_{LIM}$=20 mA, | | 30 | | mA |
| | | Forward/Reverse ON-HOOK Transmission, XBTA:XTBOT=0, VBAT = 54V | | 12 | | mA |
| | | Forward/Reverse Idle, VBAT = 54V | | 1.3 | | mA |
| | | TIP/RING Open, VBAT = 54V | | 1.0 | | mA |
| | | Ringing, Sine wave, REN=1, VBAT = 71V | | 6.0 | | mA |

1. *Typical values: TA = 25°C , VDD = 3.3 V*
2. *All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *The supply current for the DC/DC converter can be calculated by : IDC/DC=IVBAT*VBAT/(efficiency*VDC/DC)*

### 11.3. SUPPLY PARAMETERS SLFC SOLUTION (N681386/87 AND N681622)

| Parameter | Symbol | Condition | MIN | TYP | Max | Unit |
|---|---|---|---|---|---|---|
| VDD Supply Current | IDDO | Open State | | 24.0 | | mA |
| | IDDI | Low Power Idle State, VBAT=-50V | | 21.4 | | mA |
| | IDDA | Active State | | 63.3 | | mA |
| | IDDR | Ringing, 1REN, 40Vrms | | TBD | | mA |
| | IDDOT | On-Hook Transmit | | 47.9 | | mA |
| | IDDTO | Tip/Ring Open | | TBD | | mA |
| VBAT Supply Current | IBTO | Open State | | 0.4 | | mA |
| | IBTI | Low Power Idle State, VBAT=-50V | - | 0.2 | 1.2 | mA |
| | IBTA | Active State | | 29.0 | | mA |
| | IBTR | Ringing, 1REN, 40Vrms | | TBD | | mA |
| | IBTOT | On-Hook Transmit | | 14.1 | | mA |
| | IBTTO | Tip/Ring Open | | TBD | | mA |

### 11.4. MONITORING A/D PARAMETERS

$V_{DD}$=3.13 V to 3.47 V; $V_{SS}$=0 V; $T_A$=-40$^0$C to +85$^0$C

| Symbol | Parameters | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| INL | Integral Nonlinearity (8-bit resolution) | | +/-0.5 | | LSB |
| DNL | Differential Nonlinearity (8-bit resolution) | | +/-0.5 | | LSB |
| | Gain Error (Current) | | | 20 | % |
| | Gain Error (Voltage) | | | 10 | % |
| | Sample Rate per channel | -- | -- | 800 | Hz |
| | Number of channels | -- | 16 | -- | |

Typically at 12-bit the INL and DNL is 2 LSB.

### 11.5. ANALOG SIGNAL LEVEL AND GAIN PARAMETERS

$V_{DD}$=3.13 V to 3.47 V; $V_{SS}$=0 V; $T_A$=-40$^0$C to +85$^0$C; Loading 600 Ω

| PARAMETER | SYM. | CONDITION | TYP. | TRANSMIT (A/D) | | RECEIVE (D/A) | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| Absolute Level | $L_{ABS}$ | 0 dBm0 = 0 dBm @ 600Ω | 1.0954 | --- | --- | --- | --- | $V_{PK}$ |
| Max. Transmit Level | $T_{XMAX}$ | 3.17 dBm0 for u-Law<br>3.14 dBm0 for A-Law(1) | 1.5779<br>1.5725 | ---<br>--- | ---<br>--- | ---<br>--- | ---<br>--- | $V_{PK}$<br>$V_{PK}$ |
| Absolute Gain (0 dBm0 @ 1020 Hz; $T_A$=+25°C) | $G_{ABS}$ | 0 dBm0 @ 1020 Hz, $V_{DD}$ =3.3V; $T_A$=+25°C;<br>assuming ideal line impedance matching | 0 | -0.40 | +0.40 | -0.40 | +0.40 | dB |
| Absolute Gain variation with Temperature | $G_{ABST}$ | $T_A$=0°C to $T_A$=+70°C<br>$T_A$=-40°C to $T_A$=+85°C | 0 | -0.10<br>-0.20 | +0.10<br>+0.20 | -0.10<br>-0.20 | +0.10<br>+0.20 | dB |
| Absolute Gain variation with Supply Voltage | $G_{ABSS}$ | $V_{DD}$=3.13 V – 3.47 V; 0dBm0 @ 1020 Hz; $T_A$=+25°C | 0 | -0.10 | +0.10 | -0.10 | +0.10 | dB |
| Frequency Response | $G_{RTV}$ | | See Figure | | | | | |
| Gain Variation vs. Level Tone (1020 Hz relative to –10 dBm0) | $G_{LT}$ | +3 to –40 dBm0<br>-40 to –50 dBm0<br>-50 to –60 dBm0 | ---<br>---<br>--- | -0.3<br>-0.6<br>-1.6 | +0.3<br>+0.6<br>+1.6 | -0.3<br>-0.6<br>-1.6 | +0.3<br>+0.6<br>+1.6 | dB |
| Gain Step Variation | $G_{ST}$ | -6 dB to 6 dB | 0 | - | +/-0.025 | - | +/-0.025 | dB |
| Absolute Group Delay | $T_{ABS}$ | 1200 Hz | --- | 633 | 650 | 286 | 300 | usec |
| Group Delay Distortion (relative to group delay @ 1200 Hz) | $T_D$ | | See Figure | | | | | |

1. Default Gain Setting

### 11.6. 2-WIRE TO 4-WIRE CONVERSION PARAMETERS

$V_{DD}$=3.13 V to 3.47 V; $V_{SS}$=0 V; $T_A$=-40$^0$C to +85$^0$C; Loading 600 Ω

| PARAMETER | SYM. | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Return Loss | $R_L$ | 200 Hz to 3.4 kHz, 600 Ohm | 26 | 40 | | dB |
| Trans hybrid Balance | $H_B$ | 200 Hz to 3.4 kHz, 600 Ohm | 26 | 40 | | dB |

### 11.7. 2-WIRE PARAMETERS

$V_{DD}$=3.13 V to 3.47 V; $V_{SS}$=0 V; $T_A$=-40$^0$C to +85$^0$C; Loading 600 Ω

| PARAMETER | SYM. | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Longitudinal Conversion Loss | $L_{CL}$ | 300 Hz to 600 Hz | 40 | | --- | dB |
| | | 600 Hz to 3.4 kHz, | 46 | | | |
| Longitudinal to Metallic or PCM Balance | $L_{ML}$ | 300 Hz to 600 Hz | 40 | 52 | --- | dB |
| | $L_{MH}$ | 600 Hz to 3.4 kHz, | 46 | 55 | --- | dB |
| Longitudinal Impedance | $L_Z$ | 300 Hz to 3.4 kHz | --- | 18.5 | | Ohms |
| Longitudinal Current | $L_I$ | Active OFF-HOOK; 300 Hz to 3.4 kHz | --- | 6.7 | | mA |

### 11.8. LINEFEED CHARACTERISTICS

$V_{DD}$=3.13 V to 3.47 V; $V_{SS}$=0 V; $T_A$=-40$^0$C to +85$^0$C; Loading 600 Ω

| Parameter | Sym. | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| RING amplitude | $V_{TR}$ | 5 REN load; sine wave;<br>$R_{LOOP}$ =160 Ohm;<br>$V_{BAT}$ = –75 V | 44 | 45 | --- | $V_{RMS}$ |
| Loop closure / Ground start threshold accuracy | $I_{lt}$ | $I_{lt}$ = 11.43 mA | --- | --- | +/-20 | % |
| RING trip threshold accuracy | $I_{rt}$ | $I_{rt}$ = 40.64 mA | --- | --- | +/-20 | % |
| Trapezoidal RING crest factor accuracy | | Crest factor = 1.3 | --- | --- | +/-0.05 | |
| Sinusoidal RING crest factor | $R_{cf}$ | | 1.35 | --- | 1.45 | |
| Ringing frequency accuracy | | F = 20 Hz | --- | --- | +/-1 | % |
| Ringing cadence accuracy | | Accuracy of on/off time | --- | --- | +/-50 | ms |
| DC Loop Current Accuracy | | ILIM = 20 mA, $R_{LOAD}$ = 500 ohm | | --- | +/-20 | % |
| DC Open Circuit Voltage Accuracy | | Active Mode; $V_{OH}$ = 48 V, $V_{TIP} – V_{RING}$ | | --- | +/-4 | V |
| Power alarm threshold accuracy | | Power Threshold = 300 mW | --- | --- | +/-25 | % |

### 11.9. ANALOG DISTORTION AND NOISE PARAMETERS

$V_{DD}$=3.13 V – 3.47 V; $V_{SS}$=0 V; $T_A$=-40$^0$C to +85$^0$C; Loading 600 Ω

| PARAMETER | SYM. | CONDITION | TRANSMIT (A/D) | | | RECEIVE (D/A) | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Total Distortion vs. Level Tone u-Law | $D_{LTu}$ | 1020 Hz, C-Message Weighted | | See Figure | | | See Figure | | |
| Total Distortion vs. Level Tone, A-Law | $D_{LTA}$ | 1020 Hz, Psophometric Weighting | | | | | | | |
| Audio Tone Generator Signal-to-Distortion Ratio | $D_{LTT}$ | 0 dBm0, Active OFF-HOOK and OHT, ideal impedance matching | 45 | --- | --- | 45 | --- | --- | dB |
| Spurious Out-Of-Band (300 Hz to 3400 Hz @ 0dBm0) | $D_{SPO}$ | 4600 Hz to 7600 Hz<br>7600 Hz to 8400 Hz<br>8400 Hz to 100000 Hz | NA | NA | NA | --- | -70<br>-70<br>-65 | -30<br>-40<br>-30 | dB |
| Spurious In-Band (700 Hz to 1100 Hz @ 0dBm0) | $D_{SPI}$ | 300 to 3200 Hz | --- | --- | -47 | --- | --- | -47 | dB |
| Intermodulation Distortion (300 Hz to 3400 Hz –4 to –21 dBm0) | $D_{IM}$ | Two tones | --- | --- | -45 | --- | --- | -45 | dB |
| Idle Channel Noise | $N_{IDL}$ | u-Law; C-message<br>A-Law; Psophometric<br>16-bit Linear | ---<br>---<br>--- | 13<br>-74 | 18<br>-69 | ---<br>---<br>--- | 1<br>-90 | 14<br>-76 | dBrnc0<br>dBm0p |
| Power Supply Rejection | $PSRR_A$ | $V_{DDA}$; DC to 3.4 kHz | 40 | --- | --- | 40 | --- | --- | dB |
| Power Supply Rejection | $PSRR_B$ | $V_{BAT}$; DC to 3.4 kHz | 40 | --- | --- | 40 | --- | --- | dB |

## 12. FUNCTIONAL DESCRIPTION

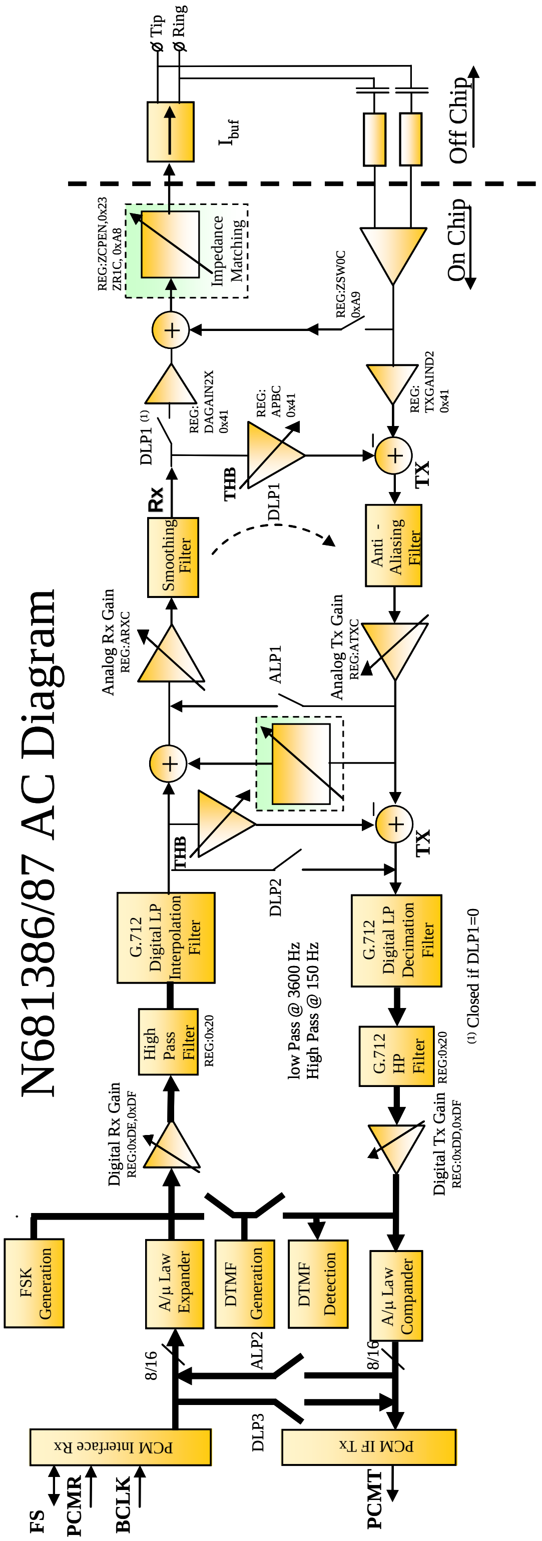


Figure 4: AC signal Path

### 12.1. BORSCHT FUNCTIONALITY

The N681386/87 connects to the TIP and RING (POTS - Plain Old Telephone Service) interface and performs the so-called BORSCHT and AC transmission functions. Following are the BORSCHT functions:

- **B**attery Feed
- **O**ver-Voltage Protection
- **R**inging (Balanced / Unbalanced)
- **S**upervision (Signaling)
- **C**oding
- **H**ybrid (2 / 4-wire conversion)
- **T**esting

#### 12.1.1. BATTERY FEED

The N681386/87, has two DC feed regions; a constant voltage region and a constant current region. As illustrated in Figure 4 the current limit **$I_{LIM}$** determines the constant current region. The ON-HOOK voltage, **$V_{OH}$**, determines the constant voltage region. The device has an inherent output resistance of typically 50Ω in non-ringing states. The Ground Margin Voltage, **$V_{GM}$**, determines the offset of the most positive terminal (TIP in Forward polarity state and RING in Reverse polarity state) with respect to ground **$I_{LIM}$**, **$V_{OH}$**, and **$V_{GM}$** are programmable as shown in Table 2.

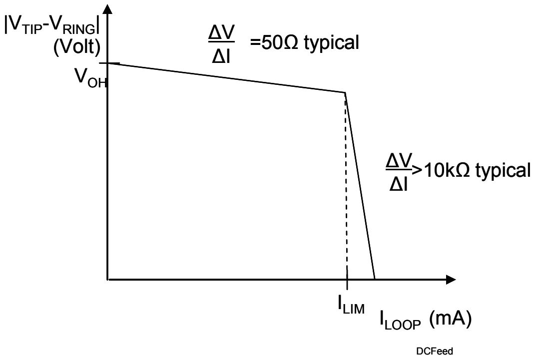


Figure 5: DC Feed Regions

| Register | Address | Parameter | Programmable Range | Step Size | Default Value | Unit |
|---|---|---|---|---|---|---|
| LCL | 0x45 | $I_{LIM}$ | 20 – 41 | 3 | 20 | mA |
| OHV | 0x4C | $V_{OH}$ | 0 to –93.5 | 1.484 | -47.488 | V |
| GMV | 0x4D | $V_{GM}$ | 0 to –93.5 | 1.484 | -2.968 | V |

Table 3: Programmable Ranges for DC Line Feed

The control circuit for TIP or RING is illustrated in Figure 5 and utilizes a three transistor discrete Linefeed circuit. Transistors Q1 and Q2 drive the voltages on the subscriber loop while transistor Q3 provides additional isolation. The Line Driver DC feedback loop is completed via DC isolation resistors $\mathbf{R_{VBAT}}$ and $\mathbf{R_{VE}}$ to the chip. TIP and RING signals are derived from the common mode and differential mode signal block. This information is, in turn, used to exercise control over the external transistors. Voice band signals are passed over a decoupling capacitor in the AC feedback loop.

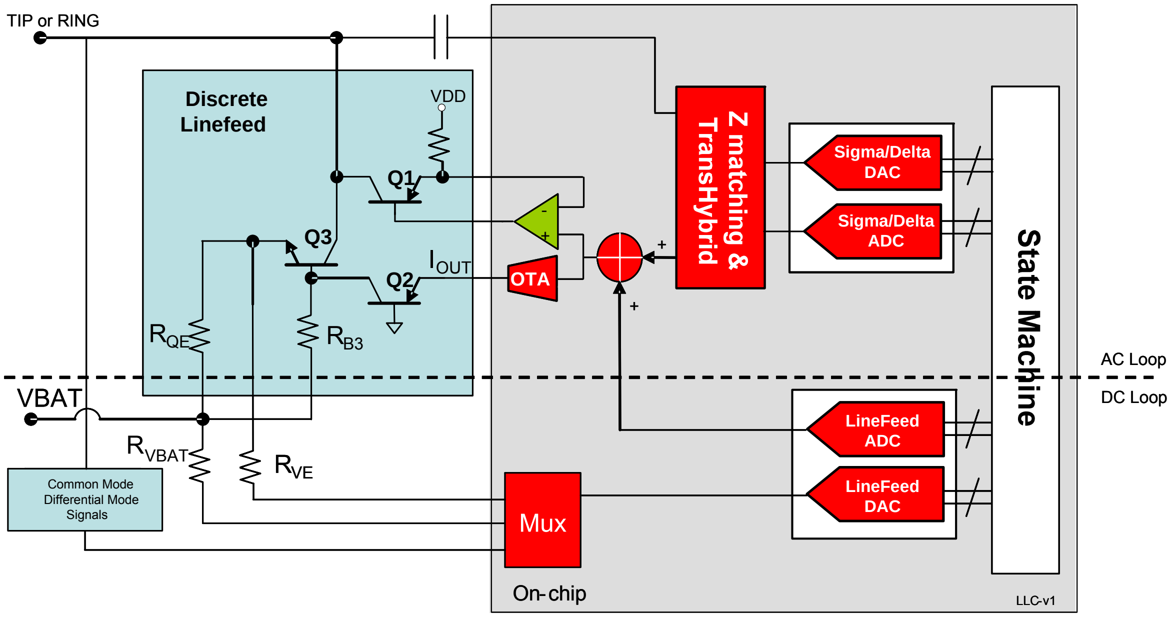


Figure 6: Line Loop Control

Control and monitoring of these transistors is done both individually and in groups. For example, TIP and RING Linefeed circuits each have a Q1 transistor. Both share the same register to set their Power Alarm Threshold values. But each TIP and RING transistor has a separate Power Alarm Interrupt bit in the interrupt register.

The control circuit for TIP and RING whenN681622 is utilized follows the same general principles.

#### 12.1.1.1. LINEFEED STATES OF OPERATION

The N681386/87 can operate in eleven states, as shown below.

| State | LS Settings<br>MSB | | | LSB | Description |
|---|---|---|---|---|---|
| Open | 0 | 0 | 0 | 0 | TIP and RING tri-state |
| Forward Active | 0 | 0 | 0 | 1 | $V_{TIP} > V_{RING}$ |
| Forward ON-HOOK Transmission | 0 | 0 | 1 | 0 | $V_{TIP} > V_{RING}$; audio signal paths powered on |
| TIP Open | 0 | 0 | 1 | 1 | TIP tri-stated, RING active; used for ground start |
| Ringing | 0 | 1 | 0 | 0 | Ringing waveform applied to TIP and RING |
| Reverse Active | 0 | 1 | 0 | 1 | $V_{RING} > V_{TIP}$ |
| Reverse ON-HOOK Transmission | 0 | 1 | 1 | 0 | $V_{RING} > V_{TIP}$; audio signal paths powered on |
| RING Open | 0 | 1 | 1 | 1 | RING tri-stated, TIP active |
| Forward Idle | 1 | 0 | 0 | 1 | $V_{TIP} > V_{RING}$ |
| Reverse Idle | 1 | 1 | 0 | 1 | $V_{RING} > V_{TIP}$ |
| Calibration | 1 | 1 | 1 | 0 | $V_{TIP} = V_{RING}$~Vbat+2 |

Table 4: Linefeed States

##### 12.1.1.1.1. OPEN STATE

Current to the external linefeed circuitry is shut off, effectively making TIP and RING tri-stated and it can also be used for fault condition detection. DC output impedance is 150K ohm.

##### 12.1.1.1.2. ACTIVE, IDLE AND ON-HOOK TRANSMISSION STATES

- Active, Idle and ON-HOOK Transmission states all have both Forward and Reverse incarnations
- In Forward state TIP is the more positive lead
- In Reverse state RING is the more positive lead
- In Idle states the external linefeed circuitry is ON but the audio signal paths are not powered up.
- In both Active states the external linefeed circuitry is ON and the audio signal paths are powered up.
- In both ON-HOOK Transmission states audio signal paths are powered up to allow ON-HOOK transmission.

The Forward and Reverse incarnations of the Active, Idle and ON-HOOK Transmission states are determined solely by setting the LS register. Fpr automatic transitions Forward and Reverse incarnations are determined by the $V_{OH}$ polarity in OHV:SB[6] address location (0x4C).

##### 12.1.1.1.3. TIP OPEN STATE

- All control currents to the external circuitry associated with TIP are shut off.
- Linefeed is provided to RING.

#### 12.1.1.1.4. RING OPEN STATE

- All control currents to the external circuitry associated with RING are shut off and keeps TIP active.

#### 12.1.1.1.5. RINGING STATE

- Drives the ringing waveforms onto the loop

#### 12.1.1.1.6. CALIBRATION STATE

Calibration state is used to compensate or correct for external component imperfections. It should be performed following the system power up. This state is enabled by setting LS:LS[3:0] address (0x44) to **'1110'**. The line should be on-hook during calibration. RING or TIP must not be connected to ground during the calibration. All automatic linefeed transitions should be disabled when performing calibration. After calibration is completed, the Linefeed state should be reset to a normal operating state and the automatic Linefeed transitions can be enabled again. Calibration state is not applicable to SLFC. For a more detailed explanation, please refer to the Calibration Application note.

Please note that Calibration state is not applicable to Subscriber Line Feed Circuit (SLFC).

### 12.1.1.2. OPERATION MODES

The N681386/87 can operate under two battery supply operation modes. The modes are selected with a pin XBAT as illustrated below.

| Operation Mode | XBAT Pin | Per Channel DC/DC | VBAT Switch [DCN/DCP Line state dependent Control] |
|---|---|---|---|
| On-Chip DC/DC Controller | 0V | On | Off |
| External Battery Supplies | 3.3V | Off | On |

Table 5: Operation Modes

### 12.1.1.3. AUTOMATIC TRANSITIONS

In addition, some automatic state transitions may also be enabled:

#### 12.1.1.3.1. POWER ALARM AUTOMATIC REACT

- Setting LAMC:PAA[2] address (0x43) bit will make the channel automatically enter the Open state upon the occurrence of a power alarm.

#### 12.1.1.3.2. SETTING RING AUTOMATIC

- Setting LAMC:RGA[1] address (0x43) bit makes the channel automatically enter the Active state from the Ringing State upon RING Trip Detect

#### 12.1.1.3.3. SETTING LOOP CLOSURE DETECT AUTOMATIC REACT

Setting LAMC:LCDA[0] address (0x43) bit makes the channel automatically enter the Active state from the ON-HOOK Transmission, Idle, TIP Open, and RING Open states upon Loop Closure Detect. Furthermore, the channel will transition from Active to Idle state if the Loop Closure Detect circuitry indicates a loop closure is no longer present, and back to Active state upon a reoccurrence of Loop Closure Detect.

When the above automatic transitions do occur, LS:LS[3:0] address (0x44) will be updated automatically to reflect the newly entered state. In all cases the shadow linefeed status bits, LS:SLS[3:0] address (0x44) reflect the actual linefeed status. This includes switching between 'Ringing' during the ring burst and 'ON-HOOK Transmission' during the cadence. This RING/cadence transition is not considered an automatic transition and LS:LS[3:0] address (0x44) will continue to reflect Ringing state. The following example state diagram illustrates LS:SLS[3:0] address (0x44) states including automatic transitions, RING/Cadence transition and several possible transitions solely governed by software.

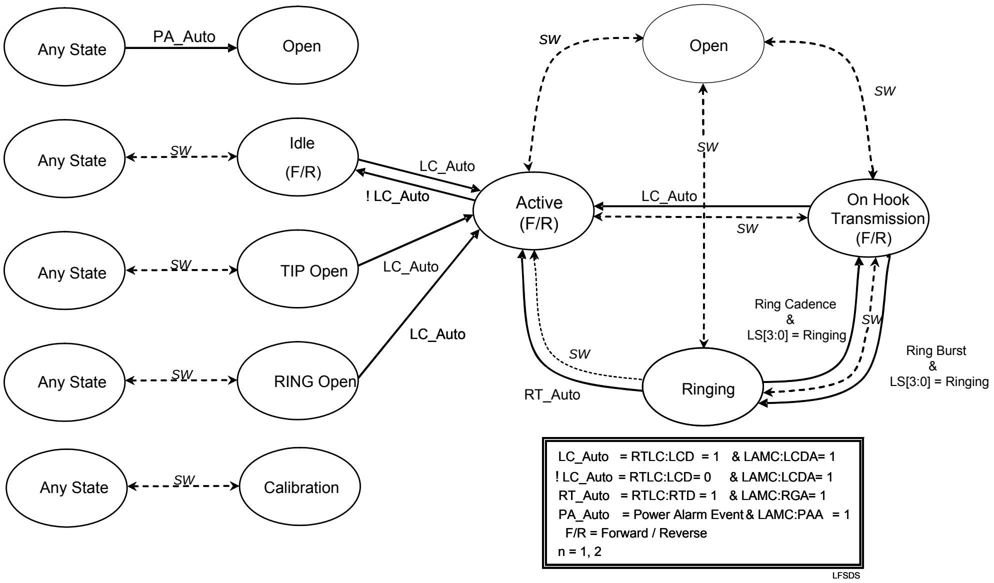


Figure 7: Example State Diagram

| Register | Bit(s) | Address | Parameter | Description / Range |
|---|---|---|---|---|
| LS | LS[3:0] | 0x44 | Programmed Linefeed Status | Eleven states |
| | SLS[7:4] | 0x44 | Shadow Linefeed Status | Reflects actual state |
| LAMC | PAA[2] | 0x43 | Power Alarm Automatic React | Enable/Disable |
| | RGA[1] | 0x43 | RING Automatic | Enable/Disable |
| | LCDA[0] | 0x43 | Loop Closure Detect Automatic React | Enable/Disable |

Table 6: Associated Registers for Linefeed Control

The device continuously monitors voltages on the line driver, driving them to target voltages appropriate to the actual linefeed state as summarized below.

| Linefeed State | TIP Target | RING Target |
|---|---|---|
| Open | High Z | High Z |
| Forward Active | $V_{TIP} > V_{RING}$ | |
| Forward ON-HOOK Transmission | $V_{TIP} > V_{RING}$ | |
| TIP Open | High Z | Active |
| Ringing | RING Signal | RING Signal |
| Reverse Active | $V_{TIP} < V_{RING}$ | |
| Reverse ON-HOOK Transmission | $V_{TIP} < V_{RING}$ | |
| RING Open | Active | High Z |
| Forward Idle | $V_{TIP} > V_{RING}$ | |
| Reverse Idle | $V_{TIP} < V_{RING}$ | |

Table 7: TIP and RING Voltage Targets

The device monitors the currents in the external transistors and makes these values available in registers. These registers and the internal A/D are updated at a rate of 800 Hz or every 1.25 msec. Other useful voltages and currents are calculated internally and made available in registers.

| Register | Bits(s) | Address | Parameter | Description / Range |
|---|---|---|---|---|
| BATV | VB[7:0] | 0x80 | Battery Voltage | 0V to -94.6V in 0.371V steps |
| SCM | SCM[11:0] | 0x92 | Common Mode Voltage | +93.5V to -93.5V in 0.023 V steps |
| QT3V | QT3V[7:0] | 0x83 | Transistor QT3 Emitter Voltage | 0V to -94.6V in 0.371V steps |
| QR3V | QR3V[7:0] | 0x84 | Transistor QR3 Emitter Voltage | 0V to -94.6V in 0.371V steps |
| QT3I | QT3I[11:0] | 0x85 | Transistor QT3 Current | 0A to 78.54 mA in 19.2 μA steps |
| QR3I | QT3I[11:0] | 0x86 | Transistor QR3 Current | 0A to 78.54 mA in 19.2 μA steps |

Table 8: Registers Associated with Line Monitoring – Measured

| Register | Bit(s) | Address | Parameter | Description / Range |
|---|---|---|---|---|
| LPV | VLP[11:0] | 0x8D | Loop Voltage | +93.5V to -93.5V in 0.023 V steps |
| QT1I | QT1I[11:0] | 0x87 | Transistor QT1 Current | 0A to 78.54 mA in 19.2 μA steps |
| QT2I | QT2I[11:0] | 0x88 | Transistor QT2 Current | 0A to 9.95 mA in 2.5 μA steps |
| QR1I | QR1I[11:0] | 0x89 | Transistor QR1 Current | 0A to 78.54 mA in 19.2 μA steps |
| QR2I | QR2I[11:0] | 0x8A | Transistor QR2 Current | 0A to 9.95 mA in 2.5 μA steps |
| LGI | ILG[11:0] | 0x8C | Longitudinal Current | +77.62 mA to –77.62 mA in 19uA |
| TIPI | ITLP[11:0] | 0x8E | TIP Current | +77.62 mA to –77.62 mA in 19uA |
| RINGI | IRLP[11:0] | 0x8F | RING Current | +77.62 mA to –77.62 mA in 19uA |
| LPI | ILP[11:0] | 0x90 | Loop Current | +77.62 mA to –77.62 mA in 19uA |

Table 9: Registers Associated with Line Monitoring – Calculated

In addition the following loop voltages and currents are derived from the above measurements and reported separately.

#### 12.1.1.4. POLARITY REVERSAL

The Linefeed states which have Forward or Reverse incarnation (Active, Idle and ON-HOOK Transmission states) can have the polarity reversed two different ways. In addition, the line (TIP or RING) which is at VOH can be collapsed towards ground by using the wink function.

- Hard polarity reversal
- Soft polarity reversal

##### 12.1.1.4.1. HARD POLARITY REVERSAL

Hard polarity is achieved by abruptly reversing the voltage between TIP and RING without any ramp-rate control. This is achieved by simply changing the linefeed register from Forward to Reverse incarnation or vice versa. A Hard polarity reversal will be performed provided that soft polarity reversal is not enabled APG:PREN[6] address (0x40) bit to 0. The sign bit (OHV:SB[6]) is used to determine the polarity of the line when going from Idle to Active States. If the new polarity is to be retained in future Idle to Active transitions, it is recommended that this bit be also changed appropriately when polarity is reversed.

##### 12.1.1.4.2. SOFT POLARITY REVERSAL

Soft polarity is achieved by reversing the voltage between TIP and RING with ramp-rate control. Soft polarity reversal is enabled by setting APG:PREN[6] = “1” address (0x40). The ramp rate at which the reversal will occur is selected in APG:RAMP[8] address (0x40). The Ramp is triggered by toggling WINK bit APG:PREN[6] = “1” address (0x40). Soft polarity reversal can be used from Forward Active to Reverse Active or vice versa. The table below illustrates the sequence of events for a Forward to Reverse soft polarity reversal. For Reverse to Forward Polarity Reversal step 2 would involve TIP and step 4 would involve RING.

| Step(s) | Register Name | Bit(s) | Bit State | Step Description |
|---|---|---|---|---|
| 1 | APG | PRE[6] | 1 | Enables soft polarity reversal |
| 2 | APG | VOHZ[5] | 1 | Wink line (RING towards 0V) |
| 3 | Use Line state register to reverse the line from Forward to Reverse | | | |
| 4 | APG | VOHZ[5] | 0 | Un-wink line (TIP side towards VOH) |
| 5 | APG | PRE[6] | 0 | Disable soft polarity reversal |

Note that the negative going ramp rate can be limited by the settling speed of the DCDC converter. Setting the minimum on time (0x57) to 0x0B before the ramp and back to the initialization value after the ramp will prevent this

| Addr | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x40 | APG | RAMP | PREN | VOHZ | RES | ARX[1:0] | | ATX[1:0] | | 0x00 |

The sign bit (OHV:SB[6]) is used to determine the polarity of the line during an automatic transition into idle, Active, and On-Hook transition states. If the new polarity is to be retained in future automatic transitions, it is recommended that OHV:SB[6] be also changed appropriately when polarity is reversed.

The ramp rate for steps 2 and 4 above is determined by the Ramp Rate bit APG:RAMP[7].

#### 12.1.1.5. WINK FUNCTION POLARITY REVERSAL

A Wink function is used for the ‘message waiting’ lamp in telephone sets. For this function to take place no Linefeed state change is necessary. The Wink function is a variation of Soft Polarity Reversal but without any Linefeed state change. In this case Soft Polarity reversal is enabled as before (APG:PREN[6] address (0x40) bit to “1”, with APG:RAMP[7] address (0x40) selecting the ramp rate). Now the OHV:VOHZ[5] address (0x4C) bit can be used to directly ramp the RING line towards 0V or back to $V_{RING}$. For example, in Forward Idle mode $V_{TIP}$ is at $V_{GM}$ and $V_{RING}$ is $V_{GM}$+$V_{OH}$. If VOHZ bit is set to “1” the Ring Voltage will ramp towards 0V. If the bit is toggled it will eventually return to the nominal $V_{RING}$ setting. The user has full control of the Wink function cadence.

| Register | Bit(s) | Address | Parameter | Programmable Range |
|---|---|---|---|---|
| APG | VOHZ[5] | 0x40 | Wink Function (Smooth transition to $V_{OH}$=0V) | 0 = Return to previous $V_{OH}$<br>1 = Ramp to 0V |
| APG | PRE[6] | 0x40 | Soft Polarity Reversal Enable | 0 = Disabled<br>1 = Enabled |
| APG | RAMP[7] | 0x40 | Soft Polarity Reversal Ramp Rate | 0 = 1.5 V/125 µs<br>1 = 3.0 V/125 µs |
| LS | LS[3:0] | 0x44 | Linefeed Status | |
| OHV | SB[6] | 0x4C | Polarity Reversal Status (Sign) | 0 = Forward<br>1 = Reverse |

Table 10: Registers for Polarity Reversal

### 12.1.2. OVER-VOLTAGE PROTECTION

It is a common requirement for electronic circuits to have to withstand some degree of over-voltage and/or reverse voltage on the power-supply lines. Integrated circuits are designed to operate from a nominal 3.3V power supply. Some kind of protection circuit is therefore needed to prevent voltages greater than the maximum allowable from being applied to the IC pins. The N681386/87 device needs to be protected from surges and AC power shorts. This should be implemented using external components and a variety of commercial approaches are typically employed. However, N681386/87 device has on-chip voltage and line monitoring capabilities which allow the system to report line faults, crossovers, and other line conditions in order to facilitate remote service. It also has sense inputs can be configured such that blown fuse can be detected. The on-chip DC/DC controller is equipped with three protection shutdown mechanisms. It detects

a) DCDC output voltage (VBAT) 10% above full scale or
b) DCDC supply voltage (VDDC) too low or
c) DCDC supply current ($I_{VDDC}$) too high;

A counter is tracking the three cases of DC/DC power alarm. The counter will automatically reset upon being read, allowing the user to monitor the number of power alarms within a specific time period. This register is a read ONLY register resets upon a read command.

| Register | Bit(s) | Address | Parameter | Programmable Range |
|---|---|---|---|---|
| APG | PALT[7:0] | 0x9F | Power Alarm Counter | Increment on every rising edge of LOW VDC or HIGH IDC; clip at 255; |

Table 11: PWM DC/DC Power Alarm Counter

### 12.1.2.1. THERMAL OVERLOAD

In addition to voltage and current monitoring described in section 6.1.1.1 “Linefeed States of Operation”, N681386/87 continuously monitors the power dissipation of each external transistor in the Linefeed circuitry. After Low Pass Filtering, the power dissipation is compared against thresholds which are listed in Table 10. The threshold and the Low Pass Filter pole are both programmable and should be set according to the characteristics of the individual transistor as follows. The Low Pass Filter pole for QT1 and QR1 is given by the equation:

$$Q1C[12:0] = \left(1 - \frac{1}{800 \times T_{TC}}\right) \times 2^{13}$$

Where $T_{TC}$ is the thermal time constant of the external transistor. The threshold should be programmed according to the maximum power dissipation of the external transistor. If the threshold is exceeded a power alarm event is deemed to have occurred. An associated interrupt may be enabled. An automatic state transition into Open state may be enabled by setting Power Alarm Automatic React (LAMC:PAA[2]) address (0x43)).

| Register | Bit(s) | Address | Parameter | Description / Range |
|---|---|---|---|---|
| PALPQ1<br>PALPQH1<br>PALPQH2 | Q1C[7:0]<br>Q1C[11:8]<br>Q1C[12] | 0xA1<br>0xA3<br>0xA4 | PA Low Pass Filter Pole for QT1 and QR1 | See Register Description |
| PALPQ2<br>PALPQH1<br>PALPQH2 | Q2C[7:0]<br>Q2C[11:8]<br>Q2C[12] | 0xA0<br>0xA3<br>0xA4 | PA Low Pass Filter Pole for QT2 and QR2 | See Register Description |
| PALPQ3<br>PALPQH2<br>PALPQH2 | Q2C[7:0]<br>Q3C[11:8]<br>Q3C[12] | 0xA2<br>0xA3<br>0xA4 | PA Low Pass Filter Pole for QT3 and QR3 | See Register Description |
| PATHQ1 | Q1TH[7:0] | 0xA6 | PA Threshold for QT1 and QR1 | 0 to 7.7 W in 30.4 mW steps |
| PATHQ2 | Q2TH[7:0] | 0xA5 | PA Threshold for QT2 and QR2 | 0 to 0.97 W in 3.8 mW steps |
| PATHQ3 | Q3TH[7:0] | 0xA7 | PA Threshold for QT3 and QR3 | 0 to 7.7 W in 30.4 mW steps |
| INT1 |  | 0x26 | Power Alarm Interrupt | Enable/Disable |
| IE1 |  | 0x27 | Power Alarm Interrupt Enable | Enable/Disable |
| LAMC | PAA[2] | 0x43 | Power Alarm Automatic React | Enable/Disable |

Table 12: Registers Associated with Thermal Overload

#### 12.1.2.2. TEMPERATURE MONITOR

The device contains an on-chip temperature sensor that senses the temperature inside the package. The sensor is read through TEMP:TS[7:0] register (0x99) which is **READ ONLY** register. The temperature T in °C is given by the following equation.

$$T = TS[7:0] - 67$$

For example TEMP:TS[7:0] = 0x23, (35 decimal) indicates a temperature T=-32°C and TEMP:TS[7:0]=0xCD (205 decimal) indicates T=138°C. Similarly threshold temperatures $T_{TH}$ can be set in register THAT:THAT[7:0] address (0xAA). The $T_{TH}$ is calculated by the following equation.

$$T_{TH} = TATH[7:0] - 67$$

By enabling the temperature sensor interrupt in IE3:TMPE[0] address (0x2B), an interrupt will be generated if the temperature reaches this threshold. This facilitates control of the temperature should the device get close to the junction temperature. Note that there is no filtering associated with this temperature alarm since the package has an intrinsic thermal time constant. It is recommended that the temperature alarm threshold be set to 125°C. The actual, TINT, internal temperature can be estimated by the following equation.

$$T_{INT} = T_A + \left( R_J \times P \right)$$

$T_A$ – Ambient Temperature, $R_J$ – Thermal Resistance, P – Power Dissipation

For example, the maximum power dissipation for the QFN device is 0.7 W. The thermal resistance of the 48-pin QFN package is 27.1°C/W. So at $T_A$=85°C, the estimated internal temperature would be:

$$T_{INT} = 85 + 27.1 * 0.7 = 104^{o}C$$

### 12.1.3. RINGING

There is a built-in RING generator that can generate balanced sinusoidal or trapezoidal ringing without the need for external components. Both trapezoidal and sine wave ringing signals can be generated. The Frequency, Amplitude, DC offset and ringing cadence of the ringing signal are programmable. In the case of trapezoidal waveforms the crest factor is also programmable. The choice of sinusoidal or trapezoidal will depend on requirements of the end user; sinusoids are required in many parts of the world to minimize cross talk between the many tip/ring pairs in a typical wiring bundle from the central office, whereas a trapezoid will deliver more power to the phone due to its low crest factor. As Ringing utilizes the Tone Generation block, we will first examine this function.

#### 12.1.3.1. TONE GENERATION

There are two tone generators Oscillator1 (OS1), and Oscillator2 (OS2). These can be used to generate signals such as dial tone, busy tone, and various test tones which can be sent either on the transmit or receive paths. Each tone generator has a similar architecture and contains a two-pole oscillator circuit with a sample rate of 8 kHz.

| Register | Bit(s) | Address | Parameter | Description / Range |
|---|---|---|---|---|
| OS1ICL<br>OS1ICH | O1IC[15:0] | 0xC2<br>0xC3 | Oscillator 1 Amplitude Coefficient | Sets Amplitude |
| OS1CL<br>OS1CH | O1C[15:0] | 0xC6<br>0xC7 | Oscillator 1 Frequency Coefficient | Sets Frequency |
| OS1ATL<br>OS1ATH | O1ON[15:0] | 0xCA<br>0xCB | Oscillator 1 Active Timer | 0 to 8 sec |
| OS1ITL<br>OS1ITH | O1OFF[15:0] | 0xCE<br>0xCF | Oscillator 1 Inactive Timer | 0 to 8 sec |
| RMPC | TOR[3] | 0xC1 | Tone Route | Towards D/A or A/D |
| OSN | O1E[0]<br>O2E[1] | 0xC0<br>0xC0 | Oscillator Control | Control |
| IE2 | O1AE[0]<br>O1IE[1]<br>O2AE[2]<br>O2IE[3] | 0x29<br>0x29<br>0x29<br>0x29 | Interrupt Mask / Enable | Control |
| INTV<br>IINT2 | | 0x24<br>0x28 | Interrupt Vector Low Register<br>Interrupt Status | Status |

Table 13: Associated Registers for Oscillator Control (Oscillator 1 Example)

For a desired frequency $f_t$ the oscillator coefficient for Oscillator m, OmC[15:0], can be calculated with the following equations. The following equations can be used for both Narrowband and Wideband. The resulting hexadecimal coefficients are inputs to registers OSmCH and OSmCL.

$$O1C\ [15:0] = COS\left[\frac{2 * \pi * f_t}{16\ \text{kHz}}\right] * 2^{15} \qquad O2C\ [17:0] = COS\left[\frac{2 * \pi * f_t}{16\ \text{kHz}}\right] * 2^{17}$$

The initial condition for Oscillator m, OSmICL[15:0], can be calculated using the following equation. The following equations can be used for both Narrowband and Wideband.

$$\text{OmIC }[15:0] = A * \sin\left[\frac{2 * \pi * f_t}{16 \text{ kHz}}\right] * 2^{15} \qquad \text{(m: 1 , 2)}$$

"A" is calculated as the ratio of desired peak amplitude, $\mathbf{A_{PK}}$, with a peak D/A output of 1.5779 $\mathbf{V_{PK}}$. $\mathbf{A_{PK}}$ cannot exceed 1.2 $\mathbf{V_{PK}}$. The resulting hexadecimal coefficient is input to registers OSmICH and OSmICL.

$$A = \frac{A_{PK}}{1.5779}$$

| Frequency (Hz) | O1C[15:0] | $A_{PK}$ (Volts) | O1IC[15:0] |
|---|---|---|---|
| 697 | 0x7B3C | 0.31 | 0x06C5 |
| 770 | 0x7A37 | 0.31 | 0x0775 |
| 852 | 0x78E7 | 0.31 | 0x0839 |
| 941 | 0x775C | 0.31 | 0x090B |
| 1209 | 0x71D8 | 0.55 | 0x145B |
| 1336 | 0x6EC9 | 0.55 | 0x164E |
| 1477 | 0x6B11 | 0.55 | 0x1868 |
| 1633 | 0x6692 | 0.55 | 0x1AA4 |

| Frequency (Hz) | O2C[17:0] | $A_{PK}$ (Volts) | O2IC[15:0] |
|---|---|---|---|
| 697 | 1ECF0 | 0.31 | 0x06C5 |
| 770 | 1E8C5 | 0.31 | 0x0775 |
| 852 | 1E39B | 0.31 | 0x0839 |
| 941 | 1DD70 | 0.31 | 0x090B |
| 1209 | 1C75E | 0.55 | 0x145B |
| 1336 | 1BB22 | 0.55 | 0x164E |
| 1477 | 1AC43 | 0.55 | 0x1868 |
| 1633 | 19A48 | 0.55 | 0x1AA4 |

Table 14: Example Register settings for Oscillator m

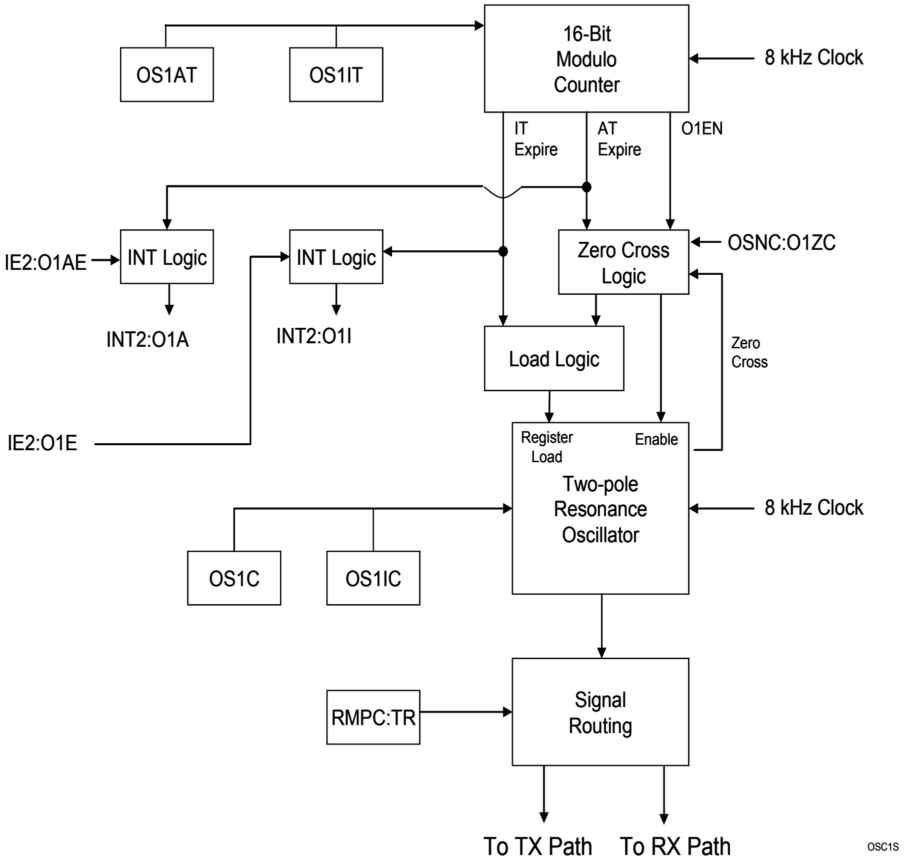


Figure 8: Block Diagram Oscillator 1

Each tone generator contains two timers, one for setting the active period and the other for the inactive period. Each period can be programmed between 0 seconds (timer disabled) to 8 seconds in 125µs increments. In addition, interrupts can be enabled on the expiration of either timer. The device has programmable cadence where the signal is generated during the active period and suspended during the inactive period.

One-shot control of the oscillation can be achieved by controlling OSN:O1E[0] and OSN:O2E[1] address (0xC0) together with the active timer and the interrupt for durations up to 8 seconds. For longer durations or for direct software control of the oscillation, enabling the active timer by setting it to any non-zero value while simultaneously disabling the inactive timer completely will put the oscillator under direct control of the OSN:OmE bit. Zero crossing detect can be enabled by setting the OSN:OmZC bit for the corresponding tone generator. Setting this bit will ensure that each oscillator pulse will end without a DC component as illustrated below.

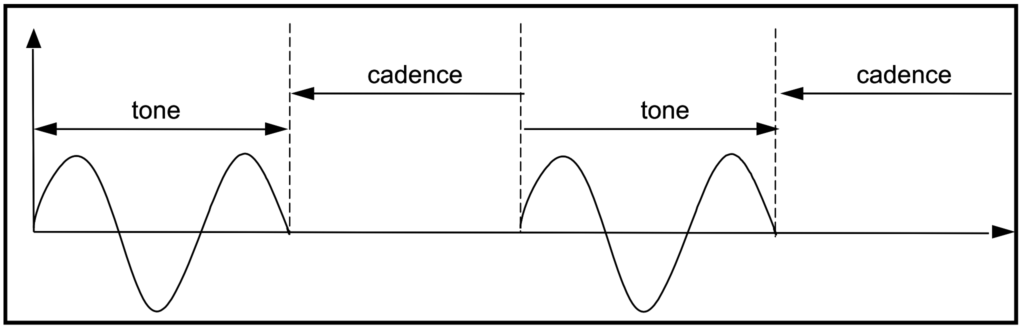


Figure 9: Zero Crossing for Tone Generation

Oscillator 2 is also specifically used to generate the Ringing signal and is unavailable for other functions during ringing. FSK generation does not utilize either one of the tone generation oscillators.

#### 12.1.3.2. RING SIGNAL GENERATION

The N681386/87 supports balanced and unbalanced Ringing up to 90 VPK (5 REN up to 4 kft, 4REN up to 4.5 kft, 3 REN up to 8 kft). Oscillator 2 from the Tone Generation block is used to generate the Ringing waveform. However, programming the waveform, sinusoidal or trapezoidal, involves some slight modifications to the procedures described for Tone Generation. The active and inactive timers of oscillator 2 can be programmed between 0 seconds (timer disabled) and 8 secs in 125us increments. A Ring phase delay can also be programmed in the OS2RPD:O2RPD[7:0] address (0xAD).

All other oscillator operations are standard and follow the description in the tone generation section. Interrupts can be enabled on the expiration of either timer, so that, for instance, Caller ID can be inserted between tones. Cadence is activated when a non-zero value is programmed into both the active and inactive timers. In this case, these timers effectively govern the transitions in and out of the Ringing state as described in Linefeed States of Operation in Section 6.1.1.1.

When the Ring Automatic bit LAMC:RGA[1] address (0x43) is set, the oscillator is automatically enabled when the Ringing state is entered and disabled when exited. If the Ring Automatic bit is enabled the transition from Ringing to Active state (Forward or Reverse) occurs automatically upon Ring Trip Detect. The oscillator enable and ring enable bits are automatically updated accordingly OSN:O2E[1] address (0xC0) and RMPC:R1EN[5] address (0xC1).

One-shot control of the oscillation can be achieved by controlling OSN:O2E[1] address (0xC0) together with the active timer and the active timer interrupt for durations up to 8 seconds. For longer durations or for direct software control of the oscillation, enabling the active timer by setting it to any non-zero value, while simultaneously disabling the inactive timer completely, will put the oscillator under complete direct control of the OSN:O2E[1] address (0xC0) bit. Zero crossing detect can be enabled by setting the OSN:O2ZC[3] address (0xC0). Setting this bit will ensure that the RING signal will end without a DC component. It is recommended that settings be reprogrammed only when the oscillator is disabled.

| Register Name | Register Name | Address | Parameter | Description / Range |
|---|---|---|---|---|
| RMPC | TRAP[7] | 0xC1 | Ringing Waveform | Sine/Trapezoid |
| OS2CL<br>OS2CH | O2C[17:0] | 0xC8<br>0xC9<br>0xDC | Ringing Frequency | 15 to 100 Hz for Sine Trapezoid Ramp Slope |
| OS2ICL<br>OS2ICH | O2IC[15:0] | 0xC4<br>0xC5 | Ringing Amplitude | 0 to 93.5 V Trapezoid tRISE / tPEAK |
| OS2RPD | OS2RPD[7:0] | 0xAD | Ringing Phase Delay | 0 to 32 ms |
| OSN | O2E[1] | 0xC0 | Ringing Oscillator Enable | Enable/Disable |
| OS2ATL<br>OS2ATH | O2ON[15:0] | 0xCC<br>0xCD | Ringing Oscillator Active Timer | 0V to 8 seconds |
| OS2ITL<br>OS2ITH | O2OFF[15:0] | 0xD0<br>0xD1 | Ringing Oscillator Inactive Timer | 0V to 8 seconds |
| OSN | O2ZC[5] | 0xC0 | Ringing Oscillator Zero Cross Enable | Enable/Disable |
| LS | LS[3:0] | 0x44 | Linefeed Status Control (Initiates Ringing State) | Ringing State = 0100b |
| VBHV | VBATH[5:0] | 0x4E | VBATH High Battery Voltage /2 | 0V to -93.5V in 1.484V steps |
| VCMR | VCMR[5:0] | 0x42 | VCMR Common Ringing Bias Adjust During Ringing | 0V to -93.5V in 1.484V steps |
| ROFFS | ROS[5:0] | 0xDC | Ringing DC voltage offset | 0V to +47.488 V in 1.484V steps |
| IE2 |  | 0x29 | Interrupt Enable | Controls |
| INTV<br>INT2 |  | 0x24<br>0x28 | Interrupt | Status |

Table 15: Registers for RING Generation

### 12.1.3.2.1. SINUSOIDAL RINGING

Sinusoidal Ringing is selected by setting RMPC:TRAP[7] address (0xC1) to LOW. For a desired frequency **$f_R$** is calculated and programmed as before (see section Tone Generation). The oscillator initial condition for oscillator 2 is set in register O2IC[15:0] address (0xC4 – 0xC5) according to the following equation.

| Description | Equation |
|---|---|
| Desired frequency $f_R$<br>*The resulting hexadecimal coefficient is input to registers **OS2CH** and **OS2C** and **ROFFS*** | $O2C\ [17:0] = COS\left[\frac{2 * \pi * f_R}{8\ kHz}\right] * 2^{17}$ |
| Oscillator initial condition for oscillator 2<br>*The resulting hexadecimal coefficient is input to registers **OS2ICH** and **OS2ICL*** | $O2IC\ [15:0] = A * \sin\left[\frac{2 * \pi * f_R}{8\ kHz}\right] * 2^{15}$ |
| A is calculated from the desired peak amplitude, **$A_{PK}$**, in volts | $A = \frac{A_{PK}}{96}$ |

Note that A is calculated differently for Tone Generation. Finally the precise phase position where the sinusoidal ringing signal begins transmitting can be controlled by programming a transmission or phase delay of up to 31.8 ms into OS2RPD:O2RPD[7:0] address (0xAD). If the zero-crossing feature is enabled signal transmission will end at the equivalent phase position.

| Target Frequency (Hz) | Frequency (Hz) | O2C[17:0] |
|---|---|---|
| 10 | 11.12 | 1FFFB |
| 11 | 11.12 | 1FFFB |
| 12 | 12.18 | 1FFFA |
| 13 | 13.15 | 1FFF9 |
| 14 | 14.07 | 1FFF8 |
| 15 | 15.73 | 1FFF6 |
| 16 | 16.49 | 1FFF5 |
| 17 | 17.22 | 1FFF4 |
| 18 | 18.60 | 1FFF2 |
| 19 | 19.27 | 1FFF1 |
| 20 | 20.51 | 1FFEF |
| 25 | 25.37 | 1FFE6 |
| 50 | 50.26 | 1FF9A |

Table 16: Example Ringer Register settings

### 12.1.3.2.2. TRAPEZOIDAL RINGING

Trapezoidal Ringing is selected by writing RMPC:TRAP[7] = 1 address (0xC1). Three parameters are required to specify a Trapezoidal RING Signal and they as follows:

- Desired frequency $f_t$ (period T)
- Desired amplitude $A_{PK}$
- Crest factor, CF

Three values are programmed across O2C[17:0] and O2IC[15:0] to describe the waveform.

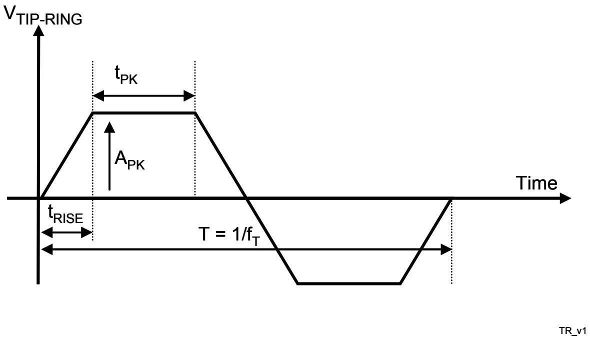


Figure 10: Trapezoidal Ringing

| Description | Equation |
|---|---|
| Calculated rise time ($t_{RISE}$) | $t_{RISE} = 0.375 * T * \left(1 - \left(\frac{1}{CF^2}\right)\right)$ |
| The rise time, expressed as an integer number of periods of 8 kHz, OS2ICL<br>*The resulting hexadecimal coefficient is input to registers OS2ICL* | $O2IC[7:0] = t_{RISE} * 8 \ \text{kHz}$ |
| Calculated peak time ($t_{PK}$) | $t_{PK} = (0.5 * T) - (2 * t_{RISE})$ |
| The peak time, expressed as an integer number of periods of 8 kHz, OS2ICH<br>*The resulting hexadecimal coefficient is input to registers OS2ICH* | $O2IC[15:8] = t_{PK} * 8 \ \text{kHz}$ |
| Calculated ramp rate is specified in O2C[15:0]<br>*Oscillator 2 has 18-bit register. The resulting hexadecimal coefficient is written to registers ROFFS:O2C[7:6], OS2CL and OS2CH* | $O2C[15:0] = \frac{\left\lfloor \frac{A_{PK}}{96} \right\rfloor * 2^{15}}{t_{RISE} * 8 \ \text{kHz}}$ |
| Precise position where the trapezoidal signal begins transmitting. If the zero-crossing feature is enabled signal transmission will end at the equivalent phase position. | OS2RPD = transmission or phase delay of up to 32 ms |

#### 12.1.3.2.3. RINGING DC OFFSET AND COMMON MODE BIAS

A Ringing DC offset voltage $V_{ROFF}$ can be defined by setting ROFFS:ROS[5:0]

$$ROS[5:0] = \left(\frac{V_{ROFF}}{96}\right) * 2^6$$

Ringing DC Offset is enabled when ROFFS:ROS[5:0] contains a non-zero value. $V_{ROFF}$ is added to, or subtracted from, the AC ringing signal depending on the setting. Similarly a Common Ringing Bias voltage $V_{CMR}$ can be defined by setting the VCMR Register.

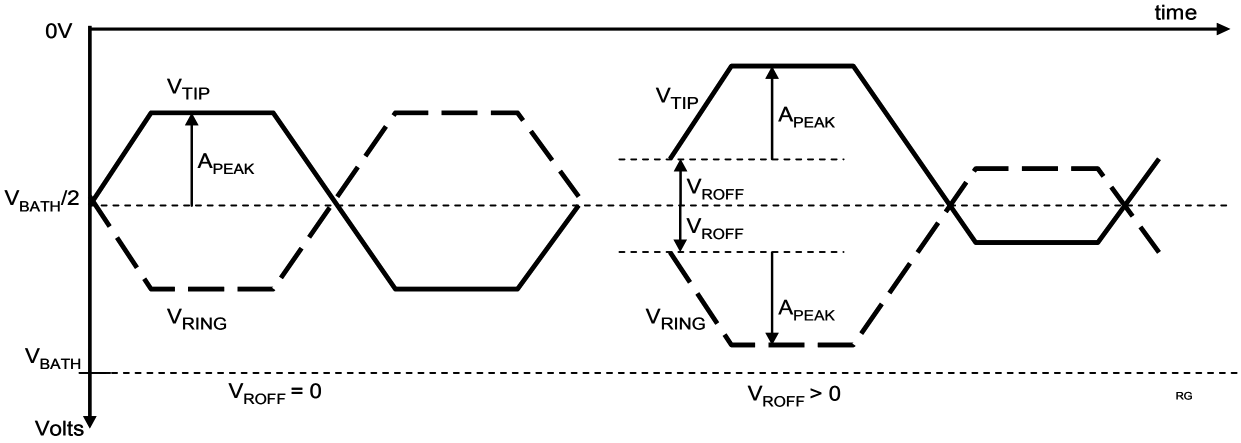


Figure 11: Positive DC offset for Trapezoidal Ringing

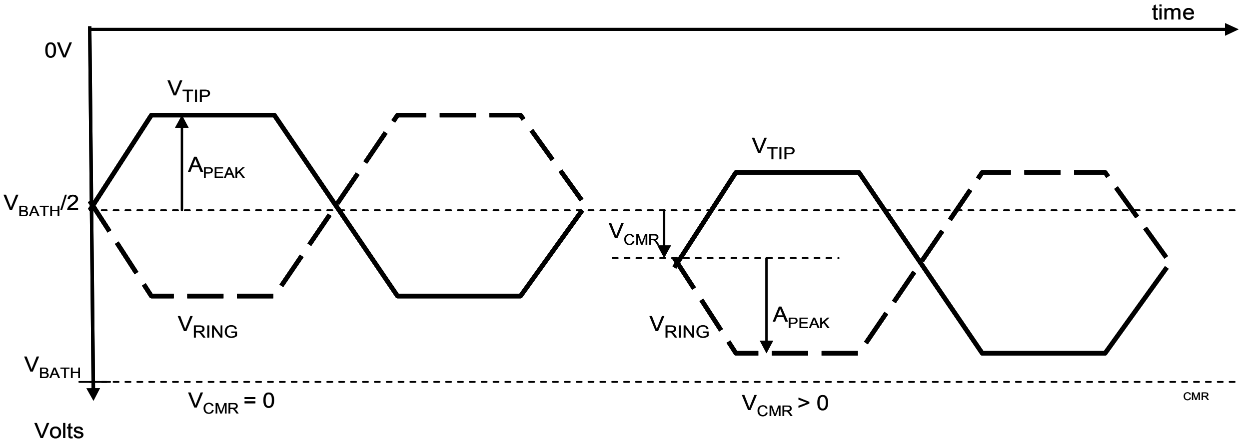


Figure 12: Programming $V_{CMR}$ voltage for Trapezoidal Ringing

#### 12.1.3.2.4. LINEFEED CONSIDERATIONS DURING RINGING

To maintain proper biasing of the external bipolar transistors the generated Ringing signal should stay between the Ringing voltage rails (GNDA and $\mathbf{V_{BATH}}$). If the ringing signal approaches the rails the signal will distort. Furthermore excessive power dissipation in the external transistors will also occur. This can be prevented if $V_{BATH}$ is programmed such that:

$$V_{BATH} > 2 \times \left( APEAK + V_{ROFF} \right) + V_{CMR}$$

### 12.1.3.3. INTERNAL UNBALANCED RINGING

An unbalanced ringing waveform can be generated by the N681386/87. This feature is enabled by setting GMV:UBR[7] address (0x4D) to “1”. The Ringing signal is only applied to the RING lead and the TIP lead remains at the programmed $V_{GM}$ voltage. The Ringing signal is programmed as described in section 9.1.3.1. A DC offset can be used to provide DC current for Ring Trip Detection (section 9.1.3.2.3). Positive $V_{ROFF}$ values will cause the DC offset point to move closer to ground. The internal unbalanced Ringing waveform is shown below.

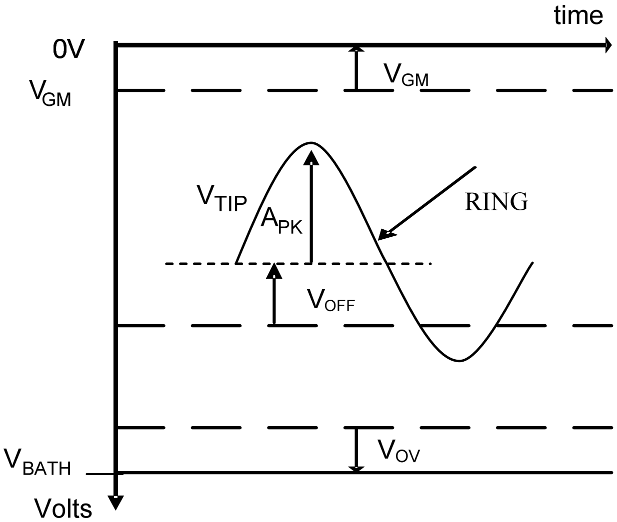


Figure 13: Unbalanced Ringing on TIP

The DC offset value should be set to less than half the ringing amplitude or the ringing signal will be clipped. Reverse unbalanced Ringing waveform can be achieved by setting the GMV:UBR[7] address (0x4D) bit to 1 (the TIP lead oscillates while the RING lead stays constant). In this mode, the polarity of $V_{ROFF}$ must also be reversed.

### 12.1.3.4. RING TRIP DETECTION

The Ring Trip Detection mechanism is used to recognize an off-hook event during Ringing. The N681386/87 monitors the Loop current through the Loop current circuitry (available at LPI:ILP[11:0] address (0x90)). If the shadow Linefeed state LS:SLS[7:4] address (0x44)indicates a Ringing state the loop current can used to evaluate whether a Ring Trip event has occurred under two alternative methods - AC path or DC path.

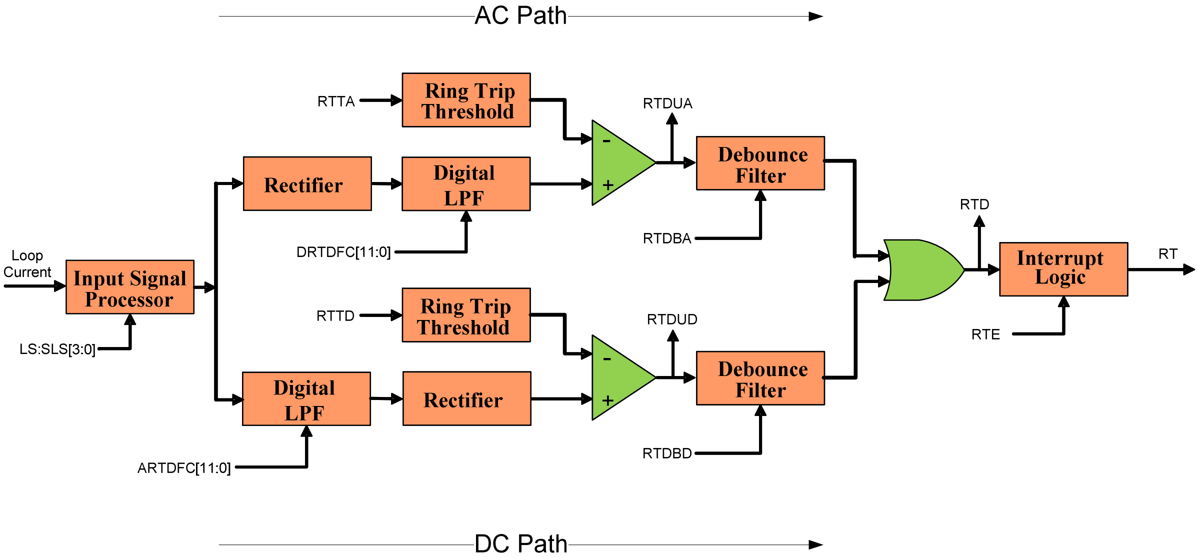


Figure 14: RING Trip Detection Mechanism

For the AC path the AC component of the loop current is determined by passing it first through a full-wave rectifier to remove the DC component and then through a Low Pass Filter for smoothing. The resulting value is compared to the AC path Ring Trip Threshold in register RTTA:ARTT[5:0] address (0x55). A subsequent debounce filter is programmed with an AC Path debounce interval from register RTDBA:ARTDI[7:0] address (0x48). If this interval is satisfied, a valid Ring Trip is judged to have occurred. However, RTLC:RTDUA[3] address (0x46) bit records the unfiltered status of the AC path Ring Trip Detect without regard to the debounce interval.

For the DC path the DC component of the loop current is determined by passing it first through a Low Pass Filter to remove the AC component and then though a rectifier to ensure a positive value. The resulting value then compared against the DC path Ring Trip Threshold in register RTTD:DRTT[5:0] address (0x67) and tested against the DC path debounce interval from register RTDBD:DRTDI[7:0] address (0x68). If this interval is satisfied, a valid Ring Trip is judged to have occurred. However, RTLC:RTDUD[4] address (0x46) bit records the unfiltered status of the DC path Ring Trip Detect without regard to the debounce interval.

If a RingTrip is judged to have occurred either on the AC path or on the DC path RTLC:RTD[1] address (0x46) bit is set. If enabled, a Ring Trip Interrupt will occur. If LAMC:RGA[1] address (0x43) is set the channel will automatically transition into the Active state (Forward or Reverse) upon a valid Ring Trip Detect.

In general, only one detection path should be utilized at one time by maximizing the Ring Trip Threshold value of the unwanted path.

| Register | Bit(s) | Address | Parameter | Description / Range |
|---|---|---|---|---|
| RTTA<br>RTTD | ARTT[5:0]<br>DRTT[5:0] | 0x55<br>0x67 | RING Trip Threshold AC & DC | 0 to 80 mA in 1.27 mA steps |
| RTDBA<br>RTDBD | ARTDI[7:0]<br>DRTDI[7:0] | 0x48<br>0x68 | RING Trip Detect Debounce Interval | 0 to 159 milliseconds |
| RTDFCLD<br>DCHA<br>RTDFCLD<br>DCHD | ARTDFC[7:0]<br>ARTDFC[11:8]<br>DRTDFC[7:0]<br>DRTDFC[11:8] | 0x51<br>0x52<br>0x65<br>0x66 | RING Trip Filter Coefficient | For Digital LPF |
| INT1 | RT[0] | 0x26 | RING Trip Interrupt Pending | Status |
| IE1 | RTE[0] | 0x27 | RING Trip Interrupt Enable | Enable/Mask |
| RTLC | RTD[1] | 0x46 | RING Trip Loop Closure Detect Status | Status |
| LS | SLS[3:0] | 0x44 | Linefeed Status Control | Ringing Shadow Status |
| LAMC | RGA[1] | 0x43 | Enable Oscillators and Transitions Automatically | Control |

Table 17: Registers for RING Trip Detection

The cutoff frequency, $f_{LP}$, of the Digital LPF is programmed in the Ring Trip Filter coefficient RTDFCA[11:0] and RTDFCD[11:0]:

$$\mathrm{RTDFCD}[11:0] = \left(1 - 2 * \pi * \left(\frac{f_{LP}}{800\mathrm{Hz}}\right)\right) * 2^{12} \qquad \mathrm{RTDFCA}[11:0] = \left(1 - 2 * \pi * \left(\frac{f_{LP}}{800\mathrm{Hz}}\right)\right) * 2^{12}$$

Values for RTDFCA, RTDFCD, RTTA, RTTD, RTDBD and RTDBA vary according to the programmed ringing frequency. The following table can be used for reference.

| Ringing Frequency | RTDFCD[11:0]<br>RTDFCA[11:0] | | RTTA<br>RTTD | | RTDBD<br>RTDBA | |
|---|---|---|---|---|---|---|
| Hz | Decimal | Hex | Decimal | Hex | Decimal | Hex |
| 16.667 | 3561 | 0x0DE9 | 34 mA | 3600 | 15 ms | 0x0C |
| 20 | 3453 | 0x0D7D | 34 mA | 3600 | 12.5 ms | 0x0A |
| 30 | 3132 | 0x0C3C | 34 mA | 3600 | 8.75 ms | 0x07 |
| 40 | 2810 | 0x0AFA | 34 mA | 3600 | 7.5 ms | 0x06 |
| 50 | 2489 | 0x09B9 | 34 mA | 3600 | 5 ms | 0x04 |
| 60 | 2167 | 0x0877 | 34 mA | 3600 | 5 ms | 0x04 |

Table 18: Recommended RING Trip Values for Ringing

### 12.1.4. SUPERVISION (SIGNALING)

#### 12.1.4.1. LOOP CLOSURE DETECTION

The recognition of an off-hook event outside Ringing is controlled by the Loop Closure Detect mechanism. Figure 16 shows the functional block.

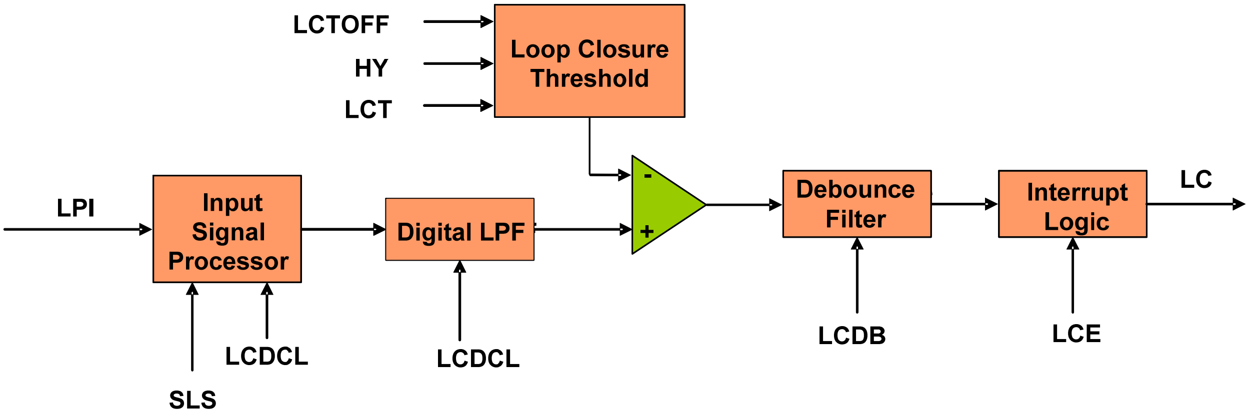


Figure 15: Loop Closure Detector Block Diagram

Loop current monitoring circuitry provides a Loop Current value which can be read at LPI:ILP[11:0] address (0x90) register. If the shadow linefeed state LS:SLS[7:4] address (0x44) indicates any state other than Open or Ringing state, the Loop Current value is fed to a digital Low Pass Filter to remove unwanted AC components. The cutoff frequency, $f_{LP}$, of the Digital LPF is programmed in the Loop Closure Detect Filter coefficient LCDCL:LCDC[11:0] address (0x50).

$$\mathrm{LCDC}[11:0] = \left(1 - 2 * \pi * \left(\frac{f_{LP}}{800\mathrm{Hz}}\right)\right) * 2^{12}$$

The resulting value is compared to a Loop Current Detect Threshold value in register LCT[5:0] address (0x53). However if the transition is an off-hook to an on-hook transition with hysteresis is enabled LCTHY:LCHYEN[6]=1 address (0x54), the threshold value in LCTHY:LCTOFF[5:0] address (0x54) is used in the comparison. A subsequent debounce filter is programmed with a debounce interval from register LCDB:LCDI[7:0] address (0x47). In addition, a special mask counter LCMCNT:LCMCNT[7:0] address (0xAB) can be enabled using RTLC:LCM[6] address (0x46) to guard against detects due to transients on the line, which can occur with reactive ringers. The RTLC:LCDU[2] address (0x46) bit records the unfiltered status of Loop Closure Detect without regard to the debounce interval or the Mask count. If the interval is satisfied a valid Loop Closure is judged to have occurred and the RTLC:LCD[0] address (0x46) bit is set. An interrupt can be enabled when the Loop Closure Interrupt occurred.

| Register | Bit(s) | Address | Parameter | Description / Range |
|---|---|---|---|---|
| LCT | LCT[5:0] | 0x53 | Loop Closure Threshold | Current Based: 0-80 mA @ 1.27 mA<br>Voltage based: 0-93.5V @ 1.484V |
| LPI | ILP[11:0] | 0x90 | Loop Closure | Current Based: 0-78.74 mA @ 1.25 mA |
| LCTHY | LCHYEN[6] | 0x54 | Enable Hysteresis | |
| LCTHY | LCTOFF[5:0] | 0x54 | Loop Closure Threshold Off-Hook to ON-HOOK state Enable Hysteresis | When hysteresis enabled only opposite transition governed by LCT.<br>Current Based: 0-80 mA @ 1.27 mA<br>Voltage based: 0-93.5V @ 1.484V |
| LCDB | LCDI[7:0] | 0x47 | Loop Closure Detect Debounce Interval | 0 to 159 milliseconds |
| LCDCL<br>DCH | LCDC[7:0]<br>LCDC[11:8] | 0x50<br>0x52 | Loop Closure Filter Coefficient | For Digital LPF |
| INT1 | LC[1] | 0x26 | Loop Closure Interrupt Pending | Status |
| IE1 | LCE[1] | 0x27 | Loop Closure Interrupt Enable | Enable/Mask |
| RTLC | LCD[0] | 0x46 | Loop Closure Detect Status | Status / Enable Voltage-based Loop Closure |
| LCMC | LCMCNT[7:0] | 0xAB | Loop Closure Detect Mask Counter | 0 to 319 ms in 1.25 ms steps |
| LAMC | LCDA[0] | 0x43 | Enable Automatic Transitions | Control |

Table 19: Loop Closure Detection Registers

If LAMC:LCDA[1] address (0x43) is set the channel will automatically transition from the Idle (Forward or Reverse), ON-HOOK Transmission (Forward or Reverse) as well as TIP Open or RING Open into the Active (Forward or Reverse) state upon a valid Loop Closure Detect.

Voltage based Loop Closure Detect can also be enabled by setting bit RTLC:VBLC[5] address (0x46). In this case the input signal is the Loop Voltage and the thresholds are interpreted as voltages. All other functionality is the same.

### 12.1.4.2. GROUND KEY DETECTION

Ground Key Detect (GKD) senses a DC current imbalance between the TIP and RING terminals when the RING terminal is connected to ground. This feature is commonly associated with PBX signaling. The feature is enabled in all states except Ringing. Figure below shows the functional blocks for ground key detector.

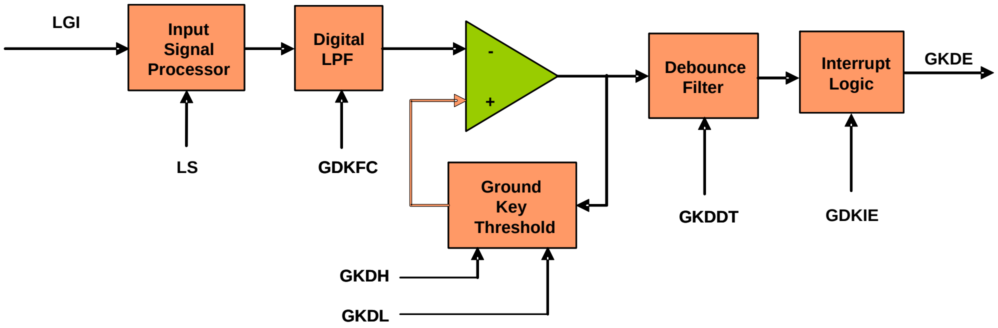


Figure 16: Ground Key Detection Circuitry

Ground Key Detection is enabled by setting the GKDFCH:GKDEN[7] address (0x64). The input to the GKD circuitry is the longitudinal current, which is available in register LGI:ILG[11:0] address (0x8C). If the shadow linefeed state LS:SLS[7:4] address (0x44) indicates a non-Ringing state, the longitudinal current is fed to a programmable Digital Low Pass Filter to remove any unwanted AC components. If $\mathbf{f_{LP}}$ is the desired cutoff frequency LPF the Low Pass Filter Coefficient GFDFC:FCGKD[11:0] address (0x63) is calculated using the following equation:

$$FCGKD[11:0] = \left(1 - 2 * \pi * \left(\frac{f_{LP}}{800Hz}\right)\right) * 2^{12}$$

A typical value of 10 (CKDFC:FCGKD[11:0] = 00A) is sufficient to filter out any unwanted ac artifacts while allowing the dc information to pass through the filter.

| Register | Bit(s) | Addr | Parameter | Range | Increment | Resolution |
|---|---|---|---|---|---|---|
| INT3 | GKDE[3] | 0x2A | Ground Key Interrupt Pending | Yes/No | N/A | N/A |
| IE3 | GKDIE[3] | 0x2B | Ground Key Interrupt Enable | Yes/No | N/A | N/A |
| GKDDT | DTGKD[7:0] | 0x62 | Ground Key Detect Debounce Interval | 0 to 320ms | 1.25ms | 1.25ms |
| LGI | ILG[11:0] | 0x8C | Longitudinal Current | Monitor only | | 500uA |
| GKDH | HGKD[5:0] | 0x60 | Ground Key Threshold (enabled) | 0 to 80 mA | 1.27mA | 1.27mA |
| GKDL | LGKD[5:0] | 0x61 | Ground Key Threshold (released) | 0 to 80 mA | 1.27mA | 1.27mA |
| GKDFC | FCGKD[11:0] | 0x63 | Ground Key Filter Coefficient | 0 to 4000h | N/A | N/A |

Table 20: Ground Key Detection Registers

The resulting value from the Low Pass Filter is compared to a Ground Key Detect High Threshold GKDH:HGKD[5:0] address (0x60) value. Hysteresis is enabled automatically by programming a second threshold GKDL:LGKD[5:0] address (0x61) to detect when the Ground Key is released. The output of the comparator is connected to a programmable debounce filter. It can be programmed with a debounce interval GKDDT address (0x62).

#### 12.1.4.3. CALLER ID AND FSK GENERATION

The N681386/87 provides an optimized Frequency-shift keying (FSK) generator for sending Caller ID information. Both Bell 202 and ITU-T V.23 standard FSK are supported. The FSK generation supports both Type I and Type II Caller ID with ability to generate CPE Alerting Signals (CAS tones) of 2130 Hz and 2750 Hz. The linear FSK waveform generator provides a mechanism to generate the linear code of FSK with continuous phase.

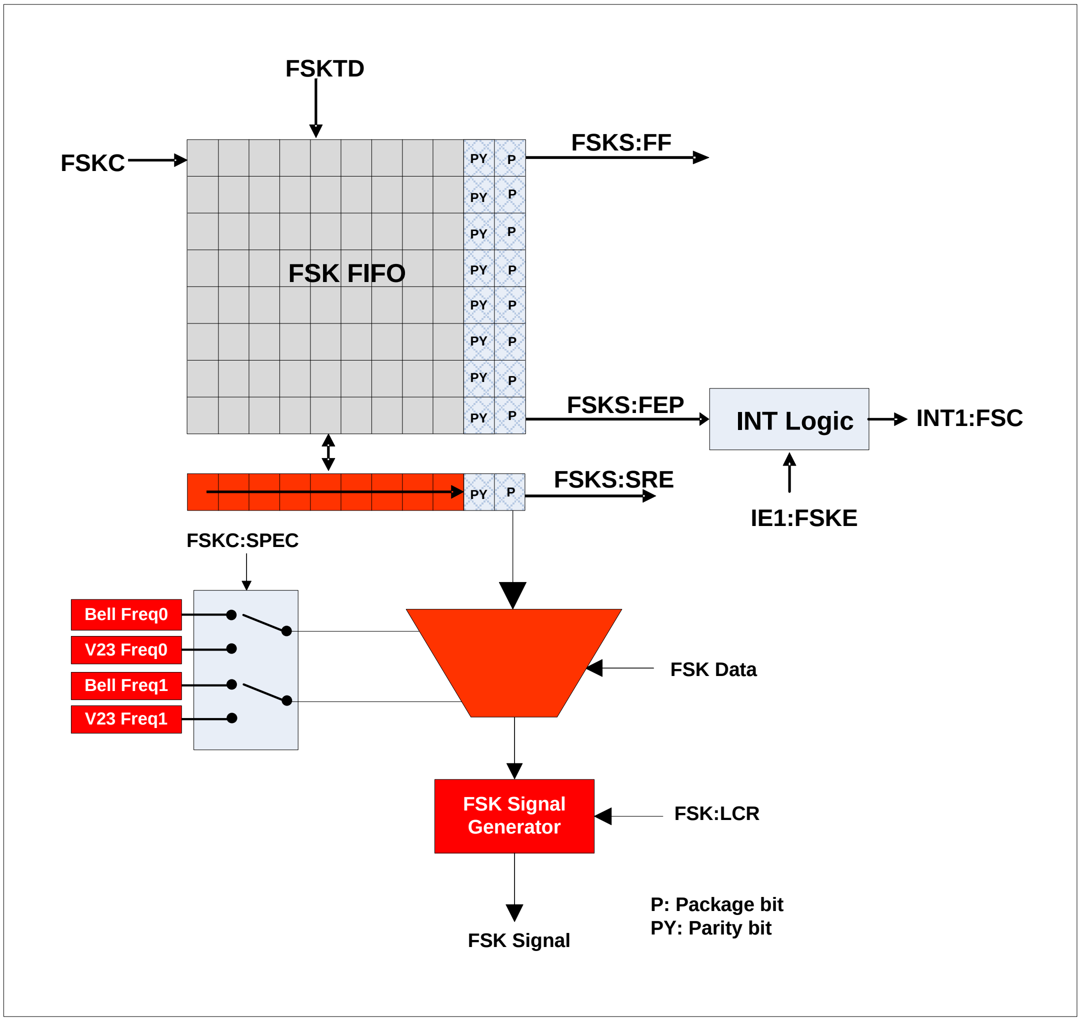


Figure 17: The Architecture of Linear FSK Waveform Generator

As the above figure illustrates, an 8-byte FIFO substantially reduces CPU intervention in generating FSK. Transmitted FSK data is placed in the FIFO by writing to the FSKTD:FSK[7:0] address (0x11) register. The writing process can be controlled by the status bits in the FSKS address (0x12) register which inform on the FIFO's current status.

FSK transmission is initiated by asserting FSKC:TX[3] address (0x10). The FSK transmit data is clocked out of the FIFO one byte at a time beginning with the LSB. If package mode is enabled a 'start bit' (Space) will automatically be amended to the head of the FSK transmit data. Furthermore, one or two 'stop bits' (Mark) are added to the end of the FSK transmit data, depending on the setting of FSKC:STOP[2] address (0x10). If package mode is not enabled the FSK transmit data is transmitted as it appears in the FSK FIFO.

There is one FSK generation engine available inside the N681386/87. An FSK interrupt is generated if the FIFO is empty. The gain of the FSK signal can also be adjusted using FSKLCR:GAIN[3:0] address (0x13) register.

| Register | Bit(s) | Address | Parameter | Description / Range |
|---|---|---|---|---|
| FSKC | | 0x10 | FSK Control Register | Control |
| FSKTD | FSK[7:0] | 0x11 | FSK Transmit Data | Binary signal to be transmitted |
| FSKS | FF[2]<br>FEP[0] | 0x12 | FSK Status Register | FIFO and Shift Register Status |
| FSKLCR | GAIN[3:0] | 0x13 | FSK Gain | See Register Description |
| FSKTCR | FSKR[1] | 0x14 | FSK Route | Route FSK Data |
| INT2 | FSKI[7] | 0x28 | Interrupt Status Registers | Status |
| IE2 | FSKIE[7] | 0x29 | Interrupt Enable Register | Enable/Mask |

Table 21: Registers for FSK Generation

#### 12.1.4.4. DTMF GENERATOR

In Dual Tone Multi Frequency (DTMF) two tones are used to generate a DTMF digit. One tone is chosen from four possible row tones, and one tone is chosen from four possible column tones. The sum of these two tones constitutes one of 16 possible DTMF digits.

| Row Frequency | Hz | Column frequency | | | |
|---|---|---|---|---|---|
| | | 1209 | 1336 | 1477 | 1633 |
| | 697 | 1 | 2 | 3 | A |
| | 770 | 4 | 5 | 6 | B |
| | 852 | 7 | 8 | 9 | C |
| | 941 | * | 0 | # | D |

Table 22: DTMF frequency mapping

DTMF tone generation can be achieved by using both oscillator 1 and oscillator 2. The table below illustrates the oscillator coefficient and initial condition which are required for the standard DTMF tone frequencies. For timing integrity both oscillators should be enabled simultaneously. Tones can be directed either towards the line or the PCM interface by programming the RMPC:TRAP[7] bit address (0xC1).

| Frequency (Hz) | $A_{PK}$ (Volts) | O1C[15:0] or O2C[17:2] | | OmIC[15:0] | |
|---|---|---|---|---|---|
| | | Decimal | Hex | Decimal | Hex |
| 697 | 0.31 | 31548 | 7B3C | 1733 | 06C5 |
| 770 | 0.31 | 31281 | 7A31 | 1909 | 0775 |
| 852 | 0.31 | 30951 | 78E7 | 2105 | 0839 |
| 941 | 0.31 | 30556 | 775C | 2315 | 090B |
| 1209 | 0.55 | 29144 | 71D8 | 2930 | 0B72 |
| 1336 | 0.55 | 28361 | 6EC9 | 3211 | 0C8B |
| 1477 | 0.55 | 27409 | 6B11 | 3513 | 0DB9 |
| 1633 | 0.55 | 26258 | 6692 | 3834 | 0EFA |

Table 22: DTMF frequency settings ($A_{PK}$ values for line impedance =600 Ω)

For a desired frequency $f_D$ the oscillator coefficient for Oscillator m, O1C[15:0] or O2C[17:2], can be calculated with the following equation. The following equations can be used for both Narrowband and Wideband. The resulting hexadecimal coefficients are register data of OSmCH and OSmCL.

$$\mathrm{O1C}[15:0] = \cos\left[\frac{2*\pi*f_D}{16\mathrm{kHz}}\right]*2^{15} \qquad \mathrm{O2C}[17:0] = \cos\left[\frac{2*\pi*f_D}{16\mathrm{kHz}}\right]*2^{17}$$

The initial condition for Oscillator m, OSmICL[15:0], can be calculated using the following equation. The following equations can be used for both Narrowband and Wideband.

$$\mathrm{OmIC}[15:0] = A*\sin\left[\frac{2*\pi*f_D}{16\ \mathrm{kHz}}\right]*2^{15} \qquad \text{(m: 1 , 2)}$$

Where A is calculated from the desired peak amplitude, $A_{PK}$, in volts in the following equation

$$A = \frac{A_{PK}}{1.5779}$$

The resulting hexadecimal coefficient is input to registers OS2ICH and OS2ICL.

#### 12.1.4.5. DTMF DETECTION

Dual Tone Multi Frequency (DTMF) tones consist of a low tone of 697Hz, 770Hz, 852Hz or 941Hz and high tone of 1209Hz, 1336Hz, 1477Hz or 1633Hz. The incoming signal is separated into high-group and low-group tones, and detected by high-group and low-group tone detectors respectively. When valid data is detected the result is pushed onto a FIFO which can be read by the host through the SPI interface.

When DTMF detection is enabled channel data is scanned for DTMF tones. Three critical time periods associated with detection can be programmed. A signal must be present for a minimum of PDT (Present Detect Time) before tone detection is triggered. Once valid tone is triggered, the tone must be present for ACCT seconds. Once this is true, DTMFRDY is active and the received data is pushed onto the FIFO. When the tone is removed, no detection is triggered for ADT (Absent Detect Time) seconds. DTMFRXDATA is decoded from the row and column frequency according to Table 22. The sensitivity and precision of detection can also be programmed.

When a DTMF tone is detected the N681386 can be configured to generate an interrupt to the host processor for service.

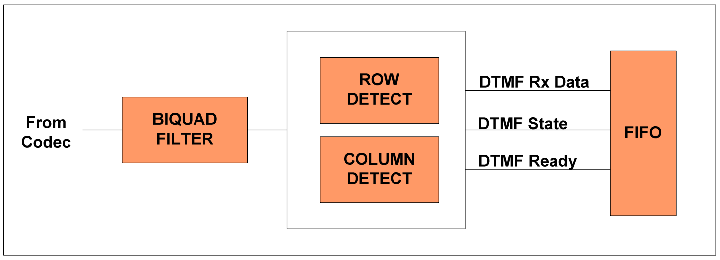


Figure 18: DTMF Detector - Functional Block Diagram

| Row Frequency | | Column frequency | | | |
|---|---|---|---|---|---|
| | | 1209 Hz | 1336 Hz | 1477 Hz | 1633 Hz |
| | 697 Hz | 1 | 2 | 3 | A |
| | | 0x01 hex | 0x02 hex | 0x03 hex | 0x0D hex |
| | 770 Hz | 4 | 5 | 6 | B |
| | | 0x04 hex | 0x05 hex | 0x06 hex | 0x0E hex |
| | 852 Hz | 7 | 8 | 9 | C |
| | | 0x07 hex | 0x08 hex | 0x09 hex | 0x0F hex |
| | 941 Hz | * | 0 | # | D |
| | | 0x0B hex | 0x0A hex | 0x0C hex | 0x00 hex |

Table 22: DTMF Tone Decoding

### 12.1.5. CODEC

The N681386/87 converts the analog transmit signal into a PCM code, either by using µ-Law, A-Law or linear PCM, and vice versa. A-Law, µ-Law and PCM encoding and decoding is performed according to the recommendations in the ITU-T G.711 specification. In the linear PCM mode a 16-bit 2s complement data format is used. Details of the Decode and Encode Characteristics are to be found in Section 11.

### 12.1.6. HYBRID

#### 12.1.6.1. AC PATH

The N681386/87 is used for digitizing and reconstructing the human voice. To digitize intelligible voice requires a signal to distortion ratio (S/D) of about 30 dB over a dynamic range of about 40 dB. N681386/87 meets this requirement by a large margin. The complete AC signal path block diagram is shown in Figure 3.

##### 12.1.6.1.1. NARROWBAND TRANSMIT PATH

The gain of this amplifier can be set by programming in APG:ATX[1:0] so that the signal takes advantage of the full range of the A/D. An anti-aliasing filter also precedes the A/D. The A/D produces a 16-bit linear PCM data stream sampled at 8 kHz. The A/D not only exceeds ITU G.712 and G.711 but also expands the voice-band cut-off frequency from a standard 3.4 kHz to 3.6 kHz for enhanced voice quality. High pass filter HXP implements the high-pass attenuation requirements for signals below 65 Hz. The linear PCM data stream is then amplified by the A/D digital gain amplifier, programmable from –inf dB to 6 dB and allowing fine gain adjustments down to a resolution of 0.1 dB. When enabled, the DTMF decoder can access this data stream at this point. Finally, if companding is selected, A-law or µ-law compression reduces the data stream to 8 bits wide. The timeslot on the PCM interface can be configured with either 8-bit compressed or 16-bit uncompressed data in mind.

##### 12.1.6.1.2. NARROWBAND RECEIVE PATH

In the receive path, data taken from the PCM highway can be 16-bit uncompressed or A-law / µ-law 8-bit compressed. In the latter case it is first expanded to 16-bit data. The linear PCM data stream is then amplified by the D/A digital gain amplifier, programmable from –∞dB to 6 dB and allowing fine gain adjustments down to a resolution of 0.1 dB. The data stream is then put through an optional high pass filter to filter out signals below 65 Hz and a low-pass interpolation filter again with 3.6 KHz cutoff frequency for enhanced voice quality before being passed to the D/A. Finally, the analog signal is amplified by the Analog Receive Amplifier. The gain of this amplifier can be set by programming in APG:ARX[1:0] before the signal is output from the chip.

The 12-bit digital gain blocks in both the transmit and receive paths provide 11 bits (1024 steps) for fine tuning the audio signals while the MSB can be used to invert the signal. To calculate the gain setting Y based on the desired dB setting X, the equation is:

$$Y = 1024 \times 10^{\left(\mathrm{XdB}/20\right)}$$

Conversely, to calculate the dB value of the gain based on known gain step values, the equation is:

$$X\ \mathrm{dB} = 20 \times \log\ 10^{\left(Y/1024\right)}$$

The table below contains a sample of possible gain settings.

| dB | Gain | Gain Setting (Y) |
|---|---|---|
| -∞ | Off | 0x000 |
| -24 | 1 / 8 | 0x040 |
| -12 | 1 / 4 | 0x100 |
| -6 | 1 / 2 | 0x200 |
| 0 | 1 | 0x400 |
| 6 | 2 | 0x7FF |

Table 23: Digital Gain Adjust Coefficients and Attenuation weightings

The device exceeds the maximum ITU requirements for frequency response, group delay distortion and signal to distortion as can be verified from the diagrams in Section 11. Audio signals larger than 0dBm0 can be processed without clipping in either compression scheme. The maximum PCM code generated for a sine wave is 3.17 dBm0 (μ-law) or 3.14 dBm0 (A-law).

The N681386/87 overload clipping limits are driven by the PCM encoding process. The presence of a high-pass filter transfer function ensures at least 30 dB of attenuation for signals below 65 Hz. The Low Pass Filter transfer function which attenuates signals above 3.6 kHz has to exceed the requirements specified by ITU G.714 and it is implemented as part of the A/D. The receive path transfer function requirement is very similar to the transmit path transfer function. We have added the high-pass filter portion as a user controlled option. Pass-band has been defined between 300 Hz to 3600 Hz. As the PCM data rate is 8 kHz, no frequencies greater than 4 kHz can be digitally encoded in the data stream.

#### 12.1.6.1.3. ANALOG TRANSHYBRID BALANCING

The N681386/87 provides fully programmable hybrid balancing to cancel transmit and receive signal echo on the full-duplex 2-wire pair. The hybrid balancing is performed at the internal 4-wire port. It is measured as the ratio of the un-cancelled return signal to the reference signal (digital-to-digital gain). Although the ITU standard recommends a hybrid balance below –18 dB within the voice band, care has been taken to reduce this further to –30 dB in order to avoid unacceptable voice quality for packet based networks.

The Tran hybrid Balance is internally set to subtract a –6 dB level from the transmit path signal, corresponding to the ideal case when the impedance matching perfectly matches the subscriber loop. This level can be adjusted from -

2.77 dB to +4.08 dB around this ideal setting by programming HB address (0x41). This register can also be used to disable the Tran hybrid balancing completely. It should also be noted that Tran hybrid Balance adjustments are independent of any other gain adjustment stages as the level shift occurs on the transmit path before any gain stages, as can be seen on Figure 3.

### 12.1.6.1.4. IMPEDANCE MATCHING

The device provides on-chip programmable two-wire impedance settings to meet a wide variety of worldwide two-wire return loss requirements.

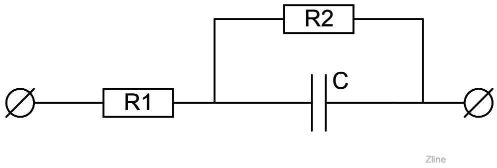


Figure 19: Characteristic Line Impedance

Figure above illustrates the characteristic line impedance model implemented on-chip. Examples of the standard impedances which the N681386/87 supports are shown below.

| Country | Requirement Impedance Element (Unit) | | |
|---|---|---|---|
| | R1(Ohm) | R2(Ohm) | C(Farad) |
| US PBX, Korea, Taiwan | 600 | Open | Short |
| Standard | 900 | Open | Short |

Table 24: Examples of Resistive Impedance Matching

Pure Resistive Impedance Settings (for example 600 Ohm and 900 Ohm) can be selected in IM1:ZR1[3:0]. In this case Complex Impedance Matching should be disabled by setting IMCTRL:IMEN[2] to 1. Register ILIM:ZCPEN[6] address (0x23) allows magnitude of the AC signal to be increased to compensate for the additional loss at the high end of the audio frequency range. ILIM:ZCPEN[6] should be enabled for Pure Resistive Impedance Matching cases.

| Country | Requirement Impedance Element (Unit) | | |
|---|---|---|---|
| | R1(Ohm) | R2(Ohm) | C(Farad) |
| Japan CO | 600 | Open | 1u |
| Bellcore | 900 | Open | 2.2u |
| CTR21 | 270 | 750 | 150n |
| China CO | 200 | 680 | 100n |
| China PBX | 200 | 560 | 100n |
| Japan PBX | 100 | 1000 | 100n |

| Country | Requirement Impedance Element (Unit) | | |
|---|---|---|---|
| | R1(Ohm) | R2(Ohm) | C(Farad) |
| India, New Zealand | 370 | 620 | 310n |
| Germany (Legacy) | 220 | 820 | 115n |
| UK (Legacy) | 320 | 1050 | 230n |
| Australia | 220 | 820 | 120n |

Table 25: Examples of Complex Impedance Matching

Complex Impedance Settings are realized using the Impedance Matching Coefficients loaded into IMRAM 0xF3 using control functions in IMCTRL 0xF5. In this case IM1:ZR1[3:0] should be should be set to 0 (600 Ohm Setting). ILIM:ZCPEN[6] should be disabled for Complex Impedance Settings.

#### 12.1.6.1.5. DAC/ADC AUTOMUTE

When the selected input data source is equal to zero for 1024 consecutive sample cycles, a mute signal is asserted to the analog front end to mute the line output signal. The control output is de-asserted on the first non-zero sample. Automute is enabled by setting AUTOMT:AUTOMTEN[7] address (0x5E). Automute has the capability of selecting two different options such as either DAC and ADC data or only DAC data by AUTOMTSEL[6] address (0x5E).

| Register | Bit(s) | Address | Parameter | Description / Range |
|---|---|---|---|---|
| AMT | AMTEN[7] | 0x5E | Automute Enable | 0 = Automute disabled (default)<br>1 = Automute enabled |
| AMT | AMTSEL[6] | 0x5E | Automute Select | 0 = DAC data+ADC data (default)<br>1 = DAC data only |

Table 26: Registers for Automute

| Automute Threshold | |
|---|---|
| **Modes** | **AMTTHR[5:0]** |
| Linear | 0 |
| u-Law | 0 |
| A-law | 8 |

### 12.1.7. TESTING

The N681386/87 includes extensive test and diagnostics features. Real-time DC linefeed measurements are available through the several voltages and current registers. GR-909 line test capabilities can also be supported. In addition five loop back test options, three digital loop backs (DLP1, DLP2 and DLP3) and two analog loop backs (ALP1, ALP2) are available. Figure 3, details the AC path architecture and also indicates the precise locations of the test loop backs.

#### 12.1.7.1. LOOP BACK TESTS

The full analog loop back LB:ALP2[4] address (0x21) allows the testing of almost all the circuitry of both transmit and receive paths. The compressed 8-bit/16-bit linear transmit data stream is fed back serially to the input of the receive path expander. The signal path starts with the analog signal at the input of the transmit path and ends with an analog signal at the output of the receive path. LB:ALP1[3] address (0x21) takes the digital stream at the output of the A/D in the transmit path and feeds it back to the input of the D/A in the receive path. As with LB:ALP2[4] address (0x21) the signal path starts with the analog signal at the input of the transmit path and ends with an analog signal at the output of the receive path.

Full digital loop back LB:DLP1[0] address (0x21) tests practically all transmit and receive path circuitry. The analog signal at the output of the receive path is fed back to the input of the transmit path by way of the Trans-hybrid filter path. The Trans-hybrid balance may be set to unity gain so that the return signal is not attenuated. A switch in the receive path is opened when this loop is selected so that no signal appears on the line during this loop back. The signal path starts with 8-bit/16-bit PCM data input to the receive path and ends with 8-bit/16-bit PCM data at the output of the transmit path. The user can bypass the companding process and interface directly to the 16-bit data. LB:DLP2[1] address (0x21) takes the digital stream at the input of the D/A in the receive path and feeds it back to the output of the A/D in the transmit path. The signal path starts with 8-bit/16-bit PCM data input to the receive path and ends with 8-bit/16-bit PCM data at the output of the transmit path. This loop back option allows the testing of the digital signal processing circuitry of the N681386/87 independent of any analog signal processing activity. DLP3 loops the digital data stream just beyond the PCM interface, taking the 8-bit/16-bit output of the PCM receive interface and looping directly to the input of the PCM transmit interface.

#### 12.1.7.2. DIAGNOSTICS SUPPORT

The N681386/87 provides a variety of registers which proved both voltages and current values from the line which are either measured or calculated (see tables 7 and 8). These registers are updated at a rate of 800 Hz or every 1.25 msec. Furthermore, the N681386/87 provides several mathematical and sampling resources to derive additional data useful in diagnostics (see illustration below). For example, peak to peak measurement results of the loop current and loop voltage is available in registers ILPP2P:LPIP2P[11:0] address (0x9C) and VLPP2P:LPVP2P[11:0] address (0x9B). These measured calculated and derived register values can be used to do GR-909 diagnostic tests.

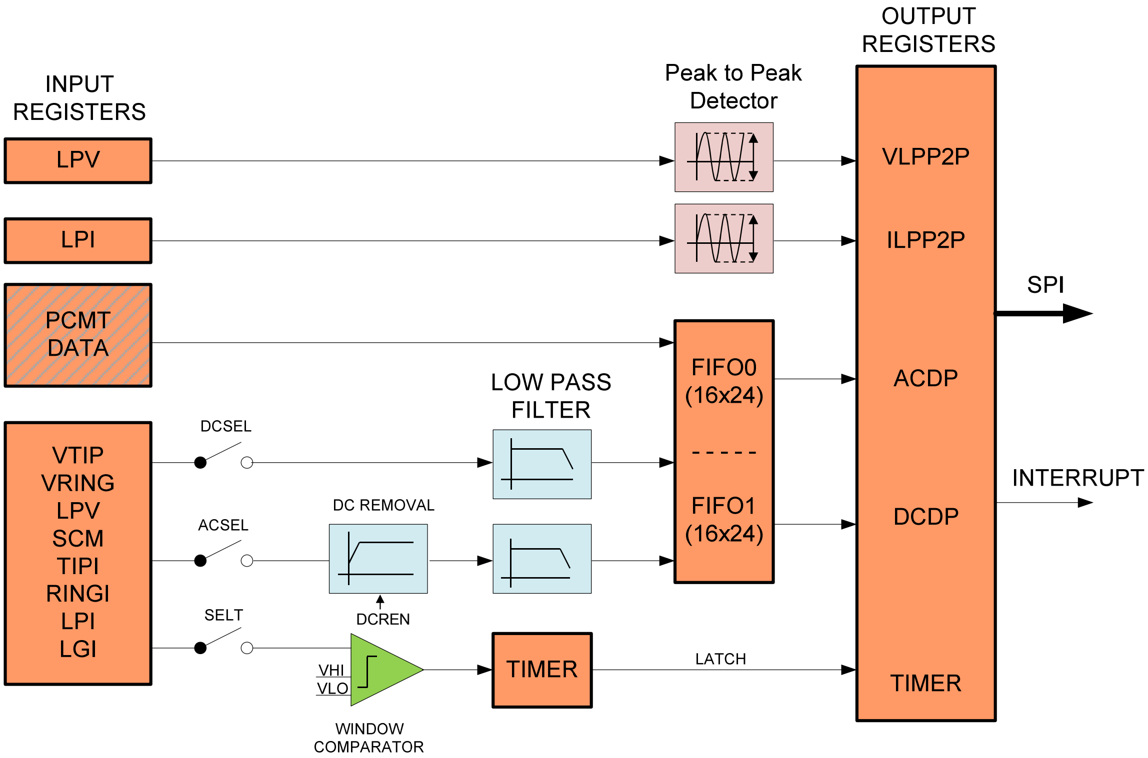


Figure 20: Diagnostics Support Block Diagram

### 12.1.8. POWER INTERFACE

The N681386/87 utilizes low-cost external components for to perform the DC/DC conversion to the high voltages required for the subscriber line interface (SLIC). The external discrete circuitry is controlled by on on-chip pulse width modulation (PWM) driver.

The battery voltage circuit and PWM driver provide a closed loop system for battery voltage regulation. Battery voltage, $V_{BAT}$, is monitored and compared to an internal target and adjustments are made accordingly. The target voltage will change, depending on different architectures and such factors as the linefeed state. As illustrated in

Figure 21 for example, if the device is operating in the constant voltage region the $V_{BAT}$ target is a combination of $V_{OV,}$ $V_{OH}$ and $V_{GM}$. A combination of coarse and fine adjustments ensures rapid convergence on the target voltage.

Two different DC/DC conversion architectures are supported and described in the following sections. Two different internal PLL master clocks (13.824 MHz, or 27.648 MHz) can be selected depending on the settings of PON:CDCC[7] address (0x22) and PLLS:PLLCM address (0x04). The width of the pulse generated by the PWM is programmed in PWMT:PT[7:0] address (0x49). A minimum off-time is programmable in the DDCC:DCOFF[7:0] address (0x4A) to allow sufficient time for stored energy to be transferred to the output capacitor. For reference monitoring the actual PWM pulse width can be checked in the read only PWCT:PWCT[7:0] address (0xB5) register. For example, if the PWCT indicates a maximum pulse width consistently, this might indicate an overload condition or a short circuit. The values for PWMT, DDCC and PWCT are based on multiples of the internal PLL master clock period.

| Register | Bit(s) | Address | Parameter | Description / Range |
|---|---|---|---|---|
| PON | CDCC[7] | 0x22 | Inductor Architecture | |
| PWMT | PT[7:0] | 0x49 | Sets PWM Pulse Width for DC/DC converter | Step size and initial value dependant on internal PLL clock selection |
| DDCC | DCOFF[7:0] | 0x4A | Sets PWM minimum Off time for DC/DC convertor | Step size and initial value dependant on internal PLL clock selection |
| PWCT | PWCT[7:0] | 0xB5 | PWM Count Register | For Reference (Read only) |
| DCTR | VTR[7:0] | 0x77 | DC/DC Target Voltage | 0V to -93.5V in 1.484V increments |
| OHV | VOH[5:0] | 0x4C | $V_{OH}$ On-Hook Voltage | 0V to -93.5V in 1.484V increments |
| GMV | VMV[5:0] | 0x4D | $V_{GM}$ Ground Margin Voltage | 0V to -93.5V in 1.484V increments |
| VBHV<br>VBLV | VBATH[5:0]<br>VBATL[5:0] | 0x4E<br>0x4F | $V_{BATH}$ High Battery Voltage<br>$V_{BATH}$ Low Battery Voltage | 0V to -93.5V in 1.484V increments |
| VOV | VOV[3:0] | 0x56 | $V_{OV}$ Offset Voltage | 0V to 24 V in 1.484 V increments |
| BATV | VB[7:0] | 0x80 | $V_{BAT}$ Battery Voltage | 0V to –95.88V in 0.376 V increments |

Table 27: Registers associated with DC/DC Conversion

#### 12.1.8.1. DC/DC CONVERSION (INDUCTOR)

A current sensing input for the DC/DC converter provided. The PWM pulse will be muted during each PWM cycle if the current exceeds a predetermined threshold level. This prevents the external discrete transistors from damage due to overload conditions. Similarly, the supply voltage is also monitored. The PWM pulse will be muted during each PWM cycle if the supply voltage falls below a predetermined level. The PWM pulse will also be muted if the battery voltage exceeds 10% of the maximum value. If this threshold is too high, an external clamp can be added in the application. See application diagram.

The Figure below illustrates how voltage regulation occurs in the Forward Active state.

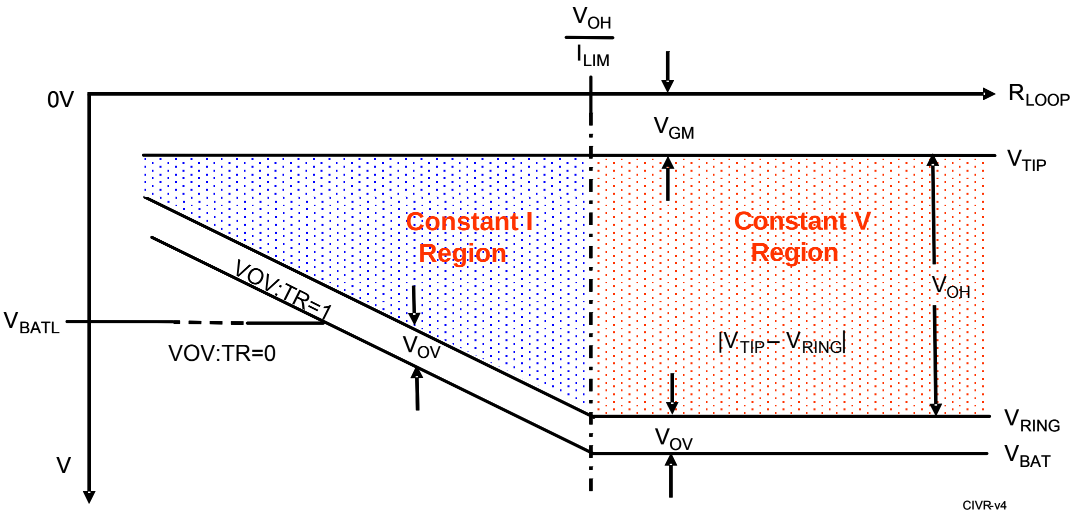


Figure 21: Voltage Tracking in Forward Active State

The values for $V_{GM}$, $V_{OH}$ and $V_{OV}$ are set in VCMR, OHV, and VOV registers respectively. When operating in the constant voltage region the $V_{BAT}$ is simply the sum of these three settings ($V_{GM}$ + $V_{OH}$ + $V_{OV}$). If the Loop current attempts to exceed $I_{LIM}$ the constant current region is entered. In this case the values for $V_{OV}$ and $V_{GM}$ are maintained but the $V_{OH}$ is adjusted to track the $R_{LOOP}$, which adjusts $V_{BAT}$ accordingly. If tracking is enabled, VOV:TR=1, tracking will continue below $V_{BATL}$. Otherwise, tracking will stop and $V_{BAT}$ will not go lower than $V_{BATL}$. A similar mechanism is implemented in the Reverse Active state.

During the Ringing state, the $V_{BAT}$ must be increased to accommodate the ring signal. Conventionally $V_{BAT}$ is set to a fixed value of $V_{BATH}$. However, the discrete linefeed circuit dissipates significant power particularly when a large REN load is applied. As an alternative the N681386/87 allows a dynamic battery target to be selected by setting the LCTHY:DBTR[7] address (0x54). In this case $V_{BAT}$ will dynamically track the actual ring signal, minimizing the power dissipation and improving efficiency during Ringing. Dynamic Battery Target is available only for DC/DC conversion architecture.

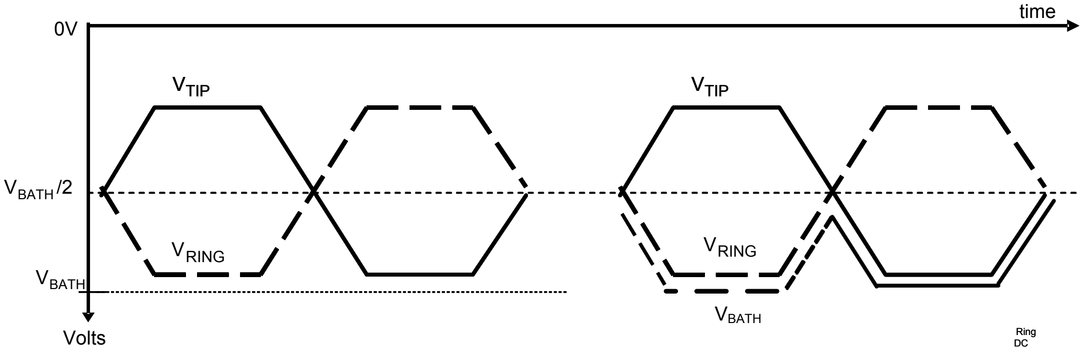


Figure 22: Dynamic Battery Target

#### 12.1.8.2. EXTERNAL BATTERY SWITCHING

The N681386/87 device can also operate from two or three external battery supplies. The external battery supply architecture can be enabled by pulling the XBAT Pin HIGH. This will also power down the on-chip PWM controllers. In this case the N681386/87 utilizes the DCPn and the DCNn pins to control the selection of externally supplied VBATR, VBATH and VBATL for VBAT by means of a external circuit such as the one illustrated below.

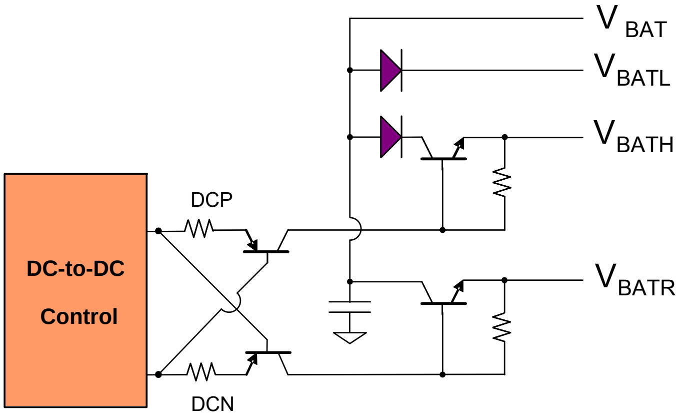


Figure 23: Three Voltage External Battery switching

The $V_{BAT}$ voltage selection is dependent on the linefeed state and the relationship is programmable. The mapping of the DCNn pins output to the linefeed state can be uniquely programmed in the XBSDCN address (0x6A) register as illustrated in the table below. The XBSDCP address (0x6B) register serves the same purpose for the DCPn pins. The combination of DCNn, DCPn outputs and the external selection circuitry allows either VBATR, VBATH or VBATL to be selected in any state.

When two external battery supplies are used (VBATH and VBATL) $V_{BAT}$ selection can be controlled by the one pin alone. Therefore, DCNn should be used to control the external battery switching.

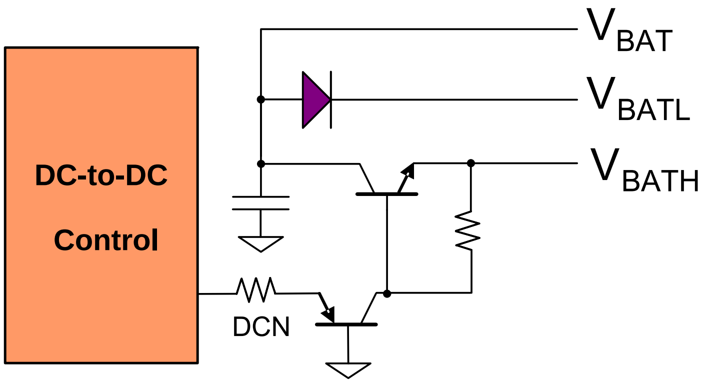


Figure 24: Two Battery Supply Control Circuit

## 12.2. DIGITAL INTERFACE

### 12.2.1. CLOCK GENERATION

The N681386/87 will generate the necessary internal clock frequencies from the BCLK input. BCLK must be synchronous to the 8 kHz frame sync clock and run at one of the following rates:

| Binary Clock | Decimal Clock |
|---|---|
| 256 kHz | 1.000 MHz |
| 512 kHz | 2.000 MHz |
| 768 kHz | 4.000 MHz |
| 1.024 MHz | 8.000 MHz |
| 1.152 MHz | |
| 1.536 MHz | |
| 1.544 MHz | |
| 2.048 MHz | |
| 4.096 MHz | |
| 8.192 MHz. | |

The frame sync can either be supplied externally or it can be generated internally by the N681386/87, by setting the PCMFS:FSS[2] address (0x05) bit to “1”. If frame sync is supplied externally (PCMFS:FSS=0), the ratio of the BCLK rate to the frame sync rate is determined via a counter clocked by BCLK which can be read at the PLLS:BCFS[4:1] address (0x04). This value is used to control the internal PLL, which multiplies BCLK appropriately to generate the internal clock frequency required to run the internal circuitry.

If the frame sync is supplied internally (PCMFS:FSS=1), the user must set PCMFS:BF[3:0] to indicate BCLK so that an appropriate multiple is calculated to generate the required internal frequency. If the frame sync is generated internally its width can be selected by programming PCMFS:IFST[3] address (0x05).

- 1-bit clock long (for Short Frame Sync, GCI and IDL modes)
- 8-bit clocks long (for 8-bit Long Frame Sync mode)

### 12.2.2. PCM INTERFACE

N681386/87 supports a flexible PCM interface structure which can be configured to perform multiple industry standard PCM modes. Data is received serially through the PCMR pin and transmitted serially through the PCMT pin.

Timeslots for data transmission and reception are independently configured using registers. Two registers, one for each direction combination, control the selection of the start point for the data timeslot:

- TTS[9:0]: Transmit Timeslot Start
- RTS[9:0]: Receive Timeslot Start
- The start point is defined in terms of a particular the BCLK period within the frame. Once the start of the timeslot is assigned the transfer will continue sequentially.
- For an 8-bit transfer the timeslot will run from the start point to the start point + 7 BCLK cycles.
- For a 16-bit transfer the timeslot will run from the start point to the start point + 15 BCLK cycles.

By setting the specific timeslot start points, the N681386/87 can be programmed to support many industry standard PCM interfaces including many Long Frame Sync and Short Frame Sync variants, IDL2 8-bit, 10-bit, B1 and B2 channel timeslots. The table below illustrates this by showing how some standard interface modes may be programmed.

| Clocking mode | BCLK PERIODS PER DATA BIT | TTS [7:0]<br>RTS [7:0] |
|---|---|---|
| Long Frame Mode | 1 | 0x00000 (slot 1) |
| Short Frame Mode | 1 | 0x00001 (slot 1) |
| GCI Mode | 2 | 0x00000 |
| IDL Mode | 1 | 0x00001 |

Table 28: Example Standard Interface modes

However N681386/87 allows even more flexibility. It can support BCLK up to 8192 kHz, or up to 1024 BCLK periods per 125usec frame. Therefore 10-bit timeslot assignment registers have sufficient flexibility to assign any timeslot start point within the frame. Care should also be taken when dealing with a BCLK lower than 8192 kHz to ensure that the timeslot start point is within the boundary of the frame, including sufficient headroom for the complete timeslot.

For example, if BCLK is 512 kHz there are 64 BCLK cycles within the frame. However, for all modes except Short Frame Sync the highest valid start position for 8-bit PCM data would be 56, sufficient for the full byte to be accommodated within the frame. For 16-bit data the highest start position would be 48. In Short Frame mode the LSB can be located up to the first BCLK of the next frame so the highest valid position is 56 for 8-bit or 48 for 16-bit.

The PCMT pin is high impedance except for the duration of the PCM transmit. PCMT will return to high impedance either on the negative edge of BCLK during the LSB, or on the positive edge of BCLK following the LSB depending on the setting of PCMC:TRI[2] address (0x00). Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots without the risk of driver contention.

#### 12.2.2.1. WIDEBAND AND NARROWBAND OPERATION

Nuvoton’s newest design in the Pro-X product line is a Narrowband and Wideband audio codec. The N681386 is limited to Narrowband audio codec communication, meaning 8kHz sampling and 8kHz frame sync with frame sync master mode capability. The Narrowband audio codec communication is compatible with the W681388, N681386, & W684386. The user could write to a reserved register that is used for Wideband operation on **N681386** without any effect to the Narrowband operation.

The **N681387** is capable of both Narrowband and Wideband audio communication. The WBAND pin which is only available on N681387 selects the Narrowband and Wideband. When WBAND pin is LOW the device is in narrowband mode and when the WBAND pin is HIGH the devices is operating in Wideband mode. However, a register PCMFS:WBEN[1] address (0x05) also needs to be programmed to ‘1’ in order to enable wideband operation.

This supports two scenarios:

1) The user permanently ties the ‘WBAND’ pin to VDD, while the PCMFS:WBEN[1] address (0x05) register is toggled to enable/disable Wideband
2) The user sets the register PCMFS:WBEN[1] address (0x05) to ‘1’ and controls the WBAND pin to enable/disable the Wideband operation.

The table below shows the modes of operation.

| WBANDPin | WBEN[1] | FSRATE[5] | FS Frequency | Band Operation (Filter & PCM) |
|---|---|---|---|---|
| GND | 0 | 0 | 8kHz | Narrow (Default) |
| GND | 1 | | | Narrow |
| VDD | 0 | | | Narrow |
| VDD | 1 | 0 | 8kHZ (1 FS with 2 Sample) | Wide |
| | | 1 | 16kHz (1 FS with 1Sample) | |

Table 29: Wideband or Narrowband Hardware Selection

The Narrowband mode is limited to 8kHz sampling and frame sync of 8kHz. The Wideband mode of operation is limited to 16kHz sampling and an option of 8kHz or 16kHz frame sync. The user needs to write a register PLLS:FSRATE[5] address (0x04) to indicate whether 8kHz (‘0’) or 16kHz (‘1’) frame sync rate is being used.

**There is no frame sync master mode supported in wideband operation.**

#### 12.2.2.2. TOGGLING BETWEEN WIDEBAND AND NARROWBAND

It is not recommended to toggle between Wideband and Narrowband when 16kHz frame sync is used, since it could unlock the PLL. However, the architecture may allow it when the pin is toggled at the right time.

For Wideband, using 8kHz frame sync, the user can toggle the WBAND pin or PCMFS:WBEN[1] address (0x05) register, while keeping the frame sync and bit clock running as is. The internal filter and PCM interface of the N681387 will switch to adjust to the Narrowband or Wideband mode of operation. This could lead to temporary glitches on the output while switching the filter. One could briefly mute the DAC and ADC path through the firmware code to prevent the glitches from being audible.

#### 12.2.2.3. PCM INTERFACE IN WIDEBAND OPERATION

##### 12.2.2.3.1. PCM INTERFACE 8KHZ FRAME SYNC

During Wideband operation and 8kHz frame sync the PCM data will be transmitted and received as two samples per frame sync. The location of the MSB of each sample on the PCM bus with respect to the frame sync pulse is programmable through two independent time slot registers. The time slots need to be programmed such that they are 62.5usec apart. An internal data ready signal will be generated to synchronize with the filters to indicate the data is ready and to synchronize the sample rate. The approximate timing diagram is shown below.

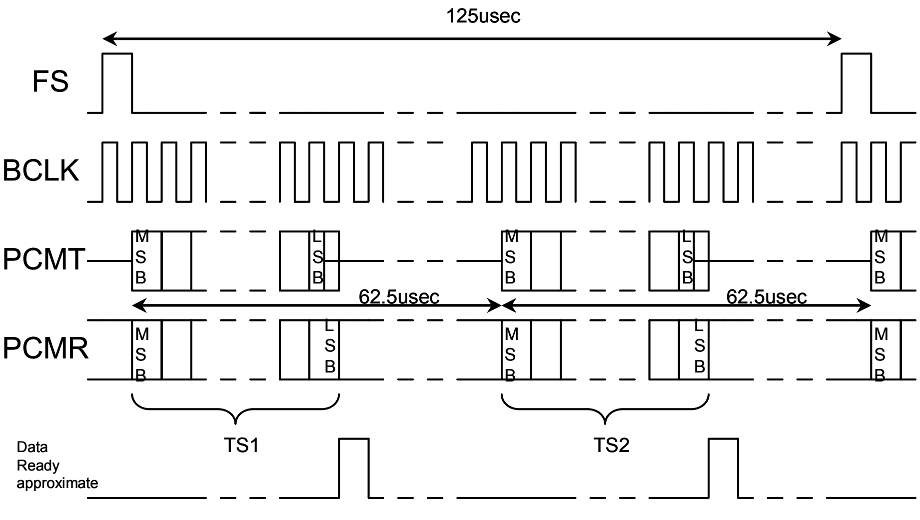


Figure 25: Wideband 8kHz Frame Sync PCM interface

### 12.2.2.3.2. PCM INTERFACE 16KHz FRAME SYNC

During Wideband operation and 16kHz frame sync the PCM data will be transmitted and received as one sample per frame sync. The location of the MSB of each sample on the PCM bus with respect to the frame sync pulse is programmable through one time slot register. The second timeslot register is not used in this case. Below is shown the approximate timing diagram for this case.

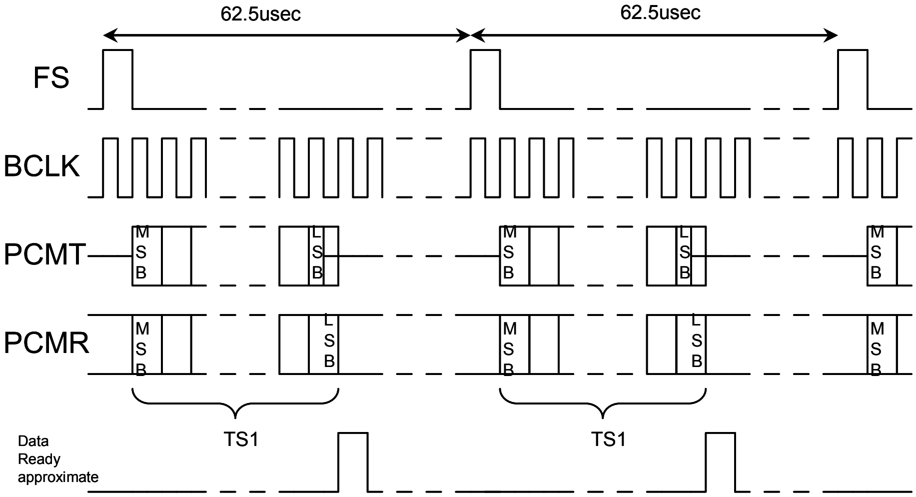


Figure 26: Wideband 16kHz Frame Sync PCM interface

### 12.2.2.4. PLL & PRESCALER IN WIDEBAND OPERATION

The prescaler determines the external bit clock frequency based on the ratio of the frame sync and bit clock frequency. When the frame sync switches to 16kHz (Wideband) it needs a signal to indicate this change in order to determine the correct bit clock frequency. In wideband and narrowband mode using 8kHz frame sync it doesn't need to adjust. Therefore, the PLL & prescaler operation can be summarized by the following truth table:

| WBAND pin | WBEN[1] | FSRATE[5] | PLLWBANDEN (switches prescaler) |
|---|---|---|---|
| GND | '0' | '0' | 0 |
| GND | '0' | '1' | 0 |
| GND | '1' | '0' | 0 |
| GND | '1' | '1' | 0 |
| VDD | '0' | '0' | 0 |
| VDD | '0' | '1' | 0 |
| VDD | '1' | '0' | 0 |
| VDD | '1' | '1' | 1 |

Table 30: PLL and Prescaler in Wideband

### 12.2.3. SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) is one of the widely accepted communication interfaces implemented in Nuvoton's Pro-X portfolio. SPI is a software protocol allowing operation on a simple 4-wire bus where the data is transferred MSB first. The SPI interface consists of a clock (SCLK), chip select (CSb), serial data input (SDI), and serial data output (SDO) to configure all the internal register contents. SCLK is static, allowing the user to stop the clock and then start it again to resume operations where it left off. The SCLK can run any speed up to internal PLL master clock (13.824MHz, 24MHz, or 27.648MHz depending on selected architecture). In the case of a write, DATA is sent by the micro-controller. In the case of a read, DATA is read by the micro-controller. To write data to the chip the controller must follow the following sequence

| | | |
|---|---|---|
| Device Address | Register Address | Data |

There are two different Read/Write architecture

- 8-bits Data Read/Write
  - The 8-bits data Write consists of 8-bits of Device Address, 8-bits of Register Address, and 8-bits of DATA.
  - The 8-bits data Read consists of 8-bits of Device Address, 8-bits of Register Address, and 8-bits of DATA.
- 16-bits Data Read/Write
  - The 16-bits data Write consists of 8-bits of Device Address, 8-bits of Register Address, and 16-bits of DATA.
  - The 16-bits data Read consists of 8-bits of Device Address, 8-bits of Register Address, and 16-bits of DATA.

The first byte, Device Address, sent to the N681386/87 from the host controller, following a CSb going HIGH to LOW, contains read/write bit, the Device type Identifier bits (wideband and narrowband selection information), and the burst mode. The 8-bits of the Device Address are explained below.

| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|---|
| Device Address | RW | 0 | 0 | 0 | 0 | CH | XP | BST |

Table 31: Device Address Bit pattern

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | 0 | 1 |
| 0 | Burst mode allows multiple consecutive registers to be written to or read using in a single sequence. The complete register address space (256 locations) can be read and written to using burst mode. | **BST** | Disable | Enable |

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | 0 | 1 |
| 1 | Control bit to select 12-Bits monitoring | **XP** | Bits[11-4] | Bits[3-0] |
| 2 | This is a channel selection bit. In case of a single channel device this bit must be set to “0” | **CH** | 0 | NA |
| 3 - 6 | Must be set to “0” for all operation | - | - | - |
| 7 | Read/Write control bit | **RW** | Write | Read |

| CH | XP | Command |
|---|---|---|
| 0 | 0 | Register Address (8-bits) |
| 0 | 1 | $2^{nd}$ byte of 12-Bits monitoring |

Table 32: 12-bit byte Selection

### 12.2.4. READ/WRITE SEQUENCE (8-BIT OR 16-BIT)

The device is accessed via the SDI input with data clocked in on the rising edge of SCLK. DATA transfer is synchronized to the SCLK input. Data is clocked out onto SDO on the falling edges of SCLK. SCLK is the only reference of SDI and SDO pins. The SDO pin will go tri-state when goes CSb HIGH

The first two pictures below illustrate the Read/Write Sequence for an 8-bit architecture. Both Read/Write sequences consist of three 8-bit transmissions, Device address, Register Address and Data. Each 8-bit transmission starts with the falling edge of the CSb line. At the end of every 8-bit transmission is complete the CSb transitions from LOW back to HIGH. After a valid Device Address and Register Address for Read, 8-bit Data is shifted out on the SDO line.

The last two pictures below illustrate the Read/Write Sequence for a 16-bit architecture. Both Read/Write sequences consist of two 16-bit transmissions, the first 16-bit transmission consisting of Device address and Register Address bytes and the second 16-bit transmission consists of Data. Each 16-bit transmission starts with the falling edge of the CSb line. At the end of every 16-bit transmission CSb transitions from LOW back to HIGH. After a valid Device address and Register Address for Read, 16-bits of Data is shifted out on the SDO line. Since all the registers are 8-bits long, the least significant byte of the 16-bit Data word should be ignored. If additional clocks are sent by the master the device will provide the same data when BST is LOW.

The SPI state machine soft resets whenever CSb asserts during an operation on an SCLK cycle that is not a multiple of eight, including burst mode. This is a mechanism for the controller to force the state machine to a known state when the controller and the device are out of synchronization.

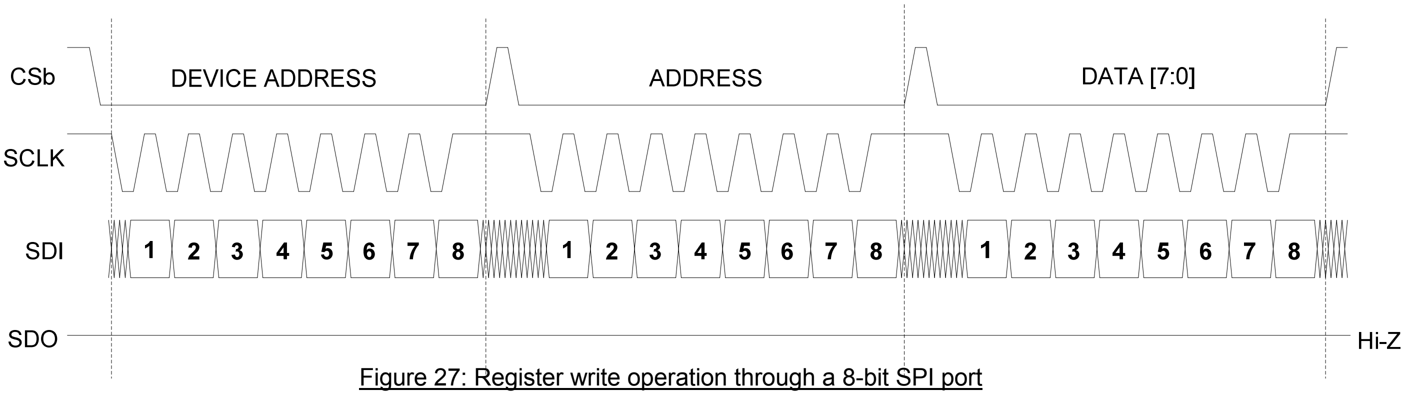


Figure 27: Register write operation through a 8-bit SPI port

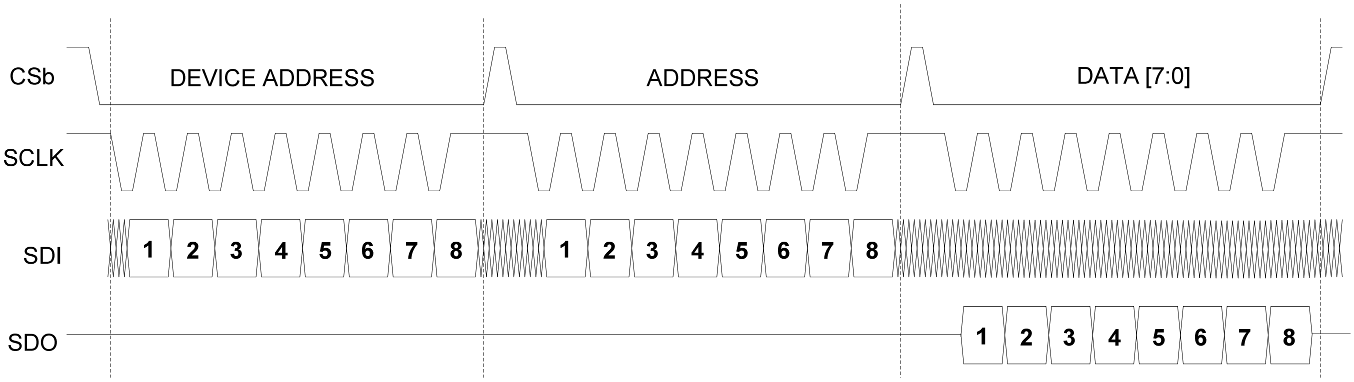


Figure 28: Register read operation through a 8-bit SPI port

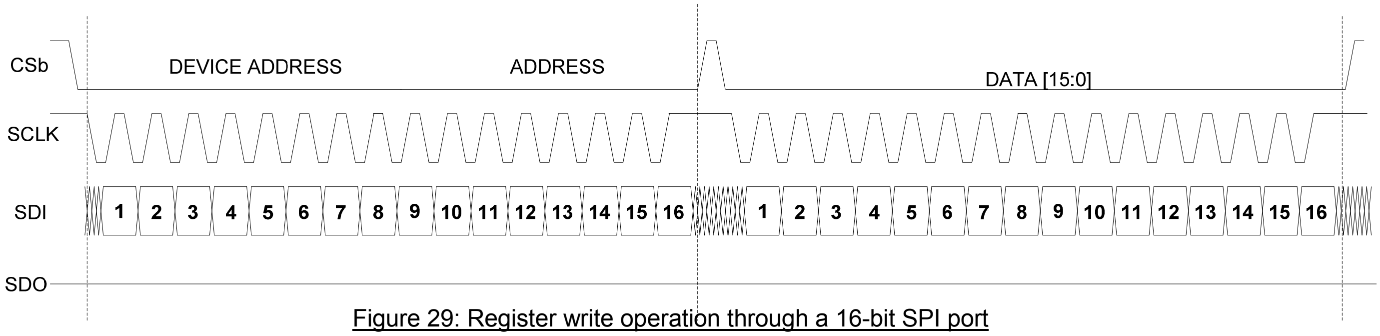


Figure 29: Register write operation through a 16-bit SPI port

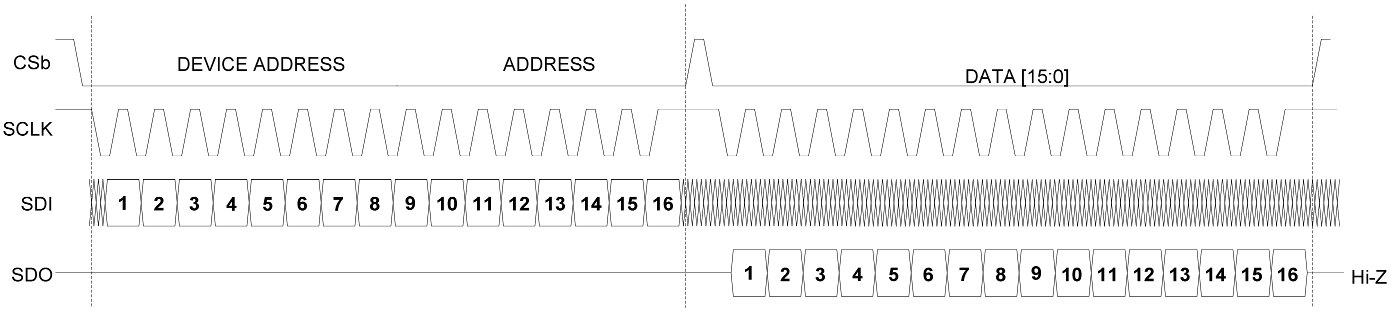


Figure 30: Register read operation through a 16-bit SPI port

### 12.2.5. SPI DAISY CHAIN

When using multiple N681386/87 devices, SPI programming can be accomplished using a daisy chain architecture which allows all chips to share one CSb and one SCLK. To enable the daisy chain configuration, the DSY pin should be set HIGH. In this configuration the SDO pin will no longer tri-state in order to pass the serial data to the next device in the chain. An internal 16-bit shift register in each device facilitates the daisy chain. After CSb goes LOW, SDI is clocked into this shift register at each rising edge of SCLK. At each falling edge of SCLK the contents of the shift register are shifted to SDO. SDO can then be connected to the SDI of the next chip in the daisy chain sequence. Each device evaluates the data in the internal shift register at the rising edge of CSb. Figure 35 illustrates a three-device daisy chain arrangement.

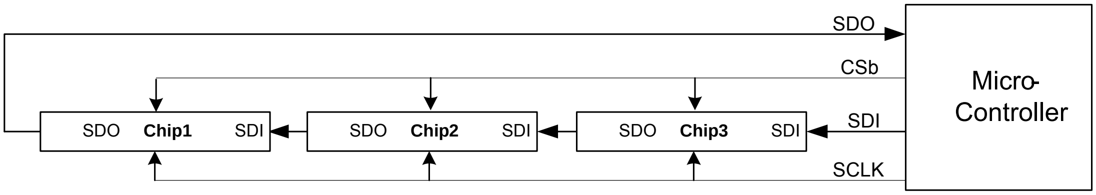


Figure 31: Three Chip Daisy Chain connection

For daisy chain operation, the length for Device address, Register Address and CSb should be 16xD bits, where D is the total number of devices in the daisy chain. Figure below illustrates the Device address, and Register Address structure for three-device daisy chain architecture. Three 16-bit Device address and Register Address words are sent sequentially, the first word for the first device in the daisy chain, the second word for the second device, etc. Device addressing is still enabled during daisy chain mode. Therefore, if a command needs to be ignored an unmatched device address can be sent with the command. If a command needs to be ignored a NOP can be sent with the command by sending a ‘1’ for any bit of C6 to C3.

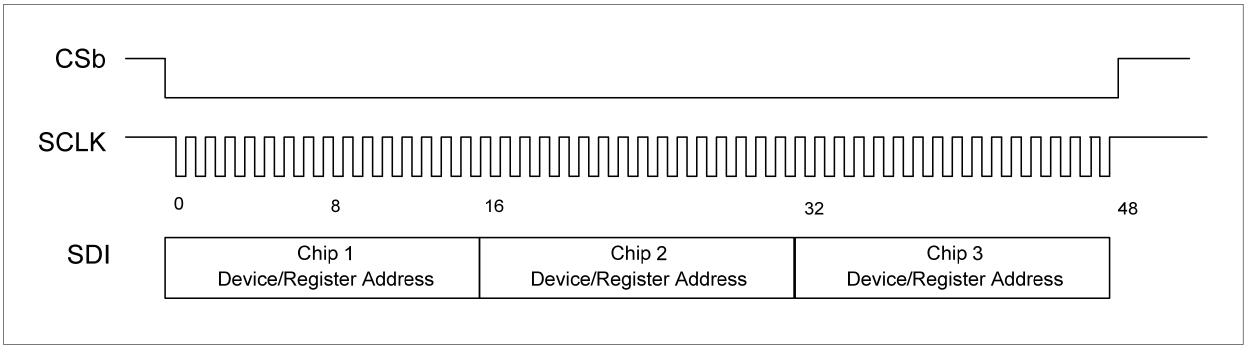


Figure 32: Device/Register Address for Three Device Daisy Chain application

Figure below illustrates the DATA structure for three-device daisy chain architecture. Three 8-bit DATA bytes are sent sequentially, the first byte for the first device in the daisy chain, the second byte for the second device, etc.

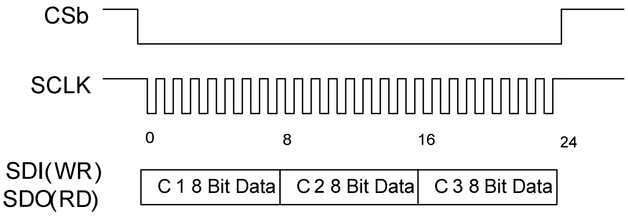


Figure 33: DATA for Three Device Daisy Chain application

### 12.2.6. SPI BURST MODE

The N681386/87 also supports a burst mode which allows multiple consecutive registers to be written to or read using a single Device address and Register address with BST=1. The complete register address space (256 locations) can be read/ written to using burst mode.

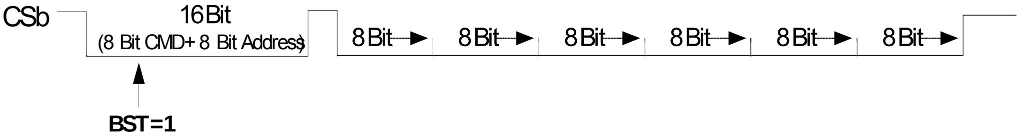


Figure 34: Burst mode operation (BST=1)

The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address (0x00) allowing the read cycle to be continued indefinitely.

When the BST bit in Device address is set during a write operation the N681386/87 will accept multiple 8-bit DATA blocks which will be written to sequential address locations beginning with the address specified in Register address. The length of the burst is determined by the Chip Select (CSb). Note that if there is a location within the sequence without a register assignment a dummy byte should be sent at the corresponding location in the DATA sequence.

Similarly during a burst read operation the device will output DATA as long as CSb is LOW. The device will output a dummy byte (0x00) when locations without register assignments are within the sequence. Register bits PCMC:BDAEN[3] address (0x00) and PCMC:BCEN[1] address (0x00) is be used to determine the broadcasting preferences. By default, after a reset, the device will accept all burst write commands without decoding bits C3 to C6. Once the PCMC:BCEN[1] address (0x00) bit is set, the device will only accept burst write data for the channel. Once the PCMC:BDAEN[3] address (0x00) bit is set, the device will only accept burst write data when C3 to C6 are ‘0’.

### 12.2.7. SPECIAL READ SEQUENCE FOR 12-BIT WIDE REGISTER

Although N681386/87 has 8-bit wide register map, it includes some additional register bits for accurate ADC monitoring. N681386/87 includes a special SPI Read feature. This read feature allows the user to read the 12-bits wide registers. It can be used in the 8-bits or 16-bits wide register data read mode. One important thing to remember is that BURST Mode cannot be use for 12-bit register read.

#### 12.2.7.1. 12-BIT READ SEQUENCE

Two separate read sequences I required to successfully read 12-bit register. Whether it is 8-bits or 16-bits wide register data N681386/87 still requires two byte read sequence. Selection of the second byte read is shown on one of the above table.

8-bits or 16-bits Data Read sequence for 12-bts ADC monitoring data

- **Sequence Read**
  - 1st byte Read
    - Device Address bits[2:1] – **00 binary**
    - Register Address any of the ADC monitoring registers
    - The 8 bits[7:0] of the first read data are the bits[11:4] of the 12-bits register

  - 2nd byte Read
    - Device Address bits[2:1] – **01 binary**
    - Register Address any of the ADC monitoring registers
    - The 4 MSB bits[7:4] of the second read data are the bits[3:0] of the 12-bits register

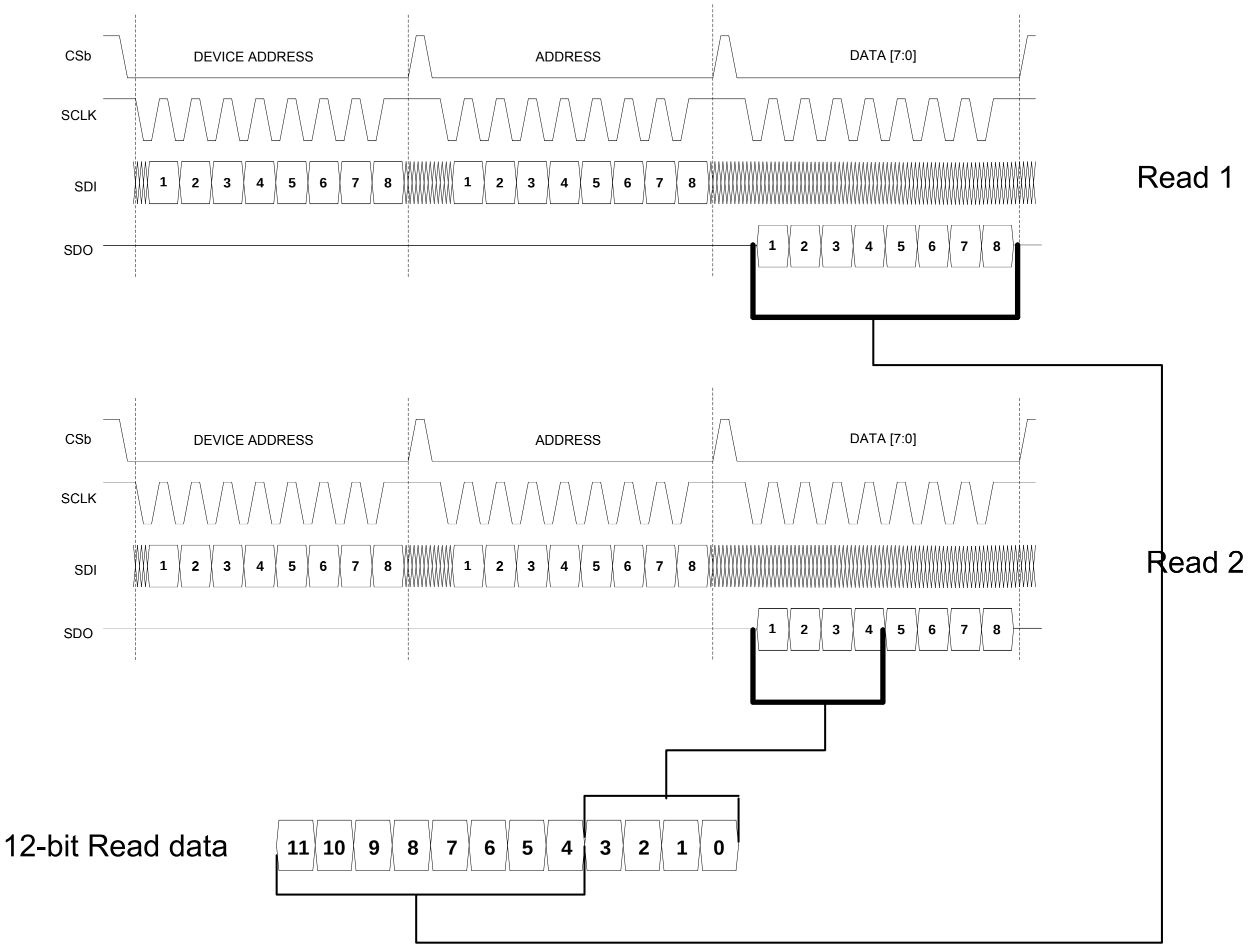


Figure 35: SPI 12-bits Read sequence

### 12.3. POWER-ON RESET

The following Power-on Reset procedure is recommended for the N681386/87.

- The Reset pin (RESETb) should be held LOW as power is applied.
  This allows logic levels to rise so that all output pins and all registers reach their default values while the system is in reset mode. This process should take less than 100 μs if the external supply is settled.
- Clocking should be applied (BCLK and, if necessary, FS)
- Ensure CSb and SCLK are set HIGH before setting RESETb HIGH
- Wait at least 400μs to ensure the PLL is locked. The status can be read in register PLLS:PL[0] address (0x04)
- Initialize all appropriate country specific registers and mode registers according to specific operating mode

### 12.4. INTERRUPT HANDLING

A number of events are capable of generating an interrupt. However, an interrupt signal is generated only if the bit corresponding to that particular interrupt event is enabled in the Interrupt Enable Register. In that case the corresponding bit is set in the Interrupt Status Register. An umbrella Interrupt Vector Register, INTV, indicates which Interrupt Status Registers have bits currently set. This vectoring allows an interrupt service routine to quickly determine which interrupt event has just occurred.

Once the interrupt has been serviced the Interrupt Status Register can be cleared by writing a one to that respective bit. The Interrupt Vector Register INTV bits will be cleared when there are no pending interrupts in the corresponding Interrupt Status Registers

| Register Name | Address | Parameter | Description / Range |
|---|---|---|---|
| INTV | 0x24 | Interrupt Vector Register | Vectors the interrupt location |
| INT1 | 0x26 | Interrupt Status Register 1 | Power Alarms, RING Trip and Loop Closure Interrupts |
| IE1 | 0x27 | Interrupt Enable Register 1 | Enables for Register 1 interrupts |
| INT2 | 0x28 | Interrupt Status Register 2 | FSK, DTMF, RING and Oscillator Interrupts |
| IE2 | 0x29 | Interrupt Enable Register 2 for | Enables for Register 2 interrupts |
| INT3 | 0x2A | Interrupt Status Register 3 | Temperature Interrupts |
| IE3 | 0x2B | Interrupt Enable Register 3 | Enables for Register 3 interrupts |

Table 33: Interrupt Registers

## 13. GENERAL DESCRIPTION FOR N681622 (LINEFEED CIRCUIT)

The N681622 is the first supporting chip of its kind in the Nuvoton's Pro-X line of products. It integrated the high voltage linefeed circuit. It can be used with N681386, N681387, N682386 and N682387. N681622 is designed to reduce substantial board space compared to the existing discrete implementation of the linefeed circuit. The N681622 operates from a 3.3V supply voltages. A small QFN20 package with exposed pad for thermal considerations allows for easy assembly and PCB design.

### 13.1. FUNCTIONAL DESCRIPTION FOR N681622 (LINEFEED CIRCUIT)

The N681622 integrates the following six transistors of the discrete line driver: QT1, QT2, QT3, QR1, QR2, and QR3. In the following register description there are some references to currents or voltages for these individual transistors. For the N681622 the important transistors are QT1, QT3, QR1, QR3. The following diagram shows a virtual circuit showing the equivalent positions of the these transistors inside the N681622.

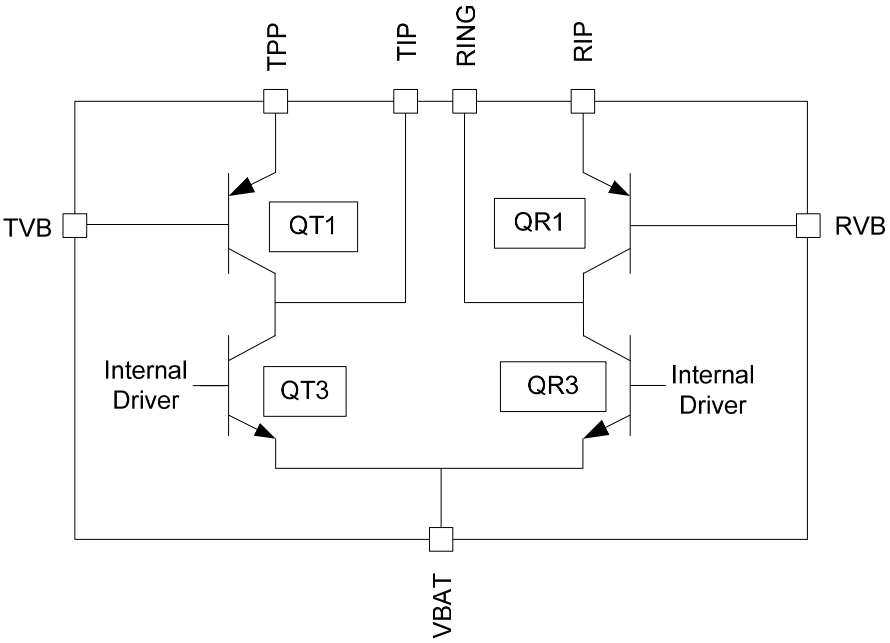


Figure 36: N681622 Equivalent Internal diagram

## 14. REGISTER DESCRIPTION

Please refer to the SPI command description to read and write instruction. For maximal forward compatibility, it is recommended that “0” be written to reserved bits.

“*RES*” in the register map means Reserved.

ASYNC means the device does not require a clock to be able to read or write

12-Bits – specific register has 12-bits

| Addr (Dec) | Addr (Hex) | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default (Hex) | R/W | ASYNC /12Bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | **PCM CONTROL REGISTERS** | | | | | | | | | | |
| 0 | 00 | **PCMC** | CMS[1:0] | | BM | GCLK | BDAEN | TRI | *RES* | EN | 00 | R/W | ASYNC (D5-D0) |
| 1 | 01 | **TTLNB** | TTSNB[7:0] | | | | | | | | 00 | R/W | ASYNC |
| 2 | 02 | **RTLNB** | RTSNB[7:0] | | | | | | | | 00 | R/W | ASYNC |
| 3 | 03 | **TCH** | RTSWB[9:8] | | TTSWB[9:8] | | RTSNB[9:8] | | TTSNB[9:8] | | 50 | R/W | ASYNC |
| 4 | 04 | **PLLS** | PLLCM | CLK1544EN | FSRATE | BCFS[3:0] (RO) | | | | PL (RO) | D9 | R/W | ASYNC (D7,D5) |
| 5 | 05 | **PCMFS** | BCF[3:0] | | | | IFST | FSS | WBEN | SRES | 00 | R/W | ASYNC (D7-D1) |
| 6 | 06 | **SIREV** | SIREV[7:0] | | | | | | | | 00 | R | |
| 7 | 07 | **DVID** | VER[7:0] | | | | | | | | C0 | R | |
| 8 | 08 | **TTLWB** | TTSWB[7:0] | | | | | | | | 00 | R/W | ASYNC |
| 9 | 09 | **RTLWB** | RTSWB[7:0] | | | | | | | | 00 | R/W | ASYNC |
| | | | **FSK REGISTERS** | | | | | | | | | | |
| 16 | 10 | **FSKC** | PE | PEN | PTYP | POL | TX | STOP | SPEC | EN | 00 | R/W | |
| 17 | 11 | **FSKTD** | FSK[7:0] | | | | | | | | 00 | R/W | |
| 18 | 12 | **FSKS** | RES | | | | | FF | *RES* | FEP | 03 | R | |
| 19 | 13 | **FSKLCR** | *RES* | | | | GAIN[3:0] | | | | 00 | R/W | |
| 20 | 14 | **FSKTCR** | *RES* | | | | | | FSKR | FMT | 00 | R/W | |
| | | | **Diagnostics** | | | | | | | | | | |
| 21 | 15 | **DIAGCTRL0** | FIFOIP | DCREN | ACLPFEN | DCLPFEN | FIFOEN | SIGNED | RES | DIAGEN | 00 | | |
| 22 | 16 | **DIAGCTRL1** | TRACNEG | ACSEL[2:0] | | | TRDCNEG | DCSEL[2:0] | | | 00 | | |
| 23 | 17 | **DIAGCTRL2** | VHI[7:0] | | | | | | | | 00 | | |
| 24 | 18 | **DIAGCTRL3** | *RES* | SELT[2:0] | | | VHI[11:8] | | | | 00 | | |
| 25 | 19 | **DIAGCTRL4** | VLO[7:0] | | | | | | | | 00 | | |
| 26 | 1A | **DIAGCTRL5** | DCRDC | DCRAC | DCRRC | *RES* | VOL[11:8] | | | | 00 | | |
| 27 | 1B | **DIAGCTRL6** | TIMER[7:0] (RO) | | | | | | | | 00 | | |
| 28 | 1C | **DIAGCTRL7** | TMREN | *RES* | | TIMER[12:8] (RO) | | | | | 00 | | |
| 29 | 1D | **DIAGCTRL8** | DCDP[11:0] (RO) ACDP[11:0] (RO) | | | | | | | | 00 | RO | |
| 30 | 1E | **DIAGFIFO0** | FIFO0[31:0] (RO) | | | | | | | | 00 | RO | |
| 31 | 1F | **DIAGFIFO1** | FIFO1[31:0] (RO) | | | | | | | | 00 | RO | |
| | | | **SYSTEM REGISTERS** | | | | | | | | | | |
| 32 | 20 | **PHF** | *RES* | | DACFF[1:0] | | ADCFF[1:0] | | ADCHP | DACHP | 80 | R/W | |
| 33 | 21 | **LB** | DACPOL | ADCPOL | *RES* | ALP2 | ALP1 | DLP3 | DLP2 | DLP1 | 00 | R/W | |
| 34 | 22 | **PON** | CDCC | *RES* | | | | DACPP | ADCPP | DCC | 01 | R/W | |
| 35 | 23 | **ILIM** | ZCPINV | ZCPEN | RNGGAIN | RIPS | TINS | ILMGAIN | CALTR1 | CALTR0 | 00 | R/W | |
| | | | **INTERUPT REGISTERS** | | | | | | | | | | |
| 36 | 24 | **INTV** | *RES* | | | | | IR3C1 | IR2C1 | IR1C1 | 00 | R/W | |
| 38 | 26 | **INT1** | PAT3 | PAR3 | PAT1 | PAR1 | PAR2 | PAT2 | LC | RT | 00 | R/W | |
| 39 | 27 | **IE1** | PAT3E | PAR3E | PAT1E | PAR1E | PAR2E | PAT2E | LCE | RTE | 00 | RO | |
| 40 | 28 | **INT2** | FSKI | DTMFI | RI | RA | O2I | O2A | O1I | O1A | 00 | R/W | |
| 41 | 29 | **IE2** | FSKIE | DTMFIE | RIE | RAE | O2IE | O2AE | O1IE | O1AE | 00 | R/W | |
| 42 | 2A | **INT3** | *RES* | | | | GKDI | *RES* | | TMP | 00 | R/W | |
| 43 | 2B | **IE3** | *RES* | | | | GKDIE | *RES* | | TMPE | 00 | R/W | |
| | | | **DTMF REGISTERS** | | | | | | | | | | |

| Addr (Dec) | Addr (Hex) | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default (Hex) | R/W | ASYNC /12Bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 | 30 | **DTMFCTRL1** | DTMFEN | ADCOSEL | DTMFFDEV[1:0] | | DTMFTC[3:0] | | | | 00 | R/W | |
| 49 | 31 | **DTMFCTRL2** | *RES* | | | | | | | DTMFCLR | 00 | R/W | |
| 50 | 32 | **DTMFCTRL3** | *RES* | | | | DTMFRCVDT[3:0] | | | | 00 | RO | |
| 51 | 33 | **DTMFST** | *RES* | | | | | | | DTMFEMT | 01 | RO | |
| 52 | 34 | **DTMFTHRH** | DTMFTHR[15:8] | | | | | | | | 01 | R/W | |
| 53 | 35 | **DTMFTHRL** | DTMFTHR[7:0] | | | | | | | | 00 | R/W | |
| 54 | 36 | **DTMFPDT** | DTMFPDT[7:0] | | | | | | | | 00 | R/W | |
| 55 | 37 | **DTMFADT** | DTMFADT[7:0] | | | | | | | | 00 | R/W | |
| 56 | 38 | **DTMFACT** | DTMFACT[7:0] | | | | | | | | 00 | R/W | |
| 58 | 3A | **DTMFRDT** | DTMFRDY | DTMFST | *RES* | | DTMFRDT[3:0] | | | | 00 | RO | |
| 59 | 3B | **DTMFRFH** | DTMFRF[15:8] | | | | | | | | 00 | RO | |
| 60 | 3C | **DTMFRFL** | DTMFRF[7:0] | | | | | | | | 00 | RO | |
| 61 | 3D | **DTMFCFH** | DTMFCF[15:8] | | | | | | | | 00 | RO | |
| 62 | 3E | **DTMFCFL** | DTMFCF[7:0] | | | | | | | | 00 | RO | |
| | | | **LINE REGISTERS** | | | | | | | | | | |
| 64 | 40 | **APG** | RAMP | PRE | VOHZ | *RES* | ARX[1:0] | | ATX[1:0] | | 00 | R/W | |
| 65 | 41 | **HB** | DACG | ADCG | *RES* | | | AHYB[2:0] | | | 1B | R/W | |
| 66 | 42 | **VCMR** | *RES* | | | VCMR[5:0] | | | | | 00 | R/W | |
| 67 | 43 | **LAMC** | *RES* | | | | | PAA | RGA | LCDA | 07 | R/W | |
| 68 | 44 | **LS** | SLS[3:0] | | | | LS[3:0] | | | | 00 | RO | |
| 69 | 45 | **LCL** | LGCRT | LGCRR | LGCM[1:0] | LGCRT | *RES* | ILM[2:0] | | | 00 | R/W | |
| 70 | 46 | **RTLC** | RTM | LCM | VBLC | RTDUD | RTDUA | LCDU | RTD | LCD | 00 | R/W | |
| 71 | 47 | **LCDB** | LCDI[7:0] | | | | | | | | 00 | R/W | |
| 72 | 48 | **RTDBA** | ARTDI[7:0] | | | | | | | | 00 | R/W | |
| 73 | 49 | **PWMT** | PT[7:0] | | | | | | | | FF | R/W | |
| 74 | 4A | **DDCC** | DCOFF[7:0] | | | | | | | | 76 | R/W | |
| 76 | 4C | **OHV** | *RES* | SB | VOH[5:0] | | | | | | 20 | R/W | |
| 77 | 4D | **GMV** | UBR | *RES* | VGM[5:0] | | | | | | 02 | R/W | |
| 78 | 4E | **VBHV** | XBATR | *RES* | VBATH[5:0] | | | | | | 32 | R/W | |
| 79 | 4F | **VBLV** | *RES* | | VBATL[5:0] | | | | | | 10 | R/W | |
| 80 | 50 | **LCDCL** | LCDC[7:0] | | | | | | | | 00 | R/W | |
| 81 | 51 | **RTDFCLD** | ARTDFC[7:0] | | | | | | | | 00 | RO | |
| 82 | 52 | **DCHD** | ARTDFC[11:8] | | | | LCDC[11:8] | | | | 00 | RW | |
| 83 | 53 | **LCT** | *RES* | | LCT[5:0] | | | | | | 00 | RO | |
| 84 | 54 | **LCTHY** | DBTR | LCHYEN | LCTOFF[5:0] | | | | | | 00 | R/W | |
| 85 | 55 | **RTTA** | *RES* | | ARTT5:0] | | | | | | 00 | R/W | |
| 86 | 56 | **VOV** | *RES* | | | TR | VOV[3:0] | | | | 00 | R/W | |
| 87 | 57 | **DCTON** | *RES* | | | TONDC[4:0] | | | | | 00 | R/W | |
| 94 | 5E | **AMT** | AMTEN | AMTSEL | AMTTHR | | | | | | 00 | R/W | |
| 95 | 5F | **XBTC** | *RES* | ASQH | CBP | XTBEN | XTBOT[1:0] | | XTBA[1:0] | | 00 | R/W | |
| | | | **GROUND KEY DETECTION REGISTERS** | | | | | | | | | | |
| 96 | 60 | **GKDH** | *RES* | | HGKD[5:0] | | | | | | 00 | RO | |
| 97 | 61 | **GKDL** | *RES* | | LGKD[5:0] | | | | | | 00 | R/W | |
| 98 | 62 | **GKDDT** | DTGKD[7:0] | | | | | | | | 00 | R/W | |
| 99 | 63 | **GKDFCL** | FCGKD[7:0] | | | | | | | | 02 | R/W | |
| 100 | 64 | **GKDFCH** | GKDEN | *RES* | | | FCGKD[11:8] | | | | 32 | R/W | |
| 101 | 65 | **RTDFCLD** | DRTDFC[7:0] | | | | | | | | 10 | R/W | |
| 102 | 66 | **DCHD** | *RES* | | | | DRTDFC[11:0] | | | | 00 | R/W | |
| 103 | 67 | **RTTD** | *RES* | XRTR | DRTT5:0] | | | | | | 00 | R/W | |
| 104 | 68 | **RTDBD** | DRTDI[7:0] | | | | | | | | 00 | R/W | |
| 106 | 6A | **XBSDCN** | DCNXB[7:0] | | | | | | | | 00 | R/W | |
| 107 | 6B | **XBSDCP** | DCPXB[7:0] | | | | | | | | 00 | R/W | |
| 110 | 6E | **LOAD** | *RES* | | | | | | | LOAD | 00 | R/W | |
| 119 | 77 | **DCTR** | VTR[7:0] | | | | | | | | C8 | RO | |

| Addr (Dec) | Addr (Hex) | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default (Hex) | R/W | ASYNC /12Bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | **MONITOR** | | | | | | | | | | |
| 120 | 78 | **RTMNT** | MNTRT[7:0] | | | | | | | | 00 | RO | |
| 121 | 79 | **LCMNT** | MNTLC[7:0] | | | | | | | | 00 | RO | |
| 122 | 7A | **MNT5** | MNTQ1[7:0] (QT1) | | | | | | | | 00 | RO | |
| 123 | 7B | **MNT7** | MNTQ2[7:0] (QR1) | | | | | | | | 00 | RO | |
| 124 | 7C | **MNT9** | MNTQ3[7:0] (QR2) | | | | | | | | 00 | RO | |
| 125 | 7D | **MNT11** | MNTQ4[7:0] (QT2) | | | | | | | | 00 | RO | |
| 126 | 7E | **MNT13** | MNTQ5[7:0] (QR3) | | | | | | | | 00 | RO | |
| 127 | 7F | **MNT15** | MNTQ6[7:0] (QT3) | | | | | | | | 00 | RO | |
| | | | **LINE CONTROL REGISTERS** | | | | | | | | | | |
| | | | **VOLTAGE REGISTERS** | | | | | | | | | | |
| 128 | 80 | **BATV** | VB[7:0] | | | | | | | | 02 | RO | |
| 129 | 81 | **VTIP** | VTIP[11:0] | | | | | | | | 000 | RO | 12-Bits |
| 130 | 82 | **VRING** | VRING[11:0] | | | | | | | | 000 | RO | 12-Bits |
| 131 | 83 | **QT3V** | QT3V[7:0] (VTVE) (VQT2) | | | | | | | | 02 | RO | |
| 132 | 84 | **QR3V** | QR3V[7:0] (VRVE) (VQR2) | | | | | | | | 02 | RO | |
| | | | **TRANSISTOR CURRENT REGISTERS** | | | | | | | | | | |
| 133 | 85 | **QT3I** | QT3I[11:0] | | | | | | | | 005 | RO | 12-Bits |
| 134 | 86 | **QR3I** | QR3I[11:0] | | | | | | | | 003 | RO | 12-Bits |
| 135 | 87 | **QT1I** | QT1I[11:0] | | | | | | | | 003 | RO | 12-Bits |
| 136 | 88 | **QT2I** | QT2I[11:0] | | | | | | | | 003 | RO | 12-Bits |
| 137 | 89 | **QR1I** | QR1I[11:0] | | | | | | | | 003 | RO | 12-Bits |
| 138 | 8A | **QR2I** | QR2I[11:0] | | | | | | | | 003 | RO | 12-Bits |
| | | | **LOOP SUPERVISION** | | | | | | | | | | |
| 140 | 8C | **LGI** | ILG[11:0] | | | | | | | | 001 | RO | 12-Bits |
| 141 | 8D | **LPV** | VLP[11:0] | | | | | | | | 001 | RO | 12-Bits |
| 142 | 8E | **TIPI** | ITLP[11:0] | | | | | | | | 002 | RO | 12-Bits |
| 143 | 8F | **RINGI** | IRLP[11:0] | | | | | | | | 000 | RO | 12-Bits |
| 144 | 90 | **LPI** | ILP[11:0] | | | | | | | | 001 | RO | 12-Bits |
| 145 | 91 | **POL** | *RES* | | P2PEN | ILGP | ILPP | IRLPP | ITLPP | VLPP | 1A | R/W | |
| 146 | 92 | **SCM** | SCM[11:0] | | | | | | | | 02 | RO | 12-Bits |
| 147 | 93 | **VEQT1** | VEQT1[7:0] | | | | | | | | 00 | RO | |
| 148 | 94 | **VQT1** | VQT1[7:0] | | | | | | | | 00 | RO | |
| 149 | 95 | **VEQR1** | VEQR1[7:0] | | | | | | | | 00 | RO | |
| 150 | 96 | **VQR1** | VQR1[7:0] | | | | | | | | 00 | RO | |
| 153 | 99 | **TEMP** | TS[7:0] (Vtemp) | | | | | | | | 00 | RO | |
| 154 | 9A | **VBGAP** | VBG[7:0] | | | | | | | | 4A | RO | |
| 155 | 9B | **VLPP2P** | LPVP2P[11:0] | | | | | | | | 000 | RO | 12-Bits |
| 156 | 9C | **ILPP2P** | LPIP2P[11:0] | | | | | | | | 000 | RO | 12-Bits |
| | | | **POWER ALARM LPF POLE REGISTERS** | | | | | | | | | | |
| 159 | 9F | **PALCNT** | PALCNT[7:0] | | | | | | | | 00 | RO | |
| 160 | A0 | **PALPQ2** | Q2C[7:0] | | | | | | | | 00 | R/W | |
| 161 | A1 | **PALPQn** | Q1C[7:0] | | | | | | | | 00 | R/W | |
| 162 | A2 | **PALPQ3** | Q3C[7:0] | | | | | | | | 00 | R/W | |
| 163 | A3 | **PALPQHn** | Q1C[11:8] | | | | Q2C[11:8] | | | | 00 | R/W | |
| 164 | A4 | **PALPQH2** | *RES* | Q3C12 | Q1C12 | Q2C12 | Q3C[11:8] | | | | 00 | R/W | |
| 165 | A5 | **PATHQ2** | Q2TH[7:0] | | | | | | | | 00 | R/W | |
| 166 | A6 | **PATHQn** | Q1TH[7:0] | | | | | | | | 00 | R/W | |
| 167 | A7 | **PATHQ3** | Q3TH[7:0] | | | | | | | | 00 | R/W | |
| | | | **IMPEDENCE MATCHING REGISTERS** | | | | | | | | | | |
| 168 | A8 | **IM1** | ZC[3:0] | | | | ZRn[3:0] | | | | 00 | R/W | |
| 169 | A9 | **IM2** | *RES* | ZSW | ZCP[1:0] | | ZR2C[3:0] | | | | 00 | R/W | |
| 170 | AA | **THAT** | THAT[7:0] | | | | | | | | 00 | R/W | |
| 171 | AB | **LCMCNT** | LCMCNT[7:0] | | | | | | | | 00 | RO | |

| Addr (Dec) | Addr (Hex) | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default (Hex) | R/W | ASYNC /12Bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 172 | AC | **CC** | *RES* | | | | CBGSW | CTRIM[2:0] | | | 00 | RO | |
| 173 | AD | **OS2RPD** | O2RPD[7:0] | | | | | | | | 00 | RO | |
| | | | **CALIBRATION REGISTERS** | | | | | | | | | | |
| 175 | AF | **CAL1** | SDAT[3:0] | | | | VBATT[3:0] | | | | 79 | RO | |
| 176 | B0 | **CAL2** | TVTE1[3:0] | | | | SDBT[3:0] | | | | 97 | RO | |
| 177 | B1 | **CAL3** | SCMT[3:0] | | | | RVTE1[3:0] | | | | 79 | RO | |
| | | | **DC OFFSET REGISTERS** | | | | | | | | | | |
| 180 | B4 | **IQTROS** | HISENSE | BTVR | ILFDB | DACSFC | *RES* | | | | 00 | R/W | |
| 181 | B5 | **PWCT** | PWCT[7:0] | | | | | | | | 00 | RO | |
| 182 | B6 | **CAL4** | XVRTS[3:0] | | | | XIRTT[1:0] | | *RES* | | 78 | R/W | |
| | | | **TONE GENERATION REGISTERS** | | | | | | | | | | |
| 192 | C0 | **OSN** | *RES* | | | | O2ZC | O1ZC | O2E | O1E | 08 | R/W | |
| 193 | C1 | **RMPC** | TRAP | LBAC | R1EN | *RES* | TOR | *RES* | | | 00 | R/W | |
| | | | **OSCILLATOR INITIAL CONDITION & COEFFICIENT REGISTERS** | | | | | | | | | | |
| 194 | C2 | **OS1ICL** | O1IC[7:0] | | | | | | | | 00 | R/W | |
| 195 | C3 | **OS1ICH** | O1IC[15:8] | | | | | | | | 00 | R/W | |
| 196 | C4 | **OS2ICL** | O2IC[7:0] | | | | | | | | 00 | R/W | |
| 197 | C5 | **OS2ICH** | O2IC[15:8] | | | | | | | | 00 | R/W | |
| 198 | C6 | **OS1CL** | O1C[7:0] | | | | | | | | 00 | R/W | |
| 199 | C7 | **OS1CH** | O1C[15:8] | | | | | | | | 00 | R/W | |
| 200 | C8 | **OS2CL** | O2C[9:2] | | | | | | | | 00 | R/W | |
| 201 | C9 | **OS2CH** | O2C[17:10] | | | | | | | | 00 | R/W | |
| | | | **OSCILLATOR ACTIVE & INACTIVE TIME REGISTERS** | | | | | | | | | | |
| 202 | CA | **OS1ATL** | O1ON[7:0] | | | | | | | | 00 | R/W | |
| 203 | CB | **OS1ATH** | O1ON[15:8] | | | | | | | | 00 | R/W | |
| 204 | CC | **OS2ATL** | O2ON[7:0] | | | | | | | | 00 | R/W | |
| 205 | CD | **OS2ATH** | O2ON[15:8] | | | | | | | | 00 | R/W | |
| 206 | CE | **OS1ITL** | O1OFF[7:0] | | | | | | | | 00 | R/W | |
| 207 | CF | **OS1ITH** | O1OFF[15:8] | | | | | | | | 00 | R/W | |
| 208 | D0 | **OS2ITL** | O2OFF[7:0] | | | | | | | | 00 | R/W | |
| 209 | D1 | **OS2ITH** | O2OFF[15:8] | | | | | | | | 00 | R/W | |
| | | | **GENERAL TONE GENERATION REGISTERS** | | | | | | | | | | |
| 220 | DC | **ROFFS** | O2C[1:0] | | ROS[5:0] | | | | | | 00 | R/W | |
| 221 | DD | **ADCL** | ADC[7:0] | | | | | | | | 00 | R/W | |
| 222 | DE | **DACL** | DAC[7:0] | | | | | | | | 00 | R/W | |
| 223 | DF | **DGH** | DAC[11:8] | | | | ADC[11:8] | | | | 44 | R/W | |
| | | | **DC-DC CONFIGURATION and OTHER FUNCTIONS** | | | | | | | | | | |
| 224 | E0 | **ST0L0** | *RES* | | | | ST0L0[3:0] | | | | 02 | R/W | |
| 225 | E1 | **ST1L0** | *RES* | | | ST1L0[4:0] | | | | | 04 | R/W | |
| 226 | E2 | **ST2L0** | *RES* | | | ST2L0[4:0] | | | | | 06 | R/W | |
| 227 | E3 | **ST0L1** | *RES* | | | | ST0L1[3:0] | | | | 08 | R/W | |
| 228 | E4 | **ST1L1** | *RES* | | | ST1L1[4:0] | | | | | 10 | R/W | |
| 229 | E5 | **ST2L1** | *RES* | | | ST2L1[4:0] | | | | | 19 | R/W | |
| 230 | E6 | **SK0L0** | SK0L0[7:0] | | | | | | | | 1F | R/W | |
| 231 | E7 | **SK1L0** | *RES* | | SK1L0[5:0] | | | | | | 04 | R/W | |
| 232 | E8 | **SK2L0** | *RES* | | | SK2L0[4:0] | | | | | 02 | R/W | |
| 233 | E9 | **SK0L1** | SK0L1[7:0] | | | | | | | | 1F | R/W | |
| 234 | EA | **SK1L1** | *RES* | | SK1L1[5:0] | | | | | | 04 | R/W | |
| 235 | EB | **SK2L1** | *RES* | | | SK2L1[4:0] | | | | | 02 | R/W | |
| 236 | EC | **WM0** | *RES* | | | WM0[4:0] | | | | | 08 | R/W | |
| 237 | ED | **WM1** | *RES* | | | WM1[4:0] | | | | | 10 | R/W | |
| 238 | EE | **WM2** | *RES* | | | WM2[4:0] | | | | | 18 | R/W | |
| 239 | EF | XSTEP | PWMTC | | | | XS[3:0] | | | | 53 | R/W | |
| 243 | F3 | IMRAM | IMDATA | | | | | | | | 00 | R/W | |

| Addr (Dec) | Addr (Hex) | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default (Hex) | R/W | ASYNC /12Bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 244 | F4 | IMDEL | IMHYBDC[3:0] | | | | IMB3PDC[3:0] | | | | 00 | R/W | |
| 245 | F5 | IMEN | *RES* | | | IMRW | *RES* | IMEN | IMR1M | IMPM | 10 | R/W | |
| 246 | F6 | PCMSCAL | PCMSCAL[7:0] | | | | | | | | 00 | R/W | |
| 247 | F7 | PCMSCAH | PCMSCAL[15:8] | | | | | | | | 20 | R/W | |
| 248 | F8 | | *RES* | | | | | | | | 00 | W | |
| 249 | F9 | | *RES* | | | | | | | | 00 | W | |
| 250 | FA | | *RES* | | | | | | | | 00 | W | |
| 251 | FB | IMEN | *RES* | | | | | | ADCLPFBYP | HBLPFBYP | 00 | R/W | |

### Decimal to Hex Conversion

To convert decimal value to hex value divide the decimal number by 16, and write the remainder on the side as the least significant digit. This process is continued by dividing the quotient by 16 and writing the remainder until the quotient is 0. When performing the division, the remainders which will represent the hex equivalent of the decimal number are written beginning at the least significant digit (right) and each new digit is written to the next more significant digit (the left) of the previous digit. Consider the number 175 decimal.

| Division | Quotient | Remainder | Hex Number |
|---|---|---|---|
| 175 / 16 | 10 = A | 15 = F | AF |

N681386/87 includes some bits that can be written without the PLL running while some bits requires the PLL running for the write to be effective. Any register that states the **ASYNC** bits means that specific DO NOT require the PLL running for the write to be effective.

### 14.1. PCM CONTROL REGISTERS

#### 14.1.1. PCM CONTROL REGISTER

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | Async (D0 - D5) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **0x00** | **PCMC** | CMS[1:0] | | BM | GCLK | BDAEN | TRI | *RES* | EN | 0x00 | |

The following table explains the PCM control register bits.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | PCM path including digital receive path | **EN** | Disable | Enable |
| 2 | Tri-state PCMT LSB | **TRI** | Positive edge of BCLK | Negative edge of BCLK |
| 3 | Burst Device Address decode enable | **BDAEN** | All Devices in Parallel | Single Device |
| 4 | GCI Clock Format (per data bit) | **GCLK** | 1 BCLK | 2 BCLK |
| 5 | Must be set appropriate to PCMC:CMS selection | **BM** | 8-bit mode | 16-bit mode |

There are three different CODEC Modes to choose from and they are as follows:

| CODEC MODE SELECTION | | |
|---|---|---|
| **CMS1** | **CMS0** | **Mode** |
| 0 | 0 | **A-Law** |
| 0 | 1 | **u-Law** |
| 1 | 0 | **Linear** |
| 1 | 1 | **Reserved** |

#### 14.1.2. RECEIVE/TRANSMIT TIMESLOT (WIDEBAND AND NARROWBAND)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | Async |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **0x01** | **TTLNB** | TTSNB[7:0] | | | | | | | | 0x00 | |
| **0x02** | **RTLNB** | RTSNB[7:0] | | | | | | | | 0x00 | |
| **0x03** | **TCH** | RTSWB[9:8] | | TTSWB[9:8] | | RTSNB[9:8] | | TTSNB[9:8] | | 0x50 | |

Transmit and receive timeslot are expressed in number of BCLK cycles in a 10-bit word. For Narrowband, Transmit Timeslot Start, TTSNB[9:0], determines the start point for the timeslot on the PCM interface for data in the transmit direction and the Receive Timeslot Start, RTSNB[9:0], determines the start point for the timeslot on the PCM interface for data in the receive direction. Timeslot Channel High, TCH address (0x03) bits are the two most significant bits of the 10-bit word for both transmit and receive timeslot, TCH:RTSWB[9:8] and TCH:TTSWB[9:8] for Wideband and TCH:RTSNB[9:8] and TCH:TTSNB[9:8] for Narrowband.

### 14.1.3. PLL STATUS REGISTER

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | **Async (D7, D5)** |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **0x04** | **PLLS** | PLLCM | CLK1544EN | FSRATE | BCFS[3:0] (RO) | | | | PL (RO) | 0xD9 | |

PL[0] and BCFS[4:1] are status bits which means they are **READ ONLY** bits in this register. Any write to these bits will be ignored. FSRATE[5], CLK1544EN[6], and PLLM[7] are READ/WRITE bits.

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | PLL Lock Status (RO) | **PL** | Not Locked | Locked |
| 5 | Frame Sync Rate | **FSRATE** | 8kHz | 16kHz |
| 6 | Enable clock 1.544MHz | **CLK1544EN** | Disabled | Enabled |

With an external 8 kHz Frame Sync set (PCMFS:FSS=0), PLL Bit Clock Frequency Status, BCFS[3:0] bits will show the value of BCLK according to the following table. Not all clocks are supported by 16KHz frame sync [ * ].

| Bit Clock Frequency | | | | |
|---|---|---|---|---|
| **BCFS[3]** | **BCFS[2]** | **BCFS[1]** | **BCFS[0]** | **BCLK(kHz)** |
| 0 | 0 | 0 | 0 | 256 |
| 0 | 0 | 0 | 1 | 512 |
| 0 | 0 | 1 | 0 | 768 |
| 0 | 0 | 1 | 1 | 1000* |
| 0 | 1 | 0 | 0 | 1024 |
| 0 | 1 | 0 | 1 | 1152 |
| 0 | 1 | 1 | 0 | 1536 |
| 0 | 1 | 1 | 1 | 1544* |
| 1 | 0 | 0 | 0 | 2000 |
| 1 | 0 | 0 | 1 | 2048 |
| 1 | 0 | 1 | 0 | 4000 |
| 1 | 0 | 1 | 1 | 4096 |
| 1 | 1 | 0 | 0 | 8000 |
| 1 | 1 | 0 | 1 | 8192 |
| 1 | 1 | 1 | 0 | NA |
| 1 | 1 | 1 | 1 | |

| DC/DC CLK Mode | | DC-DC Clock Type |
|---|---|---|
| **PLLCM[7]** | **PON:CDCC[7] (Addr – 0x22)** | |
| 0 | 0 | $\frac{1}{13.824\text{MHz}}$ |
| 0 | 1 | $\frac{1}{27.648\text{MHz}}$ |
| 1 | 0 | |
| 1 | 1 | |

### 14.1.4. PCM FREQUENCY SETTING REGISTER

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | Async (D7- D1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **0x05** | **PCMFS** | BCF[3:0] | | | | IFST | FSS | WBEN | SRES | 0x00 | |

The following table explains the PCM Frequency Setting register bits.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Soft Reset | **SRES** | Disable | Enable |
| 1 | Band Select | **WBEN** | FS = 8kHz (Narrowband) | FS = 16kHz (Wideband) |
| 2 | Frame Sync Source | **FSS** | External | Internal |
| 3 | Internal Frame Sync Type | **IFST** | Short (fixed width 1 BCLK) | Long (fixed width 8 BCLK) |

When an internal 8 kHz Frame Sync is used (PCMFS:FSS=1) these bits should be programmed with the value of BCLK Frequency, BCFS[3:0], according to the following table.

| Bit Clock Frequency | | | | |
|---|---|---|---|---|
| **BCF [4]** | **BCF [3]** | **BCF [2]** | **BCF [1]** | **BCLK (Hz)** |
| 0 | 0 | 0 | 0 | 256 |
| 0 | 0 | 0 | 1 | 512 |
| 0 | 0 | 1 | 0 | 768 |
| 0 | 0 | 1 | 1 | 1000 |
| 0 | 1 | 0 | 0 | 1024 |
| 0 | 1 | 0 | 1 | 1152 |
| 0 | 1 | 1 | 0 | 1536 |
| 0 | 1 | 1 | 1 | 1544 |
| 1 | 0 | 0 | 0 | 2000 |
| 1 | 0 | 0 | 1 | 2048 |
| 1 | 0 | 1 | 0 | 4000 |
| 1 | 0 | 1 | 1 | 4096 |
| 1 | 1 | 0 | 0 | 8000 |
| 1 | 1 | 0 | 1 | 8192 |
| 1 | 1 | 1 | 0 | NA |
| 1 | 1 | 1 | 1 | |

### 14.1.5. SILICON VERSION ID REGISTER (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x06** | **SIREV** | SIREV[7:0] | | | | | | | | 0xEF |

Silicon revision ID Register is a **READ ONLY** register.

### 14.1.6. DEVICE VERSION ID REGISTER (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x07** | **DVID** | VER[7:0] (RO) | | | | | | | | NA |

Device Version ID Register is a **READ ONLY** register.

| **Device** | VER[7:0] | Condition |
|---|---|---|
| **N681386** | 0x01 | |
| **N681387** | 0x01 | WBAND Pin = GND |
| **N681387** | 0x09 | WBAND Pin = VDD |

### 14.1.7. TIMESLOT (WIDEBAND)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **0x08** | **TTLWB** | TTSWB[7:0] | | | | | | | | 0xC0 | **Async** |
| **0x09** | **RTLWB** | RTSWB[7:0] | | | | | | | | 0xC0 | |

Transmit and receive timeslot are expressed in number of BCLK cycles in a 10-bit word. For Wideband, Transmit Timeslot Start, TTSWB[9:0], determines the start point for the timeslot on the PCM interface for data in the transmit direction and the Receive Timeslot Start, RTSWB[9:0], determines the start point for the timeslot on the PCM interface for data in the receive direction. The two most significant bits of the 10-bit word are located on register TCH address (0x03).

## 14.2. FSK REGISTERS

### 14.2.1. FSK CONTROL REGISTER

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x10** | **FSKC** | PE | PEN | PTYP | POL | TX | STOP | SPEC | EN | 0x00 |

The following table explains the FSK Control Register bits.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | FSK Encoder | **EN** | Disable | Enable |
| 1 | FSK Specification | **SPEC** | Bell 202 | ITU-T V.23 |
| 2 | Number of STOP bits | **STOP** | 1 Stop bit | 2 Stop bits |
| 3 | FSK Encoder start to transmit data from FSK FIFO | **TX** | Stop Transmission | Start Transmission |
| 4 | FSK bit stream polarity | **POL** | Non-inverted | Inverted |
| 5 | Parity Bit Type | **PTYP** | Even parity | Odd parity |
| 6 | Parity Bit Enable | **PEN** | Disable | Enable |
| 7 | FSK Package Format | **PE** | Disable | Enable |

FSK Package Format automatically amends a ‘start bit’ (Space) to the head of the FSK transmit data and one or two ‘stop bits’ (Mark) to the end, depending on programming of FSKC:STOP. “Res” in the register map means Reserved.

| | **Bell 202** | **ITU-T V.23** |
|---|---|---|
| **Mark ‘1’** | 1200 Hz | 1300 Hz |
| **Space ‘0’** | 2200 Hz | 2100 Hz |

### 14.2.2. FSK TRANSMIT REGISTER

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x11** | **FSKTD** | FSK[7:0] | | | | | | | | 0x00 |

FSK Transmit Register, FSK[7:0], is a WRITE ONLY register. Data written to this register will be placed into the Internal FIFO for transmission. Note: Reading this register will always give 0x00 as data.

### 14.2.3. FSK STATUS REGISTER (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x12** | **FSKS** | *RES* | | | | | FF (RO) | *RES* | FEP (RO) | 0x03 |

"*RES*" in the register map means reserved bit(s).

FSK Status Register is a **READ ONLY** register. The following table explains the FSK Status Register bits.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | FSK FIFO Empty Pending | **FEP** | FSK FIFO not empty (Last set of bit stream finished transmitting) | FSK FIFO is empty |
| 2 | FSK FIFO Full | **FF** | FSK FIFO not Full | FIFO Full |

### 14.2.4. FSK LCR REGISTER

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x13** | **FSKLCR** | *RES* | | | | GAIN[3:0] | | | | 0x00 |

"*RES*" in the register map means reserved bit(s).

The gain level is specified in linear values and referenced to the maximum linear PCM level (+3.14 dBm0). The following table contains the adjusted levels and the attenuated value of the correspondent maximum PCM level.

| FSK Encoder output signal level | | | | Attenuation to max PCM level |
|---|---|---|---|---|
| **GAIN3** | **GAIN2** | **GAIN1** | **GAIN0** | |
| 0 | 0 | 0 | 0 | -∞ |
| 0 | 0 | 0 | 1 | -23.512 |
| 0 | 0 | 1 | 0 | -17.499 |
| 0 | 0 | 1 | 1 | -13.978 |
| 0 | 1 | 0 | 0 | -11.48 |
| 0 | 1 | 0 | 1 | -9.542 |
| 0 | 1 | 1 | 0 | -7.956 |
| 0 | 1 | 1 | 1 | -6.617 |
| 1 | 0 | 0 | 0 | -5.458 |
| 1 | 0 | 0 | 1 | -4.434 |
| 1 | 0 | 1 | 0 | -3.52 |
| 1 | 0 | 1 | 1 | -2.692 |
| 1 | 1 | 0 | 0 | -1.937 |
| 1 | 1 | 0 | 1 | -1.242 |
| 1 | 1 | 1 | 0 | -0.599 |
| 1 | 1 | 1 | 1 | 0 |

### 14.2.5. FSK TCR REGISTER

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x14 | FSKTCR | *RES* | | | | | | FSKR | FMT | 0x00 |

"*RES*" in the register map means reserved bit(s).

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Fast Mode | **FMT** | Disabled | Enabled |
| 1 | FSK Route | **FSKR** | Output | Not Output |

### 14.3. DIAGNOSTIC REGISTERS

#### 14.3.1. DIAGNOSTIC CONTROL 0

| Addr | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x15** | **DIAGCTRL0** | FIFOIP | DCREN | ACLPFEN | DCLPFEN | FIFOEN | SIGNED | RES | DIAGEN | 0x00 |

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Enable Diagnostic Mode | **DIAGEN** | Disabled | Enabled |
| 2 | Converts unsigned Source Register data to signed data | **SIGNED** | Disabled | Enabled |
| 3 | Enable DIAGFIFO0 / DIAGFIFO1 FIFO Structure. | **FIFOEN** | Disabled | Enabled |
| 4 | Enable Low pass filter in the DC path.<br>The DC Path LPF utilizes the Loop Closure Detect LPF and is programmed in LCDCL: LCDC[11:0]. | **DCLPFEN** | Disabled | Enabled |
| 5 | Enable Low pass filter in the AC path.<br>The AC Path LPF utilizes the AC Ring Trip Detect LPF and is programmed in RTDFCLD:ARTDFC[11:0]. | **ACLPFEN** | Disabled | Enabled |
| 6 | Enable DC Removal function in the AC path | **DCREN** | Disabled | Enabled |
| 7 | Determines Data routed to DIAGFIFO0 / DIAGFIFO1 FIFO Structure DIAGCTRL0:DIAGEN must be set.<br>NOTE: DIAGCTRL0:FIFOEN will be turned on automatically if ADC PCM Data is selected. | **FIFOIP** | DC/AC Diagnostics Output | ADC PCM data |

#### 14.3.2. DIAGNOSTIC CONTROL 1

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x16** | **DIAGCTRL1** | TRACNEG | ACSEL[2:0] | | | TRDCNEG | DCSEL[2:0] | | | 0x00 |

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 3 | VTIP, VRING and SCM are forced to negative values when selected on the DC diagnostics path. | **TRDCNEG** | Disabled | Enabled |
| 7 | VTIP, VRING and SCM are forced to negative values when selected on the AC diagnostics path. | **TRACNEG** | Disabled | Enabled |

NOTE: Some diagnostic operations required signed operation, for example: DC removal.

ACSEL[6:4]: Select source register for the AC path diagnostics

DCSEL[2:0]: Select source register for the DC path diagnostics

| Select AC/DC source for Diagnostics | | | |
|---|---|---|---|
| **ACSEL2**<br>**DCSEL2** | **ACSEL1**<br>**DCSEL1** | **ACSEL0**<br>**DCSEL0** | **Source Register** |
| 0 | 0 | 0 | VTIP |
| 0 | 0 | 1 | VRING |
| 0 | 1 | 0 | LPV |
| 0 | 1 | 1 | SCM |
| 1 | 0 | 0 | TIPI |
| 1 | 0 | 1 | RINGI |
| 1 | 1 | 0 | LPI |
| 1 | 1 | 1 | LGI |

### 14.3.3. DIAGNOSTIC CONTROL 2, 3, 4. AND 5

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x17** | **DIAGCTRL2** | VHI[7:0] | | | | | | | | 0x00 |
| **0x18** | **DIAGCTRL3** | *RES* | SELT[2:0] | | | VHI[11:8] | | | | 0x00 |
| **0x19** | **DIAGCTRL4** | VLO[7:0] | | | | | | | | 0x00 |
| **0x1A** | **DIAGCTRL5** | DCRDC | DCRAC | DCRRC | *RES* | VLO[11:8] | | | | 0x00 |

| Select MADC source for timing measurement. | | | |
|---|---|---|---|
| **SELT2** | **SELT1** | **SELT0** | **Source Register** |
| 0 | 0 | 0 | VTIP |
| 0 | 0 | 1 | VRING |
| 0 | 1 | 0 | LPV |
| 0 | 1 | 1 | SCM |
| 1 | 0 | 0 | TIPI |
| 1 | 0 | 1 | RINGI |
| 1 | 1 | 0 | LPI |
| 1 | 1 | 1 | LGI |

VHI[11:0]: Determines $V_{HI}$ for DIACNTRL:TIMER[12:0] measurement.

Range, Step Size and number of valid bits same as Source Register determined by SELT.

VLO[11:0]: Determines $V_{LO}$ for DIACNTRL:TIMER[12:0] measurement.

Range, Step Size and number of valid bits same as Source Register determined by SELT.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | 0 | 1 |
| 5 | DC Removal RC Time Constant | **DCRRC** | 1.25/64ms | 1.25/32ms |
| 6 | DC Removal Accelerated Convergence. | **DCRAC** | Disable | Enable |
| 7 | Enable DC Removal output to DC Path LPF in addition to the normal connection to the AC Path LPF<br>DIACNTRL0:DCREN must be set. | **DCRDC** | Disable | Enable |

Notes:

- When enabled DC Removal is able to estimate the DC level of a selected source data and pass an AC only signal to the AC Path LPF.
- When DC Removal is enabled both DIAGCTRL5:TRDCNEG and DIAGCTRL5:TRACNEG need to be turned on if VTIP or VRING or SCM are selected as the source register.

### 14.3.4. DIAGNOSTIC CONTROL 6 AND 7 (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x1B** | **DIAGCTRL6** | TIMER[7:0] (RO) | | | | | | | | 0x00 |
| **0x1C** | **DIAGCTRL7** | TMREN | *RES* | | TIMER[12:8] (RO) | | | | | |

TIMER[12:0] are status bits which means they are **READ ONLY** bits in this register. Any write to these bits will be ignored. TMREN[5] is READ/WRITE bit.

| Bit(s) Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | 0 | 1 |
| 7 | Capacitor Charging Timer | TMREN | Reset Timer - It will increase by at the rate of 800hz when the monitored source is between VLO and VHI. | The timer will accumulate the time when the voltage of the selected source (by SELT) falls between VLO and VHI. |

| | Capacitor Charging Timer | | |
|---|---|---|---|
| | **TMREN[7] (0x1C)** | | |
| | Minimum | Maximum | Increment |
| **Range** | 0 ms | 10.24 s | 1.25 ms |

### 14.3.5. DIAGNOSTIC CONTROL 8 (READ ONLY)

<table>
<tr><th>Addr.</th><th>Name</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td rowspan="4"><b>0x1D</b></td><td rowspan="4"><b>DIAGCTRL8</b></td><td colspan="8">DCDP[7:0] (RO)</td><td rowspan="2">00</td></tr>
<tr><td colspan="4"><i>RES</i></td><td colspan="4">DCDP[11:8] (RO)</td></tr>
<tr><td colspan="8">ACDP[7:0] (RO)</td><td rowspan="2">00</td></tr>
<tr><td colspan="4"><i>RES</i></td><td colspan="4">ACDP[11:8] (RO)</td></tr>
</table>

DCDP[11:0]: DC Diagnostic Path Output

ACDP[11:0]: AC Diagnostic Path Output

NOTE: This register is structured to be read in 4 byte burst

### 14.3.6. DIAGNOSTIC FIFO 0 AND FIFO1 (READ ONLY)

<table>
<tr><th>Addr.</th><th>Name</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td rowspan="4"><b>0x1E</b></td><td rowspan="4"><b>DIAGFIFO0</b></td><td colspan="8">FIFO0[7:0] (RO)</td><td rowspan="2">00</td></tr>
<tr><td colspan="8">FIFO0[15:8] (RO)</td></tr>
<tr><td colspan="8">FIFO0[23:16] (RO)</td><td rowspan="2">00</td></tr>
<tr><td colspan="8">FIFO0[31:24] (RO)</td></tr>
<tr><td rowspan="4"><b>0x1F</b></td><td rowspan="4"><b>DIAGFIFO1</b></td><td colspan="8">FIFO1[7:0] (RO)</td><td rowspan="2">00</td></tr>
<tr><td colspan="8">FIFO1[15:8] (RO)</td></tr>
<tr><td colspan="8">FIFO1[23:16] (RO)</td><td rowspan="2">00</td></tr>
<tr><td colspan="8">FIFO1[31:24] (RO)</td></tr>
</table>

DIAGFIFO0 and DIAGFIFO1 are structured as Dual FIFO Structures. Each FIFO has 16 entries, each entry structured as a 4 byte structure illustrated above. When one FIFO is full an interrupt is generated and diagnostic data is collected in the alternative FIFO. In Diagnostic Mode (DIAGCTRL0:DIAGEN) DIAGFIFO0 uses the Ring Trip Detect Interrupt mechanism and DIAGFIFO1 uses the Loop Closure Detect Interrupt mechanism.

When DIAGCTRL0:FOFIP[7] is set to 0, DIAGFIFO0 and DIAGFIFO1 are used to store DC Diagnostic Path and AC Path Output Data

- FIFOn[15:0], n=0,1 contains DCDP[11:0]: DC Diagnostic Path Output in the lower 12 bits
  FIFOn[31:16], n=0,1 contains ACDP[11:0]: AC Diagnostic Path Output in the lower 12 bits
- NOTE: DC Diagnostic Path and AC Path Data is input to each FIFO at 800 Hz.

When DIAGCTRL0:FOFIP[7] is enabled DIAGFIFO0 and DIAGFIFO1 are used to store ADC PCM Data

- FIFOn[15:0], n=0,1 contains 16-bit ADC PCM data
  FIFOn[31:16], n=0,1 is not output
  In this case the Maximum burst read is 32 bytes per FIFO.
- NOTE: PCM Data is input to each FIFO at the sampling frequency (Wideband or Narrowband).

## 14.4. SYSTEM REGISTERS

### 14.4.1. PCM HPF (HIGH PASS FILTER)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x20** | **PHF** | DACLP | *RES* | DACFF[1:0] | | ADCFF[1:0] | | ADCHP | DACHP | 0x80 |

"*RES*" in the register map means reserved bit(s).

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | PCM Transmit HPF (DAC) | **DACHP** | Enable | Disable |
| 1 | PCM Receive HPF (ADC) | **ADCHP** | Enable | Disable |
| 7 | LPF for Wideband (DAC) | **DACLP** | Disable | Enable |

| High Pass Filter Select DAC | | |
|---|---|---|
| DACFF [5] | DACFF [4] | DAC HPF Select (Hz) |
| 0 | 0 | 20 |
| 0 | 1 | 40 |
| 1 | 0 | 80 |
| 1 | 1 | 160 |

| High Pass Filter Select ADC | | |
|---|---|---|
| ADCFF [3] | ADCFF [2] | ADC HPF Select (Hz) |
| 0 | 0 | 20 |
| 0 | 1 | 40 |
| 1 | 0 | 80 |
| 1 | 1 | 160 |

High pass filter cutoff is only programmable in the Wideband mode.

### 14.4.2. LOOP BACK CONTROL REGISTER

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x21** | **LB** | DACPOL | ADCPOL | *RES* | ALP2 | ALP1 | DLP3 | DLP2 | DLP1 | 0x00 |

"*RES*" in the register map means reserved bit(s).

The following table explains the Loop Back Control Register bits.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Digital loop back (D/A to A/D) | **DLP1** | Disable | Enable |
| 1 | Digital loop back (LP interpolation filter to LP decimation filter) | **DLP2** | Disable | Enable |
| 2 | Digital loop back (A/u law expander to A/u law compander) | **DLP3** | Disable | Enable |
| 3 | Analog Loop back 1 | **ALP1** | Disable | Enable |
| 4 | Analog Loop back 2 | **ALP2** | Disable | Enable |
| 6 | Invert ADC input Polarity | **ADCPOL** | Disable | Enable |
| 7 | Invert DAC Output Polarity | **DACPOL** | Disable | Enable |

### 14.4.3. POWER ON

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x22** | **PON** | CDCC | *RES* | | | | DACPP | ADCPP | DCC | 0x01 |

"*RES*" in the register map means reserved bit(s). The following table explains the Loop Back Control Register bits.

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | DC/DC Power Control Circuitry | **DCC** | DCDC On | DCDC OFF |
| 1 | A/D Power Path | **ADCPP** | Disable | Enable |
| 2 | DAC Power Path | **DACPP** | Disable | Enable |

| DC/DC CLK Mode | | DC-DC Clock Type |
|---|---|---|
| **PLLS:PLLCM[7] (Addr: 0x04)** | **CDCC[7]** | |
| 0 | 0 | $\frac{1}{13.824MHz}$ |
| 0 | 1 | $\frac{1}{27.648MHz}$ |
| 1 | 0 | |
| 1 | 1 | |

This table gives the PLL Period.

### 14.4.4. LINEFEED TRIM

| Addr | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x23** | **ILIM** | ZCPINV | ZCPEN | RNGGAIN | RIPS | TINS | ILMGAIN | CALTR1 | CALTR0 | 0x00 |

| CALIBRATION STATE CURRENT ADJUST | | |
|---|---|---|
| **CALTR1** | **CALTR0** | **Current** |
| 0 | 0 | 20mA |
| 0 | 1 | 19.6mA |
| 1 | 0 | 19.4mA |
| 1 | 1 | 20.4mA |

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 2 | Ring Limiting Gain Adjust strength of Ring limiting Impacts noise | **ILIMGAIN** | Default | 2 x default |
| 3 | Idle State Battery Current | **TINS** | Default current | Low current |
| 4 | Idle State Battery Current Stops RIP in idle for lower power | **RIPS** | Default current | Low current |
| 5 | Increase Ring feedback gain in idle and Ring state for more accuracy | **RNGGAIN** | Default | High gain |
| 6 | Line Capacitor Compensation | **ZCPEN** | Disabled | Enabled |
| 7 | Line Capacitor Compensation | **ZCPINV** | Subtract | Add |

## 14.5. INTERRUPT REGISTERS

### 14.5.1. INTERRUPT VECTOR LOW (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x24** | **INTV** | *RES* | | | | | IR3C1 (RO) | IR2C1 (RO) | IR1C1 (RO) | 0x00 |

"*RES*" in the register map means reserved bit(s).

Interrupt Vector Register is a **READ ONLY** register. Each bit in this register will be cleared when there are no pending interrupts reported in the corresponding interrupt status registers.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Interrupt Vector 1 Low | **IR1C1** | No INT | INT1 |
| 1 | Interrupt Vector 2 Low | **IR2C1** | No INT | INT2 |
| 2 | Interrupt Vector 3 Low | **IR3C1** | No INT | INT3 |

### 14.5.2. INTERRUPT STATUS REGISTER 1

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x26** | **INT1** | PAT3 | PAR3 | PAT1 | PAR1 | PAR2 | PAT2 | LC | RT | 0x00 |

This register displays all the Power Alarm and the Loop Closure interrupt of the device. A pending interrupt is represented by a HIGH "1" in the respective bit. Writing 1 to that respective bit clears the pending interrupt.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | RING Trip | **RT** | No INT | INT |
| 1 | Loop Closure | **LC** | No INT | INT |
| 2 | Power Alarm QR2 | **PAT2** | No INT | INT |
| 3 | Power Alarm QT2 | **PAR2** | No INT | INT |
| 4 | Power Alarm QT1 | **PAR1** | No INT | INT |
| 5 | Power Alarm QR1 | **PAT1** | No INT | INT |
| 6 | Power Alarm QR3 | **PAR3** | No INT | INT |
| 7 | Power Alarm QT3 | **PAT3** | No INT | INT |

### 14.5.3. INTERRUPT ENABLE REGISTER 1

| Addr | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x27** | **IE1** | PAT3E | PAR3E | PAT1E | PAR1E | PAR2E | PAT2E | LCE | RTE | 0x00 |

This register enables all the Power Alarm and the Loop Closure interrupt of the device. An interrupt can be enabled by writing a HIGH "1" in the respective interrupt bit.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | 0 | 1 |
| 0 | RING Trip | **RTE** | Masked | Enabled |
| 1 | Loop Closure | **LCE** | Masked | Enabled |
| 2 | Power Alarm QR2 | **PAT2E** | Masked | Enabled |
| 3 | Power Alarm QT2 | **PAR2E** | Masked | Enabled |
| 4 | Power Alarm QT1 | **PAR1E** | Masked | Enabled |
| 5 | Power Alarm QR1 | **PAT1E** | Masked | Enabled |
| 6 | Power Alarm QR3 | **PAR3E** | Masked | Enabled |
| 7 | Power Alarm QT3 | **PAT3E** | Masked | Enabled |

### 14.5.4. INTERRUPT STATUS REGISTER 2

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x28** | **INT2** | FSKI | DTMFI | RI | RA | O2I | O2A | O1I | O1A | 0x00 |

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | 0 | 1 |
| 0 | Oscillator 1 Active Timer | **O1A** | No INT | INT Pending |
| 1 | Oscillator 1 Inactive Timer | **O1I** | No INT | INT Pending |
| 2 | Oscillator 2 Active Timer | **O2A** | No INT | INT Pending |
| 3 | Oscillator 2 Inactive Timer | **O2I** | No INT | INT Pending |
| 4 | Ringing Active Timer | **RA** | No INT | INT Pending |
| 5 | Ringing Inactive Timer | **RI** | No INT | INT Pending |
| 6 | DTMF Initialize | **DTMFI** | No INT | INT Pending |
| 7 | FSK Interrupt occurs when the FSK FIFO is empty | **FSKI** | No INT | INT Pending |

### 14.5.5. INTERRUPT ENABLE REGISTER 2

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x29** | **IE2** | FSKIE | DTMFIE | RIE | RAE | O2IE | O2AE | O1IE | O1AE | 0x00 |

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Oscillator 1 Active Timer | **O1AE** | Masked | Enabled |
| 1 | Oscillator 1 Inactive Timer | **O1IE** | Masked | Enabled |
| 2 | Oscillator 2 Active Timer | **O2AE** | Masked | Enabled |
| 3 | Oscillator 2 Inactive Timer | **O2IE** | Masked | Enabled |
| 4 | Ringing Active Timer | **RAE** | Masked | Enabled |
| 5 | Ringing Inactive Timer | **RIE** | Masked | Enabled |
| 6 | DTMF Inactive Timer | **DTMFIE** | Masked | Enabled |
| 7 | FSK Enable | **FSKIE** | Masked | Enabled |

### 14.5.6. INTERRUPT STATUS REGISTER 3

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x2A** | **INT3** | *RES* | | | | GKDI | *RES* | | TMP | 0x00 |

"*RES*" in the register map means reserved bit(s).

This register displays the status of the dice Temperature interrupt of the device. A pending interrupt is represented by a HIGH "1" in the respective bit. Writing 1 to that respective bit clears the pending interrupt.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Die Temperature Interrupt | **TMP** | No INT | INT Pending |
| 3 | Ground Key Detection Interrupt | **GKDI** | No INT | INT Pending |

### 14.5.7. INTERRUPT ENABLE REGISTER 3

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x2B** | **IE3** | *RES* | | | | GKDIE | *RES* | | TMPE | **0x00** |

"*RES*" in the register map means reserved bit(s).

This register enables the dice Temperature interrupt of the device. An interrupt can be enabled by writing a HIGH "1" in the respective interrupt bit. The following table explains the Interrupt Enable Register 1 bits.

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Temperature Interrupt Enable | **TMPE** | Masked | Enabled |
| 3 | Ground Key Detection Interrupt Enable | **GKDIE** | Masked | Enabled |

### 14.6. DTMF DETECTION REGISTER

#### 14.6.1. DTMF CONTROL 1

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x30** | **DTMFC1** | DTMFEN | ADCOSEL | DTMFFDEV | | DTMFTC | | | | **0x00** |

ADC output is the signal from ADC coming to DTMF decode. Therefore, the ADC Select bit select either the ADC or PCM input to the DTMF decode. When DTMFTC[3:0] bits are set to larger values, DTMF detector needs more time to decode the DTMF signal but the numerical precision is greater.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 6 | ADC Output Select | **ADCOSEL** | ADC output comes from ADC.<br>(Receive path) | ADC output comes from PCM.<br>(Transmit path) |
| 7 | DTMF Enable | **DTMFEN** | Disabled | Enabled |

| DTMF Frequency Deviation | | |
|---|---|---|
| **DTMFFDEV[5]** | **DTMFFDEV[4]** | **Deviation (%)** |
| 0 | 0 | 1.5 |
| 0 | 1 | 2.5 |
| 1 | 0 | 3.0 |
| 1 | 1 | 3.5 |

| **Time constant used for DTMF frequency estimation** | | | | |
|---|---|---|---|---|
| **DTMFTC3** | **DTMFTC2** | **DTMFTC1** | **DTMFTC0** | **Time Constant** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |

| Time constant used for DTMF frequency estimation | | | | |
|---|---|---|---|---|
| **DTMFTC3** | **DTMFTC2** | **DTMFTC1** | **DTMFTC0** | **Time Constant** |
| 1 | 0 | 1 | 0 | 10 |
| 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 0 | 0 | 12 |
| 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 15 |

### 14.6.2. DTMF CONTROL 2

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x31** | **DTMFCTRL2** | *RES* | | | | | | | DTMFCLR | **0x00** |

"*RES*" in the register map means reserved bit(s).

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | DTMF Clear previous received data. | **DTMFCLR** | Default | Clear |

### 14.6.3. DTMF CONTROL 3

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x32** | **DTMFCTRL3** | *RES* | | | | DTMFRCVDT | | | | **0x00** |

"*RES*" in the register map means reserved bit(s).

| | | Column frequency | | | |
|---|---|---|---|---|---|
| | | 1209 Hz | 1336 Hz | 1477 Hz | 1633 Hz |
| Row Frequency | 697 Hz | 1 | 2 | 3 | A |
| | | 0x01 hex | 0x02 hex | 0x03 hex | 0x0D hex |
| | 770 Hz | 4 | 5 | 6 | B |
| | | 0x04 hex | 0x05 hex | 0x06 hex | 0x0E hex |
| | 852 Hz | 7 | 8 | 9 | C |
| | | 0x07 hex | 0x08 hex | 0x09 hex | 0x0F hex |
| | 941 Hz | * | 0 | # | D |
| | | 0x0B hex | 0x0A hex | 0x0C hex | 0x00 hex |

### 14.6.4. DTMF STATUS (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x33** | **DTMFST** | *RES* | | | | | | | DTMFEMT<br>(RO) | **0x01** |

"*RES*" in the register map means reserved bit(s). It is a **Read ONLY** bit

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | DTMF buffer is empty | **DTMFEMT** | Pending Data | Buffer is Empty |

### 14.6.5. DTMF THRESHOLD

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x34** | **DTMFTHRH** | DTMFTHR[15:8] | | | | | | | | **0xE4** |
| **0x35** | **DTMFTHRL** | DTMFTHR[7:0] | | | | | | | | **0xE5** |

This is the signal level threshold which must be present to detect a DTMF tone.

### 14.6.6. DTMF PRESENT DETECT TIME

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x36** | **DTMFPDT** | DTMFPDT[7:0] | | | | | | | | **0x00** |

| | **DTMF PRESENT DETECT TIME** | | |
|---|---|---|---|
| | The time for which a tone must be present to be qualified as a valid DTMF tone | | |
| | Minimum | Maximum | Increment |
| **Range** | 0 ms | 127 ms | 0.5 ms |

### 14.6.7. DTMF ABSENT DETECT TIME

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x37** | **DTMFADT** | DTMFADT[7:0] | | | | | | | | **0x00** |

| | **DTMF ABSENT DETECT TIME** | | |
|---|---|---|---|
| | The time for which a tone must be absent before a signal is considered a new DTMF tone | | |
| | Minimum | Maximum | Increment |
| **Range** | 0 ms | 127 ms | 0.5 ms |

### 14.6.8. DTMF ACCEPT TIME

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x38** | **DTMFACT** | DTMFACT[7:0] | | | | | | | | **0x00** |

| | **DTMF ACCEPT TIME** | | |
|---|---|---|---|
| | The time for which a tone must be stable to be qualified as a correct tone | | |
| | Minimum | Maximum | Increment |
| **Range** | 0 ms | 127 ms | 0.5 ms |

This guard time improves detection performance by rejecting detected signals with insufficient duration and by masking momentary detection dropout.

### 14.6.9. DTMF RECEIVE DATA STATUS

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x3A** | **DTMFRDT** | DTMFRDY | DTMFST | *RES* | | DTMFRDT[3:0] | | | | **0x00** |

"*RES*" in the register map means reserved bit(s).

DTMF Detector received data, DTMFRDT[3:0]. This data is valid when DTMF Ready, DTMFRDY[7], is active.

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 6 | DTMF State (indicates whether a valid DTMF tone is currently being detected and DTMF Present Time DTMFPDT[7:0], is qualified.) | **DTMFST** | Data Not Valid | Data Valid |
| 7 | DTMF Ready (indicates that a valid DTMF tone has been present for required DTMF Hold Time (ACCT) | **DTMFRDY** | Data Not Ready | Data Ready |

| | | Column frequency | | | |
|---|---|---|---|---|---|
| | | 1209 Hz | 1336 Hz | 1477 Hz | 1633 Hz |
| Row Frequency | 697 Hz | 1 | 2 | 3 | A |
| | | 0x01 hex | 0x02 hex | 0x03 hex | 0x0D hex |
| | 770 Hz | 4 | 5 | 6 | B |
| | | 0x04 hex | 0x05 hex | 0x06 hex | 0x0E hex |
| | 852 Hz | 7 | 8 | 9 | C |
| | | 0x07 hex | 0x08 hex | 0x09 hex | 0x0F hex |
| | 941 Hz | * | 0 | # | D |
| | | 0x0B hex | 0x0A hex | 0x0C hex | 0x00 hex |

### 14.6.10. DTMF ROW FREQUENCY

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x3B** | **DTMFRFH** | DTMFRF[15:8] | | | | | | | | **0x00** |
| **0x3C** | **DTMFRFL** | DTMFRF[7:0] | | | | | | | | **0x00** |

These two bytes are for debug mode, and display the DTMF Row frequency directly.

- DTMFRF[15:3] is the integer part of the DTMF Row frequency,
- DTMFRF[2:0] is the decimal fraction part of the DTMF Row frequency (13.3 format).

### 14.6.11. 14/15 DTMF COLUMN FREQUENCY

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x3D** | **DTMFCFH** | DTMFCF[15:8] | | | | | | | | **0x00** |
| **0x3E** | **DTMFCFL** | DTMFCF[7:0] | | | | | | | | **0x00** |

These two bytes are for debug mode, and display the DTMF Column frequency directly.

- DTMFCF[15:3] is the integer part of the DTMF Column frequency,
- DTMFCF[2:0] is the decimal fraction part of the DTMF Column frequency (13.3 format).

### 14.7. LINE REGISTERS

#### 14.7.1. AC PATH GAIN

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x40** | **APG** | RAMP | PREN | VOHZ | *RES* | ARX[1:0] | | ATX[1:0] | | 0x00 |

| Analog Receive Gain | | |
|---|---|---|
| **ARX1** | **ARX0** | **Gain (dB)** |
| 0 | 0 | 0 |
| 0 | 1 | - 3.5 |
| 1 | 0 | + 3.5 |
| 1 | 1 | Mute |

| Analog Transmit Gain | | |
|---|---|---|
| **ATX1** | **ATX0** | **Gain (dB)** |
| 0 | 0 | 0 |
| 0 | 1 | - 3.5 |
| 1 | 0 | + 3.5 |
| 1 | 1 | Mute |

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 5 | Wink function | **VOHZ** | Return to nominal $V_{RING}$ | Ramp towards 0 $V_{RING}$ |
| 6 | Soft Polarity Reversal | **PREN** | Disable | Enable |
| 7 | Soft Polarity Reversal ramp | **RAMP** | 1.484 V/125 µs | 2.968 V/125 µs |

#### 14.7.2. HYBRID BALANCE

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x41** | **HB** | DACG | ADCG | *RES* | | | AHYB[2:0] | | | 0x1B |

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 6 | Analog ADC Path Gain | **ADCG** | -6 dB | 0 dB |
| 7 | Analog DAC Path Gain | **DACG** | 0 dB | 6 dB |

| Audio Hybrid Balance Adjustment | | | |
|---|---|---|---|
| **AHYB2** | **AHYB1** | **AHYB0** | **Trans hybrid Gain** |
| 0 | 0 | 0 | +4.08 |
| 0 | 0 | 1 | +2.50 |
| 0 | 1 | 0 | +1.16 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | - 1.02 |
| 1 | 0 | 1 | - 1.94 |
| 1 | 1 | 0 | - 2.77 |
| 1 | 1 | 1 | Disable |

### 14.7.3. COMMON RINGING BIAS ADJUST DURING RINGING

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x42** | **VCMR** | *RES* | | VCMR[5:0] | | | | | | 0x00 |

"RES" in the register map means reserved bit(s).

The above register sets Common Ringing Bias Adjustment voltage during Ringing. To convert decimal value to hex value please refer to the beginning of this section (Register Description).

| | **COMMON RINGING BIAS ADJUST VOLTAGE DURING RINGING** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 V | –93.5 V | 1.484 V |

### 14.7.4. LINE AUTOMATIC MANUAL CONTROL

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x43** | **LAMC** | *RES* | | | | | PAA | RGA | LCDA | 0x07 |

"*RES*" in the register map means reserved bit(s).

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Loop Closure Detect Automatic | **LCDA** | Manual Mode | Automatic Control |
| 1 | RING Automatic | **RGA** | Manual Mode | Automatic RING Control |
| 2 | Power Alarm Automatic React<br>(Enters Open state automatically upon power alarm regardless of current state) | **PAA** | Manual Mode | Automatic Control |

In RING Automatic, LAMC:RGA[1] address (0x43), when entering Ringing state the RING Oscillator is automatically enabled. Both OSN:O2E[1] address (0xC0) and RMPC:R1EN[5] address (0xC1) are set automatically. Enter Active state from ringing state automatically upon RING Trip Detect. The RING Oscillators are automatically disabled. Forward or Reverse states determined primarily by OHV:SB[6] address (0x4C) Upon entering Loop Closure Detect Automatic LAMC:LCDA[0] address (0x43) the device will enter the Active state from Idle, TIP Open, RING Open and ON-HOOK Transmission states automatically upon Loop Closure Detect. Forward or Reverse states determined primarily by OHV:SB[6] address (0x4C).

### 14.7.5. LINEFEED STATUS

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x44** | **LS** | SLS[3:0] | | | | LS[3:0] | | | | 0x00 |

| **LineFeed Status** | | | | |
|---|---|---|---|---|
| LS3 | LS2 | LS1 | LS0 | State |
| 0 | 0 | 0 | 0 | Open |
| 0 | 0 | 0 | 1 | Forward Active |
| 0 | 0 | 1 | 0 | Forward ON-HOOK Transmission |
| 0 | 0 | 1 | 1 | TIP Open |
| 0 | 1 | 0 | 0 | Ringing |
| 0 | 1 | 0 | 1 | Reverse Active |
| 0 | 1 | 1 | 0 | Reverse ON-HOOK Transmission |
| 0 | 1 | 1 | 1 | RING Open |
| 1 | 0 | 0 | 1 | Forward Idle |
| 1 | 1 | 0 | 1 | Reverse Idle |
| 1 | 1 | 1 | 0 | Calibration Mode |

LS:LS[3:0] is the Linefeed Status Register bits which reflects the programmed linefeed state, not necessarily the actual linefeed state. See LS:SLS[3:0] definition. When automatic transitions occur LS:LS[3:0] will also update accordingly.

SLS[3:0] is the Shadow Linefeed Status Register bits which reflects the actual real-time linefeed state. Automatic operations may cause actual linefeed state to deviate from the state defined in LS:LS[3:0]. For example when LS:LS[3:0] is programmed for ‘Ringing’ state, LS:SLS[3:0] will only indicate ‘Ringing’ during the actual RING burst. During the RING cadence LS:SLS[3:0] will indicate ‘ON-HOOK Transmission’. This register has the same setting as the Linefeed Status Register bits.

### 14.7.6. LOOP CURRENT LIMIT

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x45** | **LCL** | LGCRT | LGCRR | LGCM[1:0] | | *RES* | ILM[2:0] | | | 0x00 |

“*RES*” in the register map means reserved bit(s). To convert Current Limit decimal value to hex value please refer to the beginning of this section (Register Description).

| | **CURRENT LIMIT [ILM[2:0]]** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 20 mA [0x00] | 41 mA [0x07] | 3 mA |

| LGCM1 | LGCM0 | Common Mode Correction |
|---|---|---|
| 0 | 0 | Open (none) |
| 0 | 1 | Small (one) |
| 1 | 0 | Medium (two) |
| 1 | 1 | Large (three) |

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | 0 | 1 |
| 6 | Series Resistor with CRn | **LGCRR** | OFF | ON |
| 7 | Series Resistor with CTn | **LGCRT** | OFF | ON |

### 14.7.7. RING TRIP DETECT STATUS/ LOOP CLOSURE STATUS (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x46** | **RTLC** | RTM | LCM | VBLC | RTDUD (RO) | RTDUA (RO) | LCDU (RO) | RTD (RO) | LCD (RO) | 0x00 |

"*RES*" in the register map means reserved bit(s).

RING Trip Detect Unfiltered Indicator (RTDUD) bit reflects the real-time output of RING trip detects circuit before debounce. Loop Closure Detect Unfiltered Indicator (LCDU) bit reflects the real-time output of Loop Closure Detect circuit before debounce**. Bits of register RTLC[7:5] are READ/WRITE but the bits RTLC[4:0] are READ ONLY**

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | 0 | 1 |
| 0 | Loop Closure Detect (filtered output) | **LCD** | LCD has not occurred | LCD has occurred |
| 1 | RING Trip Detect (filtered output) | **RTD** | RTD has not occurred | RTD has occurred |
| 2 | Loop Closure Detect Unfiltered | **LCDU** | Threshold not exceeded | Threshold exceeded |
| 3 | RING Trip Detect Unfiltered AC | **RTDUA** | Threshold not exceeded | Threshold exceeded |
| 4 | RING Trip Detect Unfiltered DC | **RTDUD** | Threshold not exceeded | Threshold exceeded |
| 5 | Voltage-Based Loop Closure | **VBLC** | LC determined by loop current | LC determined by Tip to RING voltage |
| 6 | Loop Closure Mask Counter | **LCM** | Disabled | Enabled |
| 7 | Ring Trip Mask Control | **RTM** | Disabled | Enabled |

### 14.7.8. LOOP CLOSURE DEBOUNCE

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x47** | **LCDB** | LCDI[7:0] | | | | | | | | 0x00 |

Loop Closure Detect Debounce Interval LCDI[7:0] is an 8-bit register which sets time interval (decimal value) in digital format. To convert decimal value to hex value please refer to the beginning of this section (Register Description).

| | **LOOP CLOSURE DEBOUNCE INTERVAL** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 msec | 159 msec | 1.25 msec |

### 14.7.9. RING TRIP DEBOUNCE INTERVAL

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x48** | **RTDBA** | ARTDI[7:0] | | | | | | | | 0x00 |

RING Trip Detect Debounce Interval ARTDI[6:0] is an 8-bit register which sets time interval (decimal value) in digital format. To convert decimal value to hex value please refer to the beginning of this section (Register Description).

| | **RING TRIP DEBOUNCE** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 msec | 159 msec | 1.25 msec |

### 14.7.10. PWM PERIOD

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x49** | **PWMT** | PT[7:0] | | | | | | | | 0xFF |

This register sets PWM period for the DC/DC converter. Use the following equation to calculate the period.

PWM Period = (PT[7:0] + 1) x PLL Period

The PWM period should be set to a value greater than the DC/DC Converter Minimum OFF Time

PWMT:PT[7:0] > DDCC:DCOFF[4:0]

The PLL Period (expressed in nsec) which is selected based on the setting of PON:CDCC[7] address (0x22) and whether the BCLK is binary or decimal.

### 14.7.11. DC/DC CONTROLLER CONTROL

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x4A** | **DDCC** | DCOFF[7:0] | | | | | | | | 0x76 |

This register sets DC/DC Converter Minimum OFF Time. Use the following equation to calculate the period. DCOFF[7:0] should be programmed to values ≥ 04 hex

TOFF = DCOFF[7:0] x PLL Period

The PLL Period (expressed in nsec) which is selected based on the setting of PON:CDCC[7] address (0x22) and whether the BCLK is binary or decimal.

### 14.7.12. ON-HOOK VOLTAGE

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x4C** | **OHV** | *RES* | SB | VOH[5:0] | | | | | | 0x20 |

"*RES*" in the register map means reserved bit(s).

| | **ON-HOOK VOLTAGE ($V_{TIP} – V_{RING}$) [VOH]** | | | |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | Default |
| **Range** | 0 V | - 93.5 V | 1.484 V | - 47.488 V |

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 6 | Determines polarity of Idle, Active, and On-hook transition states after automatic transitions | **SB** | Forward | Reverse |

### 14.7.13. GROUND MARGIN VOLTAGE

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x4D** | **GMV** | UBR | *RES* | VGM[5:0] | | | | | | 0x02 |

"*RES*" in the register map means reserved bit(s).

| | GROUND MARGIN VOLTAGE [VGM] | | | |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | Default |
| **Range** | 0 V | - 93.5 V | 1.484 V | -2.968 V |

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | 0 | 1 |
| 7 | Unbalanced Ringing | **UBR** | Balanced Ringing | Unbalanced Ringing |

### 14.7.14. HIGH BATTERY VOLTAGE

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x4E** | **VBHV** | XBATR | *RES* | VBATH[5:0] | | | | | | 0x32 |

"*RES*" in the register map means reserved bit(s).

| | HIGH BATTERY VOLTAGE [VBATH] | | | |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | Default |
| **Range** | 0 V | - 93.5 V | 1.484 V | - 74.2 V |

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | 0 | 1 |
| 7 | External Battery Enable | **XBATR** | Disabled | Enabled |

### 14.7.15. LOW BATTERY VOLTAGE

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x4F** | **VBLV** | *RES* | | VBATL[5:0] | | | | | | 0x10 |

"*RES*" in the register map means reserved bit(s).

| | LOW BATTERY VOLTAGE [VBATL] | | | |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | Default |
| **Range** | 0 V | - 93.5 V | 1.484 V | - 23.744 V |

### 14.7.16. LOOP CLOSURE DETECT/RING TRIP DETECT COEFFICIENT

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x50** | **LCDCL** | LCDC[7:0] | | | | | | | | 0x00 |
| **0x51** | **RTDFCLD** | ARTDFC[7:0] | | | | | | | | 0x00 |
| **0x52** | **DCHD** | ARTDFC[11:8] | | | | LCDC[11:8] | | | | 0x00 |

Loop Closure Detect Coefficient LCDC[11:0] is governed by the cutoff frequency $f_{LP}$

$$LCDC[11:0] = \left(1 - 2 * \pi * \left(\frac{f_{LP}}{800Hz}\right)\right) * 2^{12}$$

AC Ring Trip Detect Filter Coefficient ARTDFC[11:0] is governed by the cutoff frequency $f_{LP}$

$$ARTDFC[11:0] = \left(1 - 2 * \pi * \left(\frac{f_{LP}}{800Hz}\right)\right) * 2^{12}$$

### 14.7.17. LOOP CLOSURE DETECT THRESHOLD WITHOUT / WITH HYSTERESIS

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x53** | **LCT** | *RES* | | LCT[5:0] | | | | | | **0x00** |
| **0x54** | **LCTHY** | DBTR | LCHYEN | LCTOFF[5:0] | | | | | | **0x00** |

"*RES*" in the register map means reserved bit(s).

| Bit Location | Bit Description | Condition | | Bit Name | Range | Increment |
|---|---|---|---|---|---|---|
| **(0x53)<br>D0 - D5** | **Loop Closure Detect Threshold** | If hysteresis enabled (LCTHY:LCHYEN=1) LCT[5:0] only used to determine transitions from ON-HOOK to OFF-HOOK state | Current Based (RTLC:VBLC=0,) | **LCT** | 0 to 80 mA | 1.27 mA |
| | | | Voltage Based (RTLC:VBLC=1,) | | 0 to 93.5 V | 1.484 V |
| **(0x54)<br>D0 - D5** | **Loop Closure Detect Threshold with hysteresis** | Only valid if hysteresis enabled (LCTHY:LCHYEN=1) LCTOFF[5:0] only used to determine transitions from OFF-HOOK to ON-HOOK state | Current Based | **LCTOFF** | 0 to 80 mA | 1.27 mA |
| | | | Voltage Based (LCDB:VBLC=1) | | 0 to 93.5 V | 1.484 V |

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 6 | Loop Closure Hysteresis | **LCHYEN** | Disable | Enable |
| 7 | Dynamic Battery Target | **DBTR** | Disable | Enable |

### 14.7.18. RING TRIP DETECT THRESHOLD

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x55** | **RTTA** | *RES* | | ARTT[5:0] | | | | | | **0x00** |

| | **RING TRIP DETECT THRESHOLD [ARTT]** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 A | 80 mA | 1.27 mA |

### 14.7.19. OFFSET VOLTAGE

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x56** | **VOV** | *RES* | | | TR | VOV[3:0] | | | | **0x00** |

“*RES*” in the register map means reserved bit(s).

The Tracking Mode is enabled by set TR bit HIGH and disabled by setting it LOW.

| | **Offset Voltage between TIP and RING [VOV]** | | | |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | Default |
| **Range** | 0 V | 24 V | 1.484 V | 3.0 V |

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 4 | Tracking Mode | **TR** | $\lvert V_{BAT} \rvert$ will not go below $V_{BATL}$ | $V_{BAT}$ tracks $V_{RING}$ in constant current region |

### 14.7.20. DC/DC TIME ON

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x57** | **DCTON** | *RES* | | | TONDC[5:0] | | | | | **0x00** |

“*RES*” in the register map means reserved bit(s).

Minimum DCDC on time

### 14.7.21. DAC/ADC AUTOMUTE FUNCTION

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x5E** | **AUTOMT** | AMTEN | AMTSEL | AMTTHR | | | | | | **0x00** |

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 6 | Automute Select | AMTSEL | DAC data + ADC data | DAC data only |
| 7 | Automute Enable | AMTEN | Disabled | Enabled |

| Automute Threshold | |
|---|---|
| **Modes** | **AMTTHR[5:0]** |
| Linear | 0 |
| u-Law | 0 |
| A-law | 8 |

### 14.8. GROUND KEY DETECTION

#### 14.8.1. LINEFEED CONTROL

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x5F** | **XBTC** | *RES* | ASQH | CBP | XBEN | XTBOT1 | XTBOT0 | XTBAT[1:0] | | **0x00** |

"*RES*" in the register map means reserved bit(s).

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 2 | DC Bias Current OFF-Hook | **XTBOT0** | 8 mA | 4 mA |
| 3 | DC Bias Current On-Hook TR | **XTBOT1** | 4 mA | 8 mA |
| 4 | Ringer Bias Enable | **XBEN** | Disable | Enable |
| 5 | Capacitor Bypass | **CBP** | capacitors CP() and CM (C2) in circuit | Capacitors CT and CR bypassed |
| 6 | Audio Mute | **ASQH** | STIPAC and SRINGAC pins are not muted | STIPAC and SRINGAC pins are muted |

The DC bias current flows through external BJTs in the both On-Hook Transmission and in Active Off-Hook State. Increasing this value (External Transistor Bias Levels) increases the TIP to RING peak of the differential AC current.

| Current Limit adjustment | | |
|---|---|---|
| **XTBA1** | **XTBA0** | **DC Bias Current** |
| **0** | **0** | Nominal ILIM |
| **0** | **1** | +1 mA |
| **1** | **0** | +2 mA |
| **1** | **1** | -1 mA |

#### 14.8.2. GROUND KEY DETECT HIGH/LOW THRESHOLD

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x60** | **GKDH** | *RES* | HGKD[7:0] | | | | | | | 0x00 |
| **0x61** | **GKDL** | *RES* | LGKD[7:0] | | | | | | | 0x00 |

| | **GKD HIGH/LOW THRESHOLD** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 A | 80 mA | 1.27mA |

### 14.8.3. GROUND KEY DETECT DEBOUNCE TIME

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x62** | **GKDDT** | DTGKD[7:0] | | | | | | | | 0x00 |

| | **GKD DEBOUNCE TIME** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 msec | 320 msec | 1.25 msec |

### 14.8.4. GROUND KEY DETECT FILTER COEFFICIENT LOW/ HIGH

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x63** | **GKDFCL** | FCGKD[7:0] | | | | | | | | 0x00 |
| **0x64** | **GKDFCH** | GKDEN | *RES* | | | FCGKD[11:8] | | | | 0x00 |

Ground Key Detection Filter Coefficient governs the Ground Key Detect LPF cutoff frequency $f_{LP}$

$$FCGKD[11\ :0] = \left(1 - \ 2 * \pi * \left(\frac{f_{LP}}{800Hz}\right)\right) * 2^{12}$$

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 7 | Enable Ground Key detection | **GKDEN** | Disable | Enable |

### 14.8.5. DC RING TRIP DEBOUNCE FILTER COEFFICIENT LOW

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x65** | **RTDCDL** | DRTDFC[7:0] | | | | | | | | 0x00 |
| **0x66** | **DCHD** | *RES* | | | | DRTDFC[11:8] | | | | 0x00 |

DC Ring Trip Coefficient is governed by the cutoff frequency $f_{LP}$

$$DRTFC[11:0] \ = \left[\frac{1 \ -(2 * \pi * f_{LP})}{800}\right] \ x \ \ 2^{12}$$

### 14.8.6. DC RING TRIP CURRENT THRESHOLD

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x67** | **RTTD** | *RES* | XRTR | DRTT[5:0] | | | | | | 0x00 |

DC Ring Trip current Threshold in Internal Ringing Mode

| | **RING TRIP DETECT THRESHOLD [DRTT]** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 A | 80 mA | 1.27 mA |

### 14.8.7. DC RING TRIP DEBOUNCE TIME

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x68** | **RTDBD** | DRTD[7:0] | | | | | | | | 0x00 |

| | **DC RING TRIP DEBOUNCE TIME** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 msec | 159 msec | 1.25 msec |

### 14.8.8. EXTERNAL BATTERY SWITCH OUTPUT CONFIGURATION 1

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x6A** | **XBSDCN** | DCNXB[7:0] | | | | | | | | 0x00 |
| **0x6B** | **XBSDCP** | DCPXB[7:0] | | | | | | | | 0x00 |

External battery switch DCN pin and DCP output configuration for different line states

| Linefeed State | XBSDCN Register<br>XBSDCP Register | | | | | | | | DCN output<br>DCP output |
|---|---|---|---|---|---|---|---|---|---|
| Open | x | x | x | x | x | x | x | 0 | LOW |
| Open | x | x | x | x | x | x | x | 1 | HIGH |
| Forward/Reverse Active | x | x | x | x | x | x | 0 | x | LOW |
| Forward/Reverse Active | x | x | x | x | x | x | 1 | x | HIGH |
| Forward/Reverse ON-HOOK Transmission | x | x | x | x | x | 0 | x | x | LOW |
| Forward/Reverse ON-HOOK Transmission | x | x | x | x | x | 1 | x | x | HIGH |
| TIP/RING Open | x | x | x | x | 0 | x | x | x | LOW |
| TIP/RING Open | x | x | x | x | 1 | x | x | x | HIGH |
| Ringing | x | x | x | 0 | x | x | x | x | LOW |
| Ringing | x | x | x | 1 | x | x | x | x | HIGH |
| Forward/Reverse Idle | x | x | 0 | x | x | x | x | x | LOW |
| Forward/Reverse Idle | x | x | 1 | x | x | x | x | x | HIGH |
| Calibration Mode | x | 0 | x | x | x | x | x | x | LOW |
| Calibration Mode | x | 1 | x | x | x | x | x | x | HIGH |

### 14.8.9. DC/DC HEAVY CURRENT CONVERTER

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x6E** | **LOAD** | *RES* | | | | | | | LOAD | 0x00 |

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | DC/DC Heavy Current Load | **LOAD** | Light load | Heavy Current Load such as Ringing for DC/DC converter |

### 14.8.10. DC/DC TARGET VOLTAGE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x77** | **DCTR** | VTR[7:0] (RO) | | | | | | | | **0XC8** |

In Inductor mode the Target Voltage for DC/DC Converter is a **READ ONLY** register.

| | **DC/DC TARGET VOLTAGE [VTR]** | | | |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | Default |
| **Range** | 0 V | - 93.5 V | 1.484 V | 3.0 V |

## 14.9. MONITORING REGISTERS

### 14.9.1. MONITOR CURRENT FOR RING TRIP AND LOOP CLOSURE

| Addr (Hex) | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default (Hex) | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 78 | **RTMNT** | MNTRT[7:0] | | | | | | | | 00 | RO |
| 79 | **LCMNT** | MNTLC[7:0] | | | | | | | | 00 | RO |

| | **RING TRIP CURRENT MONITOR<br>LOOP CLOSURE CURRENT MONITOR** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 A | 80 mA | 0.317 mA |

### 14.9.2. MONITOR CURRENT FOR RING TRIP AND LOOP CLOSURE

| Addr (Hex) | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default (Hex) | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 7A | **MNT5** | MNTQ1[7:0] | | | | | | | | | RO |
| 7B | **MNT7** | MNTQ2[7:0] | | | | | | | | | RO |
| 7C | **MNT9** | MNTQ3[7:0] | | | | | | | | | RO |
| 7D | **MNT11** | MNTQ4[7:0] | | | | | | | | | RO |
| 7E | **MNT13** | MNTQ5[7:0] | | | | | | | | | RO |
| 7F | **MNT15** | MNTQ6[7:0] | | | | | | | | | RO |

| TRANSISTOR POWER DESSIPATION<br>TIP, RING, and LOOP CURRENT SENSE | | | | | |
|---|---|---|---|---|---|
| **DESCRIPTION** | **CONDITION** | **Range** | **Minimum** | **Maximum** | **Stepsize** |
| Dependent on the maximum power dissipation rating of the external transistors | QT1 and QR1 | PATHQ2 | 0 W | 7.70 W | 30.4 mW |
| | QT2 and QR2 | PATHQ1 | 0 W | 0.97 W | 3.80 mW |
| | QT3 and QR3 | PATHQ3 | 0 W | 7.70 W | 30.4 mW |

### 14.10. LINE CONTROL REGISTERS

### 14.10.1. VOLTAGE REGISTERS

### 14.10.1.1. BATTERY VOLTAGE SENSE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x80** | **BATV** | VB[7:0] **(RO)** | | | | | | | | **0x02** |

Battery Voltage VB[7:0] is a **READ ONLY** register.

| | **BATTERY VOLTAGE SENSE [VB]** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 V | - 95.88 V | 0.376 V |

### 14.10.1.2. TIP/RING VOLTAGE SENSE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x81** | **VTIP** | VTIP[11:4] **(RO)** | | | | | | | | **0x00** |
| | **VTRIP (XP)** | VTIP[3:0] **(RO)** | | | | *RES* | | | | |
| **0x82** | **VRING** | VRING[11:4] **(RO)** | | | | | | | | **0x00** |
| | **VRING (XP)** | VRING[3:0] **(RO)** | | | | *RES* | | | | |

“XP” stands for extra precision register. TIP and RING voltage is a **READ ONLY** register. The range value depends on calibration. The values provided for range is without any calibration. Please refer to the SPI Peripheral Interface section for details.

| | **TIP AND RING VOLTAGE SENSE [VTIP, VRING]** | | | **Precision Bits** |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | |
| **Range** | 0 V | -95.88 V | 374 mV | 8 |
| | 0 V | -95.88 V | 23.4 mV | 12 |

### 14.10.1.3. TIP/RING TRANSISTOR 3 EMITTER VOLTAGE SENSE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x83** | **QT3V** | QT3V[7:0] (VTVE) (VQT2) **(RO)** | | | | | | | | **0x03** |
| **0x84** | **QR3V** | QR3V[7:0] (VRVE) (VQR2) **(RO)** | | | | | | | | **0x02** |

Transistors QT3 / QR3 Emitter Voltage (QT3V, QR3V) is a **READ ONLY** register. The range value depends on calibration. The values provided for range is without any calibration.

| | **TRANSISTORS QT3 / QR3 EMITTER VOLTAGE** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 V | - 95.88 V | 0.376V |

## 14.11. TRANSISTOR CURRENT REGISTERS (TIP/RING TRANSISTOR 1/2/3 CURRENT SENSE)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x85 | QT3I | QT3I[11:4] | | | | | | | | 0x05 |
| | QT3I (XP) | QT3I[3:0] | | | | *RES* | | | | |
| 0x86 | QR3I | QR3I[11:4] | | | | | | | | 0x03 |
| | QR3I (XP) | QR3I[3:0] | | | | *RES* | | | | |
| 0x87 | QT1I | QT1I[11:4] | | | | | | | | 0x03 |
| | QT1I (XP) | QT1I[3:0] | | | | *RES* | | | | |
| 0x88 | QT2I | QT2I[11:4] | | | | | | | | 0x03 |
| | QT2I (XP) | QT2I[3:0] | | | | *RES* | | | | |
| 0x89 | QR1I | QR1I[11:4] | | | | | | | | 0x03 |
| | QR1I (XP) | QR1I[3:0] | | | | *RES* | | | | |
| 0x8A | QR2I | QR2I[11:4] | | | | | | | | 0x03 |
| | QR2I (XP) | QR2I[3:0] | | | | *RES* | | | | |

"XP" stands for extra precision register. TIP/RING Transistor 1/2/3 Current register is a **READ ONLY**. The range value depends on calibration. The values provided for Range is without any calibration. Please refer to the SPI Peripheral Interface section for details.

| | **REAL TIME CURRENT** | | | **Precision Bits** |
|---|---|---|---|---|
| | **Range** | | | |
| | Minimum | Maximum | Increment | |
| **QT3I** | 0 A | 78.54 mA | 306 µA | 8 |
| | 0 A | 78.54 mA | 19.18 µA | 12 |
| **QR3I** | 0 A | 78.54 mA | 306 µA | 8 |
| | 0 A | 78.54 mA | 19.18 µA | 12 |
| **QT1I** | 0 A | 78.54 mA | 306 µA | 8 |
| | 0 A | 78.54 mA | 19.18 µA | 12 |
| **QT2I** | 0 A | 9.95 mA | 38.8 µA | 8 |
| | 0 A | 9.95 mA | 2.43 µA | 12 |
| **QR1I** | 0 A | 78.54 mA | 306 µA | 8 |
| | 0 A | 78.54 mA | 19.18 µA | 12 |
| **QR2I** | 0 A | 9.95 mA | 38.8 µA | 8 |
| | 0 A | 9.95 mA | 2.43 µA | 12 |

## 14.12. LOOP SUPERVISION

### 14.12.1. LONGITUDINAL CURRENT

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x8C** | **LGI** | ILG[11:4] | | | | | | | | **0x00** |
| | **LGI (XP)** | ILG[3:0] | | | | *RES* | | | | |

"XP" stands for extra precision register. The range value depends on calibration. The values provided for Range is without any calibration. Please refer to the SPI Peripheral Interface section for details.

$$ILG = \frac{(IQT1 - IQT3 - IQR3 + IQR1)}{2}$$

| | **LONGITUDINAL CURRENT** | | | **Precision Bits** |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | |
| **Range** | 0 mA | 77.62 mA | 303 uA | 8 |
| | 0 mA | 77.62 mA | 18.95 uA | 12 |

### 14.12.2. LOOP VOLTAGE SENSE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x8D** | **LPV** | VLP[11:4] (RO) | | | | | | | | **00** |
| | **LPV (XP)** | VLP[3:0] (RO) | | | | *RES* | | | | |

"XP" stands for extra precision register. Loop Voltage is a **READ ONLY** register. The range value depends on calibration. The values provided for Range is without any calibration. This is a 12-bit register. Please refer to the SPI Peripheral Interface section for details.

| | **LOOP VOLTAGE** ($V_{TIP} - V_{RING}$) | | | **Precision Bits** |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | |
| **Range** | 0 V | - 95.88 V | 374 mV | 8 |
| | 0 V | - 95.88 V | 23.41mV | 12 |

### 14.12.3. TIP, RING, AND LOOP CURRENT (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x8E** | **TIPI** | ITLP[11:4] (RO) | | | | | | | | **NA** |
| | **TIPI (XP)** | ITLP[3:0] (RO) | | | | *RES* | | | | |
| **0x8F** | **RINGI** | IRLP[11:4] (RO) | | | | | | | | **NA** |
| | **RINGI (XP)** | IRLP[3:0] (RO) | | | | *RES* | | | | |
| **0x90** | **LPI** | ILP[11:4] (RO) | | | | | | | | **NA** |
| | **LPI (XP)** | ILP[3:0] (RO) | | | | *RES* | | | | |

"XP" stands for extra precision register. The above registers are **READ ONLY**. The range value depends on calibration. The values provided for Range is without any calibration. Please refer to the SPI Peripheral Interface section for details.

| | **TIP, RING, and LOOP CURRENT** | | | **Precision Bits** |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | |
| **Range** | 0 mA | 77.62 mA | 303 uA | 8 |
| | 0 mA | 77.62 mA | 18.95 uA | 12 |

### 14.12.4. POLARITY

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x91** | **POL** | *RES* | | P2PEN | ILGP | ILPP | IRLP | ITLP | VLP | **NA** |

Loop voltage, TIP Current, RING Current, Loop Current, and Longitudinal Current all have Sign Bit associated with it. The Polarity register contains all the Sign or Polarity bits. For these registers mentioned the range can also extend in the negative direction by setting the Sign or Polarity bit.

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Loop Voltage | **VLP** | Positive | Negative |
| 1 | TIP Current | **ITLP** | Positive | Negative |
| 2 | RING Current | **IRLP** | Positive | Negative |
| 3 | Loop Current | **ILPP** | Positive | Negative |
| 4 | Longitudinal Current | **ILGP** | Positive | Negative |
| 5 | Loop current PK-2-PK clear | **P2PEN** | Clear value | Continuously updates new peak values |

When P2PEN[5] is set from 0 to 1 the peak detector circuit register value is cleared. If P2PEN[5] is set to HIGH and it remain at HIGH than the peak detector circuit register value is continuously updated with new peak values.

### 14.12.5. COMMON MODE VOLTAGE

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x92** | **SCM** | SCM[11:4] | | | | | | | | **NA** |
| | **SCM (XP)** | SCM[3:0] | | | | *RES* | | | | |

"XP" stands for extra precision register. The Common Mode Voltage is calculated using the equation below. Please refer to the SPI Peripheral Interface section for details.

$$\frac{(V_{TIP} + V_{RING})}{2}$$

### 14.12.6. TIP EMITTER VOLTAGE FOR TRANSISTORS QT1 SENSE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x93** | **VEQT1** | VEQT1[7:0] (RO) | | | | | | | | **NA** |

This is the emitter sense of the transistor QT1 which is used for the power alarm computation. This register is a **READ ONLY** register. The range value depends on calibration. The values provided for range is without any calibration.

| | **TIP - TRANSISTOR QT1 EMITTER VOLTAGE SENSE** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 V | - 95.88 V | 0.376 V |

### 14.12.7. TIP VOLTAGE FOR TRANSISTOR QT1 SENSE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x94** | **VQT1** | VQT1[7:0] (RO) | | | | | | | | **NA** |

The value in this register is derived from TIP voltage and TIP emitter voltage of the transistor. This is the emitter sense of the transistor QT1 which is used for the power alarm computation. This register is a **READ ONLY** register. The range value depends on calibration. The values provided for range is without any calibration.

| | **TIP - TRANSISTOR QT1 VOLTAGE SENSE** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 V | - 95.88 V | 0.376 V |

### 14.12.8. RING EMITTER VOLTAGE FOR TRANSISTOR QT1 SENSE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x95** | **VEQR1** | VEQR1[7:0] (RO) | | | | | | | | **NA** |

This is the emitter sense of the transistor QR1 which is used for the power alarm computation. This register is a **READ ONLY** register. The range value depends on calibration. The values provided for range is without any calibration.

| | **RING - TRANSISTOR QR1 EMITTER VOLTAGE SENSE** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 V | - 95.88 V | 0.376 V |

### 14.12.9. RING VOLTAGE FOR TRANSISTOR QT1 SENSE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x96** | **VQR1** | VQR1[7:0] (RO) | | | | | | | | **NA** |

The value in this register is derived from RING voltage and RING emitter voltage of the transistor. This is the emitter sense of the transistor QR1 which is used for the power alarm computation. This register is a **READ ONLY** register. The range value depends on calibration. The values provided for range is without any calibration.

| | **RING - TRANSISTOR QR1 VOLTAGE SENSE** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 V | - 95.88 V | 0.376 V |

### 14.12.10. TEMPERATURE SENSE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x99** | **TEMP** | TS[7:0] (RO) | | | | | | | | **NA** |

Die Temperature Sense TS[7:0] is a **READ ONLY** register. The actual temperature T is given by:

$$T = TS[7:0] - 67 \qquad @\ 1^\circ C \text{ Increment}$$

### 14.12.11. BAND GAP VOLTAGE

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x9A** | **VBGAP** | VBG[7:0] | | | | | | | | **0x00** |

Bandgap Voltage Trim VBG[7:0] is a trim parameters which can be used during the calibration sequence.

### 14.12.12. PEAK TO PEAK LOOP VOLTAGE (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x9B** | **VLPP2P** | LPVP2P[11:4] (RO) | | | | | | | | **0x00** |
| | **VLPP2P (XP)** | LPVP2P[3:0] (RO) | | | | *RES* | | | | |

"XP" stands for extra precision register. This read only register captures the peak-to-peak loop voltage. The peak detector circuit clears this register value when POL:P2PEN[5] address (0X91)is set from 0 to 1 and continuously updates new peak values when P2PEN[5] is HIGH. The final peak value is held in VLPP2P:LPVP2P address (0X91) when P2PEN[5] is cleared to LOW until P2PEN[5] is set again. The peak-to-peak loop voltage is measured as (max positive peak + max negative peak) / 2.

| | **PEAK TO PEAK LOOP VOLTAGE** | | | **Precision Bits** |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | |
| **Range** | 0 V | - 95.88 V | 374 mV | 8 |
| | 0 V | - 95.88 V | 23.41mV | 12 |

### 14.12.13. PEAK TO PEAK LOOP CURRENT (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x9C** | **ILPP2P** | LPIP2P[11:4] (RO) | | | | | | | | **NA** |
| | **ILPP2P (XP)** | LPIP2P[3:0] (RO) | | | | *RES* | | | | |

"XP" stands for extra precision register. This read only register captures the peak-to-peak loop current. The peak detector circuit clears this register value when POL:P2PEN[5] address (0X91)is set from 0 to 1 and continuously updates new peak values when P2PEN[5] is HIGH. The final peak value is held in ILPP2P:LPIP2P address (0X91) when P2PEN[5] is cleared to LOW until P2PEN[5] is set again. The peak-to-peak loop current is measured as (max positive peak + max negative peak) / 2.

| | **PEAK TO PEAK LOOP CURRENT** | | | **Precision Bits** |
|---|---|---|---|---|
| | Minimum | Maximum | Increment | |
| **Range** | 0 mA | -77.62 mA | 303 uA | 8 |
| | 0 mA | -77.62 mA | 18.95 uA | 12 |

## 14.13. POWER ALARM LPF POLE REGISTERS

### 14.13.1. POWER ALARM COUNTER

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0x9F** | **PALCNT** | PALCNT[7:0] | | | | | | | | **0x00** |

The Power Alarm Counter indicates the number of rising edges of the LOWVDC or HIGHIDC flags. The value of this register clips at 255. This counter is reset after every read from this address.

a) DCDC output voltage (VBAT) 10% above full scale or
b) DCDC supply voltage (VDDC) too low or
c) DCDC supply current ($I_{VDDC}$) too high;

### 14.13.2. POWER ALARM LOW PASS FILTER POLE FOR TRANSISTORS 1/2/3

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xA0** | **PALPQ2** | Q2C[7:0] | | | | | | | | **0x00** |
| **0xA1** | **PALPQ1** | Q1C[7:0] | | | | | | | | **0x00** |
| **0xA2** | **PALPQ3** | Q3C[7:0] | | | | | | | | **0x00** |
| **0xA3** | **PALPQHn** | Q1C[11:8] | | | | Q2C[11:8] | | | | **0x00** |
| **0xA4** | **PALPQH2** | LPFEN | Q3C12 | Q1C12 | Q2C12 | Q3C[11:8] | | | | **0x00** |

The Power Alarm register are 13 bit registers. For example Q2 Power Alarm bits are located at address 0xA0, (D0 – D7, Q2C[7:0]) first 8-bits. The next 4-bits are located at address 0xA3 (D0 – D3 bits, Q2C[11:8]) and the last bit out of 13-bits is located at address 0xA4 (D4 – Q2C[12]). The other two transistor bits can be located the same way. LPFEN enables the Low Pass Filter when set to 1.

| **POWER ALARM LOW PASS FILTER POLE FOR TRANSISTORS 1/2/3** | | |
|---|---|---|
| Dependent on the thermal time constant of the external transistors | | |
| **QT2 and QR2** | **QT1 and QR1** | **QT3 and QR3** |
| **PALPQ2** | **PALPQ1** | **PALPQ3** |
| $Q2C[12:0]=\left(1-\frac{1}{800*T_{TC}}\right)*2^{13}$ | $Q1C[12:0]=\left(1-\frac{1}{800*T_{TC}}\right)*2^{13}$ | $Q3C[12:0]=\left(1-\frac{1}{800*T_{TC}}\right)*2^{13}$ |

### 14.13.3. POWER ALARM THRESHOLD FOR TRANSISTOR 1-3

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xA5** | **PATHQ2** | Q2TH[7:0] | | | | | | | | **0x00** |
| **0xA6** | **PATHQ1** | Q1TH[7:0] | | | | | | | | **0x00** |
| **0xA7** | **PATHQ3** | Q3TH[7:0] | | | | | | | | **0x00** |

| TIP, RING, and LOOP CURRENT | | | | | |
|---|---|---|---|---|---|
| **DESCRIPTION** | **CONDITION** | **Range** | **Minimum** | **Maximum** | **Increment** |
| Dependent on the maximum power dissipation rating of the external transistors | QT1 and QR1 | PATHQ2 | 0 W | 7.7 W | 30.4 mW |
| | QT2 and QR2 | PATHQ1 | 0 W | 0.97 W | 3.8 mW |
| | QT3 and QR3 | PATHQ3 | 0 W | 7.7 W | 30.4 mW |

### 14.14. IMPEDANCE MATCHING 1/2

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xA8** | **IM1** | *RES* | | | | ZR1[3:0] | | | | **0x00** |
| **0xA9** | **IM2** | *RES* | ZSW | *RES* | | | | | | **0x00** |

"*RES*" in the register map means reserved bit(s).

| Impedance Matching/ R1 Element | | | | |
|---|---|---|---|---|
| **ZR13** | **ZR12** | **ZR11** | **ZR10** | **R1 (Ohm)** |
| 0 | 0 | 0 | 0 | 600 Ω |
| 0 | 0 | 0 | 1 | 900 Ω |
| 0 | 0 | 1 | 0 | 600 Ω |
| 0 | 0 | 1 | 1 | 900 Ω |
| 0 | 1 | 0 | 0 | 270 Ω |
| 0 | 1 | 0 | 1 | 200 Ω |
| 0 | 1 | 1 | 0 | 200 Ω |
| 0 | 1 | 1 | 1 | 100 Ω |
| 1 | 0 | 0 | 0 | 370 Ω |
| 1 | 0 | 0 | 1 | 220 Ω |
| 1 | 0 | 1 | 0 | 320 Ω |
| 1 | 0 | 1 | 1 | 220 Ω |
| 1 | 1 | x | x | Not Used |

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 6 | Impedance matching Feedback loop Disable | **ZSW** | Default, enabled | Disables impedance matching feedback loop for diagnostics testing |

### 14.14.1. TEMPERATURE ALARM THRESHOLD

| Addr | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xAA** | **THAT** | TATH[7:0] | | | | | | | | **0x00** |

$T_{TH}$ = TATH[7:0] – 67 @ Increment of 1°C

### 14.14.2. LOOP CLOSURE MASK COUNT

| Addr | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xAB** | **LCMCNT** | LCMCNT[7:0] | | | | | | | | **0x00** |

| | LOOP CLOSURE MASK COUNT | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 ms | 319 ms | 1.25 ms |

### 14.14.3. COARSE CALIBRATION INTERNAL RESISTOR

| Addr | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xAC** | **CC** | *RES* | | | | CBGSW | CTRIM[2:0] | | | **0x00** |

*"RES"* in the register map means reserved bit(s).Coarse Calibration CTRIM[2:0] and Internal Resistor CBGSW are a trim parameters which can be used during the calibration sequence.

### 14.14.4. OSCILLATOR 2 RINGING PHASE DELAY

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xAD** | **OS2RPD** | O2RPD[7:0] | | | | | | | | 0x00 |

When Oscillator 2 is used for Tone Generation it is recommended this register be set to 0x00. If the ringing phase delay in oscillator 2 (0xAD) is used , zero crossing function must be enabled OSN:O2ZC[5] address 0xC0.

| | **OSCILLATOR 2 RINGING PHASE DELAY** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 ms | 31.8 ms | 125 us |

### 14.15. CALIBRATION

| Addr | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xAF** | **CAL1** | SDAT[3:0] | | | | VBATT[3:0] | | | | 0X77 |
| **0xB0** | **CAL2** | TVTE1[3:0] | | | | SDBT[3:0] | | | | 0X97 |
| **0xB1** | **CAL3** | SCMT[3:0] | | | | RVTE[3:0] | | | | 0X79 |

All values are trim parameters which can be used during the calibration sequence.

| Bits | Trim |
|---|---|
| VBATT[3:0] | VBAT Trim |
| SDAT[3:0] | SDA Trim |
| SDBT[3:0] | SDB Trim |
| TVTE1[3:0] | TVE1 Trim |
| RVTE[3:0] | RVE1 Trim |
| SCMT[3:0] | SCM Trim |

## 14.16. DC OFFSET REGISTERS

### 14.16.1. DC OFFSET (RING, TIP, AND VBAT)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xB4** | **IQTROS** | HISENSE | BTVR | ILFDB | DACSFC | *RES* | | | | **0x00** |

"*RES*" in the register map means reserved bit(s).

All values are trim parameters which can be used during the calibration sequence.

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 4 | Smoothing Filter | **DACSFC** | Cutoff at 1xfc | Cutoff 2xfc |
| 5 | Line driver bias | **ILFDB** | Fixed Bias | Bias varies with coarse calibration |
| 6 | DC/DC Range | **BTVR** | Normal | Low VBAT |
| 7 | Monitor DC Range | **HISENSE** | Normal line | Extended line |

### 14.16.2. PWM COUNT (READ ONLY)

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xB5** | **PWCT** | PWCT[7:0] (RO) | | | | | | | | NA |

This register is a **READ ONLY**. PWM Count Register can calculate DC/DC Converter Pulse Width TON with the following equation.

TON = PWCT[7:0] * PLL Period

The TON Range is 0 ns to (PWM Period-TOFF) see PWMT and DDCC with a stepsize of PLL period. The PLL Period (expressed in nsec) which is selected based on the setting of PON:CDCC[7] address (0x22) and whether the BCLK is binary or decimal.

## 14.17. TONE GENERATION REGISTERS

### 14.17.1. OSCILLATOR CONTROL

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xC0** | **OSN** | *RES* | | O2ZC | O1ZC | *RES* | | O2E | O1E | 0x00 |

"*RES*" in the register map means reserved bit(s).

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Oscillator 1 | **O1E** | Disable | Enable |
| 1 | Oscillator 2 | **O2E** | Disable | Enable |
| 4 | Oscillator n Zero-Crossing | **O1ZC** | Disable | Enable |
| 5 | Oscillator 2 Zero-Crossing | **O2ZC** | Disable | Enable |

### 14.17.2. RING CONTROL

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xC1** | **RMPC** | TRAP | LBAC | R1EN | *RES* | TOR | *RES* | | | 0x00 |

"*RES*" in the register map means reserved bit(s).

| Bit Location | Bit Description | Bit Name | Bit Value | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 3 | Tone Route | **TOR** | Transmit direction (towards DAC) | Receive direction (towards ADC) |
| 5 | Ringer 1 | **R1EN** | Disable | Enable |
| 6 | Ringing Waveform | **LBAC** | Sinusoidal RING Waveform | Trapezoidal RING Waveform |
| 7 | Ringing Waveform Select | **TRAP** | Disable | Enable |

### 14.17.3. OSCILLATOR 1 AND 2 INITIAL CONDITION LOW/HIGH

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xC2** | **OS1ICL** | O1IC[7:0] | | | | | | | | 0x00 |
| **0xC3** | **OS1ICH** | O1IC[15:8] | | | | | | | | 0x00 |
| **0xC4** | **OS2ICL** | O2IC[7:0] | | | | | | | | 0x00 |
| **0xC5** | **OS2ICH** | O2IC[15:8] | | | | | | | | 0x00 |

Initial Condition for Oscillator m OmIC[15:0] m=1,and 2 can be determined by formula.  Refer to Tone Generation see Section for the formula.

### 14.17.4. OSCILLATOR 1 AND 2 COEFFICIENT LOW/HIGH

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xC6** | **OS1CL** | O1C[7:0] | | | | | | | | 0x00 |
| **0xC7** | **OS1CH** | O1C[15:8] | | | | | | | | 0x00 |
| **0xC8** | **OS2CL** | O2C[9:2] | | | | | | | | 0x00 |
| **0xC9** | **OS2CH** | O2C[17:10] | | | | | | | | 0x00 |

Coefficient for Oscillator m (OmC[15:0] m=1, and 2, refer to Tone Generation see section for the formula. OS2CL is 18-bits long word. The 16 most significant bits are on address 0xC8[9:2] and 0xC9[17:10]. The 2 least significant bits are located in register address 0xDC (D7 - D6).

## 14.18. OSCILLATOR 1 AND 2 ACTIVE/ INACTIVE TIME LOW/HIGH

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xCA** | **OS1ATL** | O1ON[7:0] | | | | | | | | 0x00 |
| **0xCB** | **OS1ATH** | O1ON[15:8] | | | | | | | | 0x00 |
| **0xCC** | **OS2ATL** | O2ON[7:0] | | | | | | | | 0x00 |
| **0xCD** | **OS2ATH** | O2ON[15:8] | | | | | | | | 0x00 |
| **0xCE** | **OS1ITL** | O1OFF[7:0] | | | | | | | | 0x00 |
| **0xCF** | **OS1ITH** | O1OFF[15:8] | | | | | | | | 0x00 |
| **0xD0** | **OS2ITL** | O2OFF[7:0] | | | | | | | | 0x00 |
| **0xD1** | **OS2ITH** | O2OFF[15:8] | | | | | | | | 0x00 |

| | | | | **OSCILLATOR 1/2 ACTIVE/INACTIVE TIME** | | |
|---|---|---|---|---|---|---|
| | | | | Minimum | Maximum | Stepsize |
| Active/Inactive Timer Oscillator m | Tone Generation | Timer is disabled by programming zero | O1ON<br>O2ON<br>O1OFF<br>O2OFF | 0 s | 8 s | 125us |
| Active/Inactive Timer Oscillator 2 | Ringing only | Timer is disabled by programming zero | O2ON<br>O2OFF | 0 s | 8 s | 125us |

## 14.19. GENERAL TONE GENERATION

### 14.19.1. RING OFFSET

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xDC** | **ROFFS** | O2C[1:0] | | ROS[5:0] | | | | | | **0x00** |

"RES" in the register map means reserved bit(s).

TIP to RING Offset for Ringing, Sets DC Offset component to the Ringing Waveform

| | **RING OFFSET [ROS]** | | |
|---|---|---|---|
| | Minimum | Maximum | Increment |
| **Range** | 0 V | 47.488 V | 1.484 V |

### 14.19.2. ADC/DAC DIGITAL GAIN

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xDD** | **ADCL** | ADC[7:0] | | | | | | | | **0x00** |
| **0xDE** | **DACL** | DAC[7:0] | | | | | | | | **0x00** |
| **0xDF** | **DGH** | DAC[11:8] | | | | ADC[11:8] | | | | **0x44** |

| | | | **DIGITAL GAIN** | |
|---|---|---|---|---|
| | | | Minimum | Maximum |
| Digital Gain | ADC = $1024x10^{(XdB/20)}$<br>DAC = $1024x10^{(XdB/20)}$ | ADC<br>DAC | –∞ dB | 6 dB |

| **ADC<br>DAC** | **Gain** | **dB** |
|---|---|---|
| 0x000 | Off | -∞ |
| 0x040 | 1 / 8 | -24 |
| 0x100 | 1 / 4 | -12 |
| 0x200 | 1 / 2 | -6 |
| 0x400 | 1 | 0 |
| 0x7FF | 2 | 6 |

### 14.19.3. PWM DC/DC FINE TUNING

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xE0** | **ST0L0** | *RES* | | | | ST0L0[3:0] | | | | 0x02 |
| **0xE1** | **ST1L0** | *RES* | | | ST1L0[4:0] | | | | | 0x04 |
| **0xE2** | **ST2L0** | *RES* | | | ST2L0[4:0] | | | | | 0x06 |
| **0xE3** | **ST0L1** | *RES* | | | | ST0L1[3:0] | | | | 0x08 |
| **0xE4** | **ST1L1** | *RES* | | | ST1L1[4:0] | | | | | 0x10 |
| **0xE5** | **ST2L1** | *RES* | | | ST2L1[4:0] | | | | | 0x19 |

"*RES*" in the register map means reserved bit(s).

| Addr. | Name | Symbol | Description | Unit |
|---|---|---|---|---|
| 0xE0 – 0xE5 | Stepsize Region State | STx | x = 0, 1, 2 | Proportional to master clock period |
| | | Ly | L0 - Non-RINGING<br>L1 - RINGING | |

| Addr. | Name | Recommendation |
|---|---|---|
| 0xE0 | ST0L0 | 0x02 |
| 0xE1 | ST1L0 | 0x02 |
| 0xE2 | ST2L0 | 0x02 |
| 0xE3 | ST0L1 | 0x08 |
| 0xE4 | ST1L1 | 0x08 |
| 0xE5 | ST2L1 | 0x08 |

### 14.19.4. PWM DC/DC FINE TUNING SKIP PERIOD

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xE6** | **SK0L0** | SK0L0[7:0] | | | | | | | | 0x1F |
| **0xE7** | **SK1L0** | *RES* | | SK1L0[5:0] | | | | | | 0x04 |
| **0xE8** | **SK2L0** | *RES* | | | ST2L0[4:0] | | | | | 0x02 |
| **0xE9** | **SK0L1** | SK0L1[7:0] | | | | | | | | 0x1F |
| **0xEA** | **SK1L1** | *RES* | | SK1L1[5:0] | | | | | | 0x04 |
| **0xEB** | **SK2L1** | *RES* | | | SK2L1[4:0] | | | | | 0x02 |

"*RES*" in the register map means reserved bit(s).

| Addr. | Name | Recommendation |
|---|---|---|
| 0xE6 | SK0L0 | 0x06 |
| 0xE7 | SK1L0 | 0x06 |
| 0xE8 | SK2L0 | 0x06 |
| 0xE9 | SK0L1 | 0x06 |
| 0xEA | SK1L1 | 0x06 |
| 0xEB | SK2L1 | 0x06 |

| Addr. | Name | Name | Description | Unit |
|---|---|---|---|---|
| 0xE6 – 0xEB | Skip Region State | SKx | = 0, 1, 2 | # of PWM duty cycle |
| | | Ly | L0 - Non-RINGING<br>L1 - RINGING | |

### 14.19.5. PWM DC/DC FINE TUNING

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xEC** | **WM0** | *RES* | | | WM0[4:0] | | | | | 0x08 |
| **0xED** | **WM1** | *RES* | | | WM1[4:0] | | | | | 0x10 |
| **0xEE** | **WM2** | *RES* | | | WM2[4:0] | | | | | 0x18 |
| **0xEF** | **XSTEP** | PWMTC | | | | XS[3:0] | | | | 0x53 |

"*RES*" in the register map means reserved bit(s). **"n"** is the number written to the register in decimal

| Addr. | Name | Symbol | Description | Unit |
|---|---|---|---|---|
| 0xEC – 0xEE | Watermark | WMx | 0, 1, 2 | n x 1.484V |
| 0xEF | Fine Adjust Region | XS | | n x 1.484V |
| 0xEF | Time constant of VLoop sensing filter for PWM | PWMTC | | |

| Addr. | Name | Recommendation |
|---|---|---|
| 0xEC | WM0 | 0x01 |
| 0xED | WM1 | 0x02 |
| 0xEE | WM2 | 0x02 |
| 0xEF | XSTEP | 0x60 |

### 14.19.6. IMPEDANCE MATCH REGISTER

#### 14.19.6.1. IMPEDENCE MATCHING COEFFICIENT RAM

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xF3** | **IMRAM** | IMDATA | | | | | | | | 0x00 |

Read and Write location for the Impedance Matching Coefficient RAM. Used in conjunction with Write Sequence described in IMCTRL 0xF5.

#### 14.19.6.2. IMPEDANCE MATCHING DELAY COUNT

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xF4** | **IMDEL** | IMHYBDC[3:0] | | | | IMB3PDC[3:0] | | | | 0x00 |

| Bit | Impedance Matching Delay Count |
|---|---|
| IMB3PDC[3:0] | Delay count of B3Parallel path - Default no delay |
| IMHYBDC[7:4] | Delay count of Hybrid2 path - Default no delay |

Programmed in conjunction with Impedance Matching Coefficient RAM.

#### 14.19.6.3. IMPEDANCE MATCHING COEFFICIENT RAM CONTROL

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xF5** | **IMCTRL** | *RES* | | | IMRW | *RES* | IMEN | *RES* | IMPM | 0x10 |

| **Bit Location** | **Bit Description** | **Bit Name** | **Bit Value** | |
|---|---|---|---|---|
| | | | **0** | **1** |
| 0 | Program Impedance Matching Coefficient RAM | IMPM | Disable | Enable |
| 2 | Complex Impedance Matching enable | IMEN | Disable | Enable |
| 4 | Read/Write Impedance Matching Coefficient RAM | IMRW | Read | Write |

Bits 3, 5, 6, and 7 must be set to “0”. For Complex Impedance Matching Cases the appropriate set (144 Bytes) should be loaded into the following sequence into the Coefficient RAM.

**Write Step Sequence:**
1. Set IMCTRL:IMRW[4] to 1
2. Set IMCTRL:IMPM[0] to 1
3. WRITE all 144 Bytes of Impedance Matching Coefficient set to Register IMRAM (Address 0xF3) in sequence
4. Set IMCTRL:IMPM[0] to 0

**Read Step Sequence:**
1. Set IMCTRL:IMRW[4] to 0
2. Set IMCTRL:IMPM[0] to 1
3. READ all 144 Bytes of Impedance Matching Coefficient set from Register IMRAM (Address 0xF3) in sequence
4. Set IMCTRL:IMRW[4] to 1 (to Restore Default Value)
5. Set IMCTRL:IMPM[0] to 0

Once the of Impedance Matching coefficients are loaded into the RAM, the Complex Impedance is enabled by setting IMCTRL:IMEN[2]

#### 14.19.6.4. PCM SCALING

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xF6** | **PCMSCAL** | PCMSCAL[7:0] | | | | | | | | 0x00 |
| **0xF7** | **PCMSCAH** | PCMSCAL[15:8] | | | | | | | | 0x20 |

| Bit | PCM Scaling |
|---|---|
| PCMSCA[15:0] | Scaling for PCM signal. Format: 3.13 |

#### 14.19.6.5. RESERVED REGISTERS

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xF8** | | *RES* | | | | | | | | 0x00 |
| **0xF9** | | *RES* | | | | | | | | 0x00 |
| **0xFA** | | *RES* | | | | | | | | 0x00 |

These three register must be set to 0x00 during a write operation

#### 14.19.6.6. FILTER BYPASS

| Addr. | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| **0xFB** | **IMEN** | *RES* | | | | | | ADCLPFBYP | HBLPFBYP | 0x00 |

| Bit | PCM Scaling |
|---|---|
| HBLPFBYP[0] | Bypass the HB LPF. Default: 0(not bypass) |
| ADCLPFBYP[1] | Bypass the ADC LPF. Default: 0(not bypass) |

## 15. TIMING DIAGRAM

### 15.1. PCM TIMING DIAGRAM FOR NON-GCI

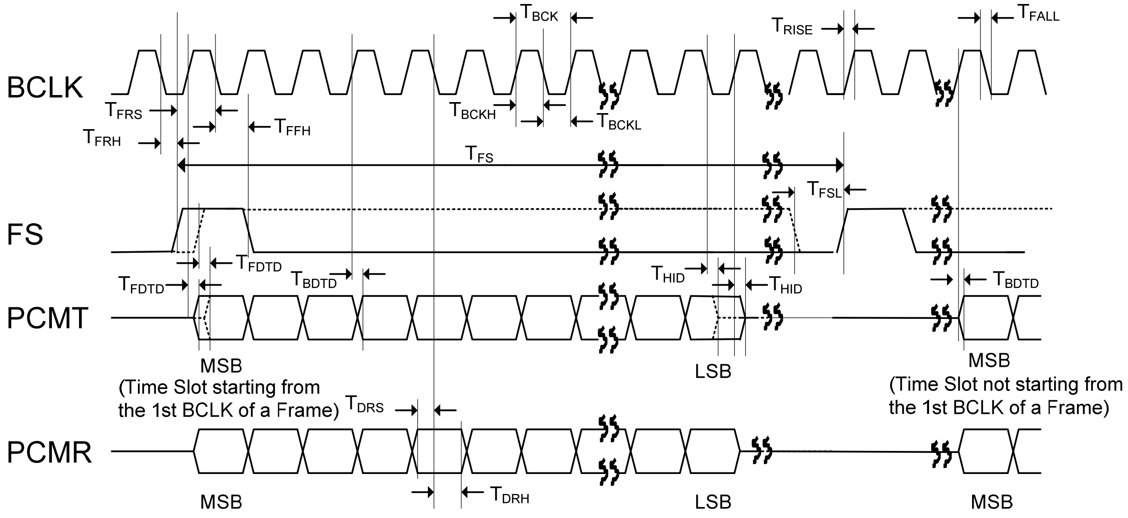


Figure 37: PCM Timing for Non-GCI

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $1/T_{FS}$ | FS Frequency | --- | 8 | --- | kHz |
| $T_{FSL}$ | FS Minimum LOW Width | $T_{BCK}$ | | | sec |
| $1/T_{BCK}$ | BCLK, BCLK Frequency | 256 | --- | 8192 | kHz |
| $T_{BCKH}$ | BCLK HIGH Pulse Width | 50 | --- | --- | ns |
| $T_{BCKL}$ | BCLK LOW Pulse Width | 50 | --- | --- | ns |
| $T_{FRH}$ | BCLK Falling Edge to FS Rising Edge Hold Time | 20 | --- | --- | ns |
| $T_{FRS}$ | FS Rising Edge to BCLK Falling edge Setup Time | 25 | --- | --- | ns |
| $T_{FFH}$ | BCLK Falling Edge to FS Falling Edge Hold Time | 20 | --- | --- | ns |
| $T_{FDTD}$ | The later of BCLK Rising Edge or FS Rising Edge to valid PCMT Delay Time if MSB Starts from the 1st BCLK of a Frame | --- | --- | 20 | ns |
| $T_{BDTD}$ | BCLK Rising Edge to Valid PCMT Delay Time | --- | --- | 20 | ns |
| $T_{HID}$ | Delay Time from BCLK Falling edge of the LSB or BCLK Rising edge following the LSB (Depending on Register TRI) to PCMT Output High Impedance | 10 | --- | 50 | ns |
| $T_{DRS}$ | Valid PCMR to BCLK Falling Edge Setup Time | 25 | --- | --- | ns |
| $T_{DRH}$ | PCMR Hold Time from BCLK Falling Edge | 20 | --- | --- | ns |

Table 8.1: PCM Timing Parameters for Non-GCI

### 15.2. PCM TIMING DIAGRAM FOR GCI

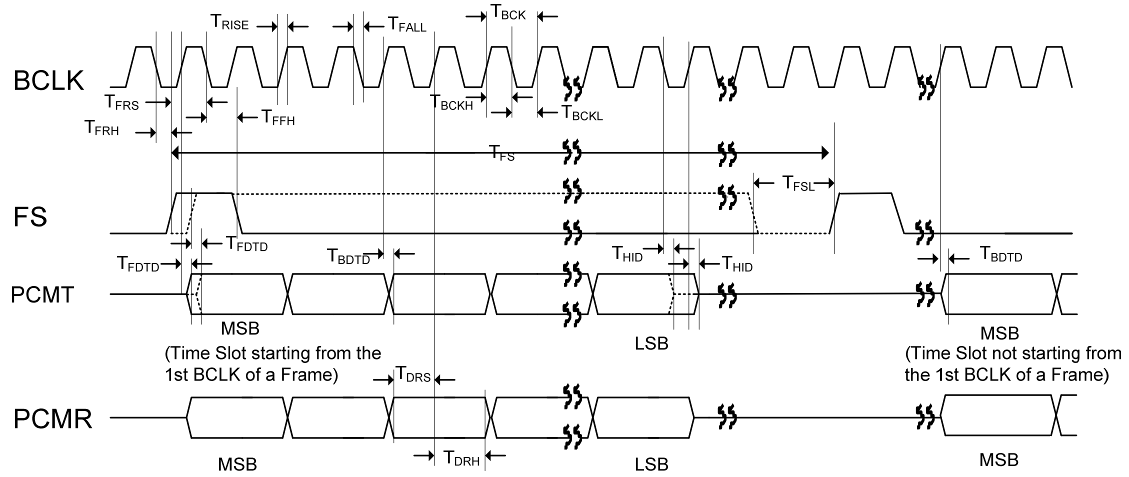


Figure 38: GCI PCM Timing

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $1/T_{FS}$ | FS Frequency | --- | 8 | --- | kHz |
| $1/T_{BCK}$ | BCLK Frequency | 512 | --- | 8192 | kHz |
| $T_{BCKH}$ | BCLK HIGH Pulse Width | 50 | --- | --- | ns |
| $T_{BCKL}$ | BCLK LOW Pulse Width | 50 | --- | --- | ns |
| $T_{FRH}$ | BCLK Falling Edge to FS Rising Edge Hold Time | 20 | --- | --- | ns |
| $T_{FRS}$ | FS Rising Edge to BCLK Falling edge Setup Time | 50 | --- | --- | ns |
| $T_{FFH}$ | BCLK Falling Edge to FS Falling Edge Hold Time | 20 | --- | --- | ns |
| $T_{FDTD}$ | The later of BCLK or FS Rising Edge to Valid PCMT Delay Time if MSB Starts from the 1st BCLK of a Frame | 10 | --- | 50 | ns |
| $T_{BDTD}$ | BCLK Rising Edge to Valid PCMT Delay Time | 10 | --- | 50 | ns |
| $T_{HID}$ | Delay Time from the Second BCLK Falling Edge of the LSB or the BCLK Rising Edge following LSB (Depending on Register TRI setting) to the PCMT Output High Impedance | 10 | --- | 50 | ns |
| $T_{DRS}$ | Valid PCMR to BCLK Rising Edge Setup Time | 20 | --- | --- | ns |
| $T_{DRH}$ | PCMR Hold Time from BCLK Rising Edge | 50 | --- | --- | ns |

Table 8.2: GCI Timing Parameters

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $1/T_{BCK}$ | BLCK Clock Frequency | --- | 0.256<br>0.512<br>0.768<br>1.000<br>1.024<br>1.152<br>1.536<br>1.544(2)<br>2.000<br>2.048<br>4.000<br>4.096<br>8.000<br>8.192 | --- | MHz |
| $T_{jitter}$ | BLCK Period Jitter Tolerance(1) | -120 | --- | 120 | ns |
| $T_{BCKH}$ / $T_{BCK}$ | BCLK Duty Cycle for 256 kHz Operation | 40% | 50% | 60% | |
| $T_{BCKH}$ | Minimum Pulse Width HIGH for BCLK(512 kHz or Higher) | 50 | --- | --- | ns |
| $T_{BCKL}$ | Minimum Pulse Width LOW for BCLK (512 kHz or Higher) | 50 | --- | --- | ns |
| $T_{FRH}$ | BCLK falling Edge to FS Rising Edge Hold Time | 50 | --- | --- | ns |
| $T_{FRS}$ | FS Rising Edge to BCLK Falling edge Setup Time | 50 | --- | --- | ns |
| $T_{RISE}$ | Rise Time for All Digital Signals | --- | --- | 25 | ns |
| $T_{FALL}$ | Fall Time for All Digital Signals | --- | --- | 25 | ns |

Table 8.3: General PCM Timing Parameters

1 *At 512 kHz BCLK*
2. *This clock is not a multiple of 256kHz or 1.000MHz. Therefore, it uses a non-integer divider.*

### 15.3. SPI TIMING DIAGRAM

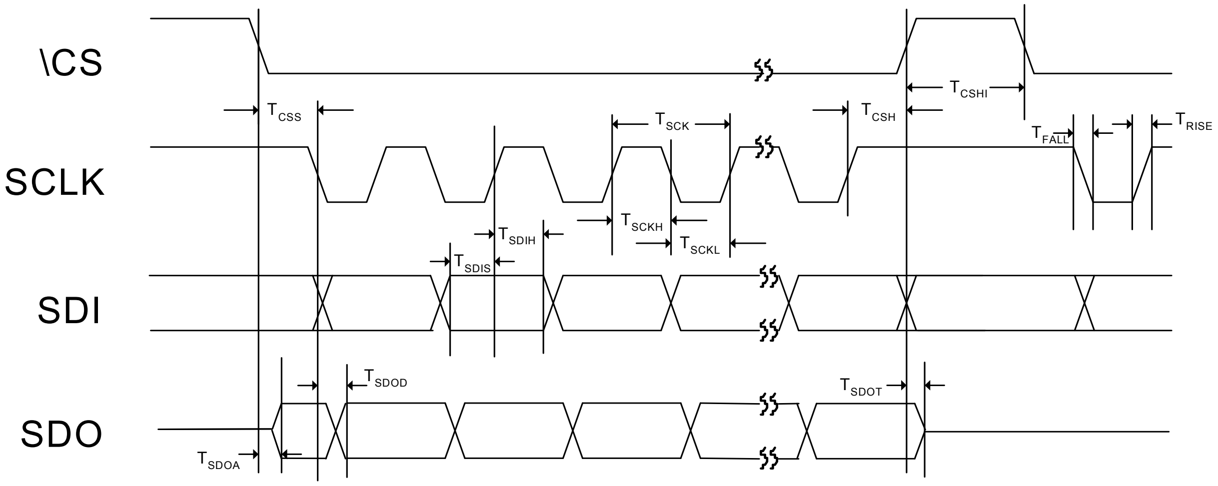


Figure 39: SPI Timing (Non-Daisy Chain Mode)

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{SCK}$ | SCLK Cycle Time | 90 | --- | --- | ns |
| $T_{SCKH}$ | SCLK High Pulse Width | 45 | --- | --- | ns |
| $T_{SCKL}$ | SCLK Low Pulse Width | 45 | --- | --- | ns |
| $T_{RISE}$ | Rise Time for All Digital Signals | --- | --- | 25 | ns |
| $T_{FALL}$ | Fall Time for All Digital Signals | --- | --- | 25 | ns |
| $T_{CSS}$ | CSb Falling Edge to 1st SCLK Falling Edge Setup Time | 45 | --- | --- | ns |
| $T_{CSH}$ | Last SCLK Rising Edge to CSb Rising Edge Hold Time | 45 | --- | --- | ns |
| $T_{CSHI}$ | CSb High, Delay Time between Chip Selects | 200 | --- | --- | ns |
| $T_{SDIS}$ | SDI to SCLK Rising Edge Setup Time | 20 | --- | --- | ns |
| $T_{SDIH}$ | SCLK Rising Edge to SDI Hold Time | 20 | --- | --- | ns |
| $T_{SDOD}$ | Delay Time from SCLK Falling Edge to SDO Data | --- | --- | 20 | ns |
| $T_{SDOT}$ | Delay Time from CSb Rising Edge to SDO Tri-State | --- | --- | 10 | ns |
| $T_{SDOA}$ | Delay Time from CSb Falling Edge to SDO Active | --- | --- | 10 | ns |

Table 8.4: General SPI Timing Parameters

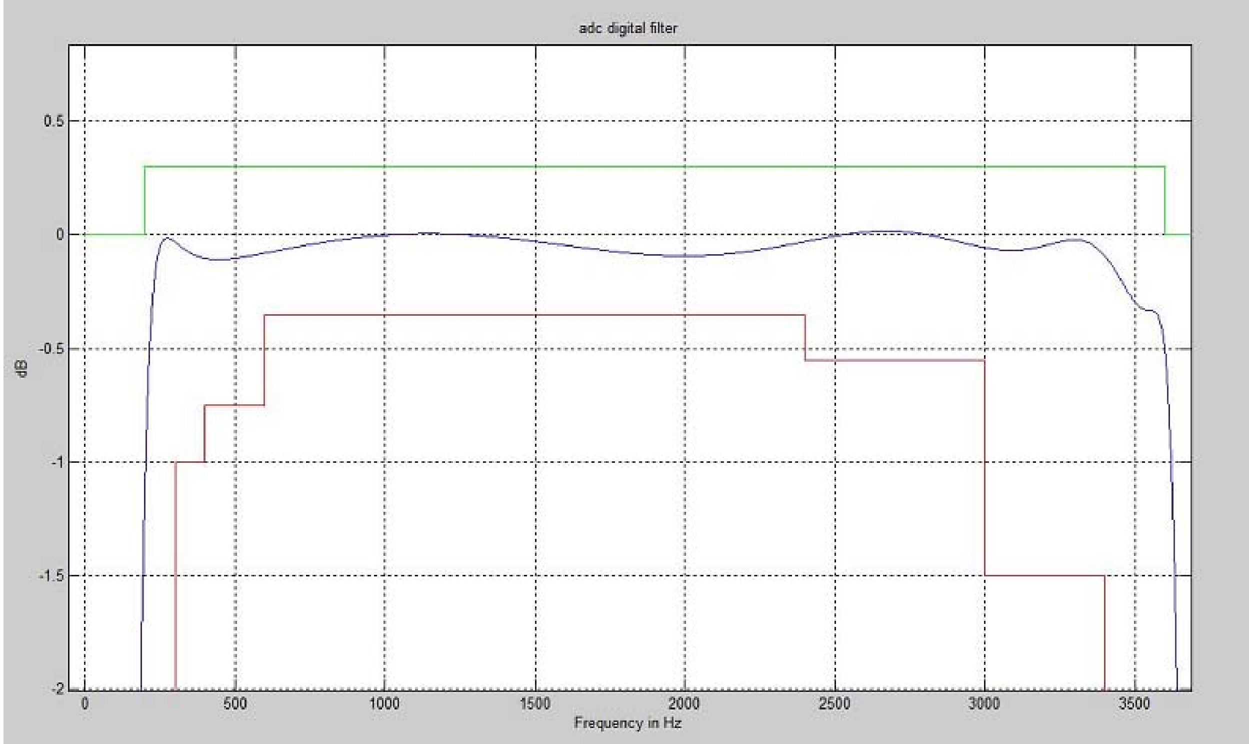


Figure 40: In-band Transmit Frequency Response

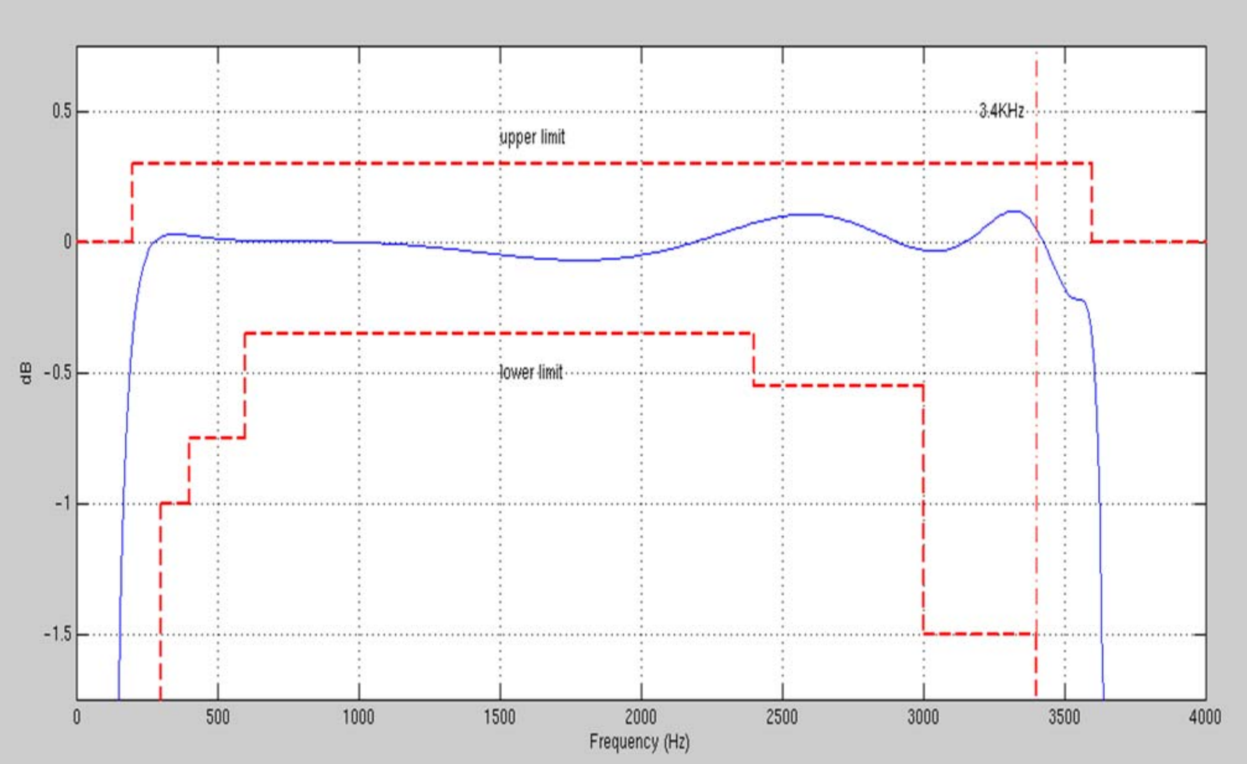


Figure 41: In-band Receive Frequency Response

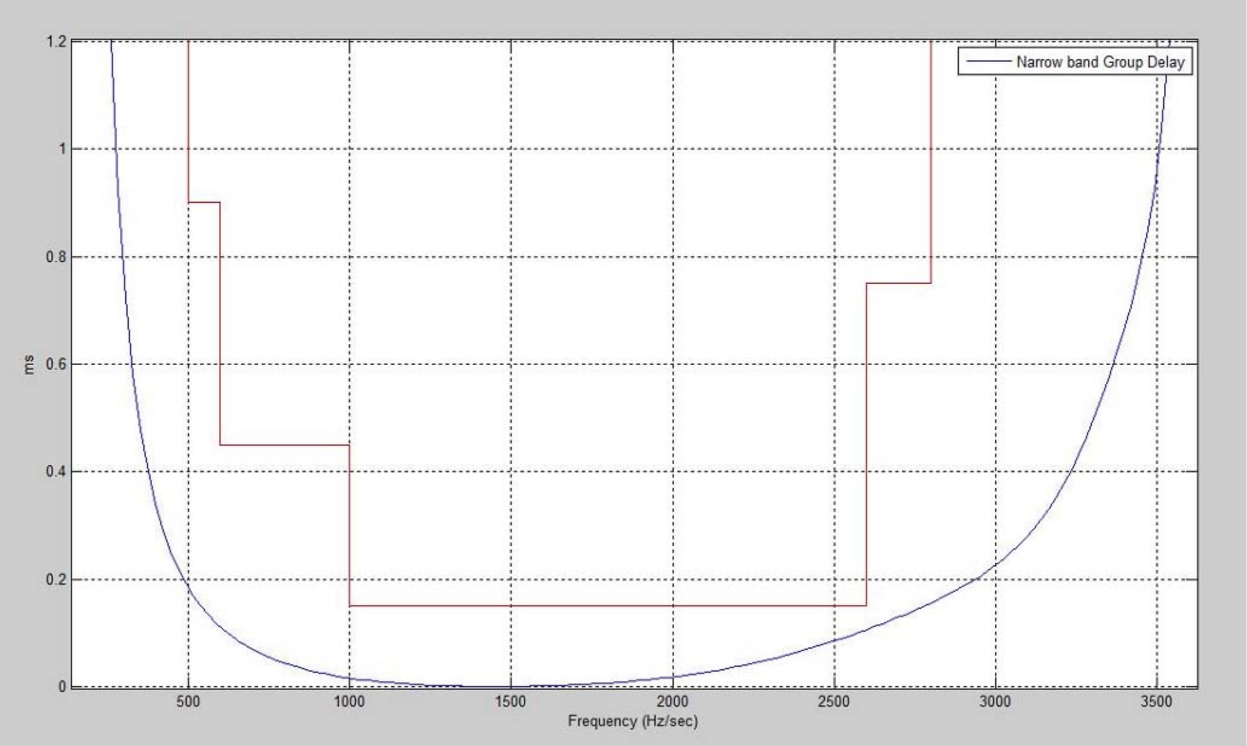


Figure 42: Transmit Group Delay Distortion

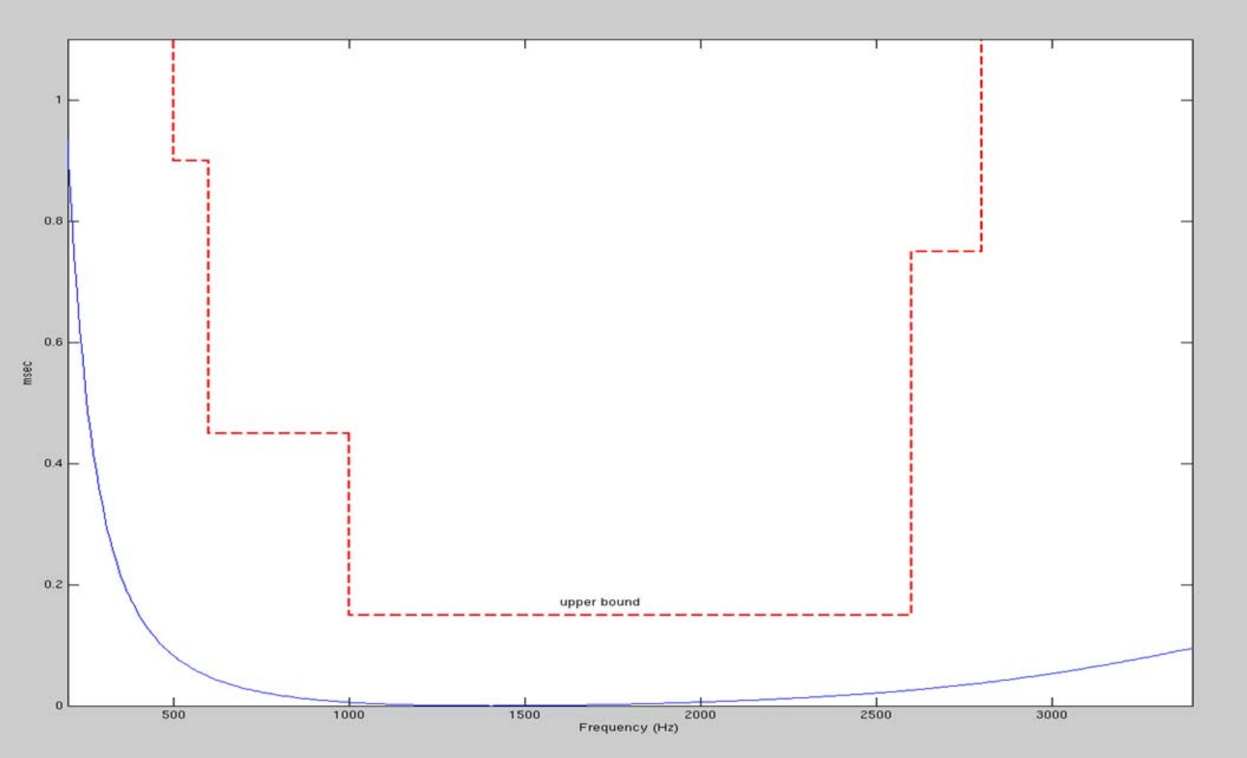


Figure 43: Receive Group Delay Distortion

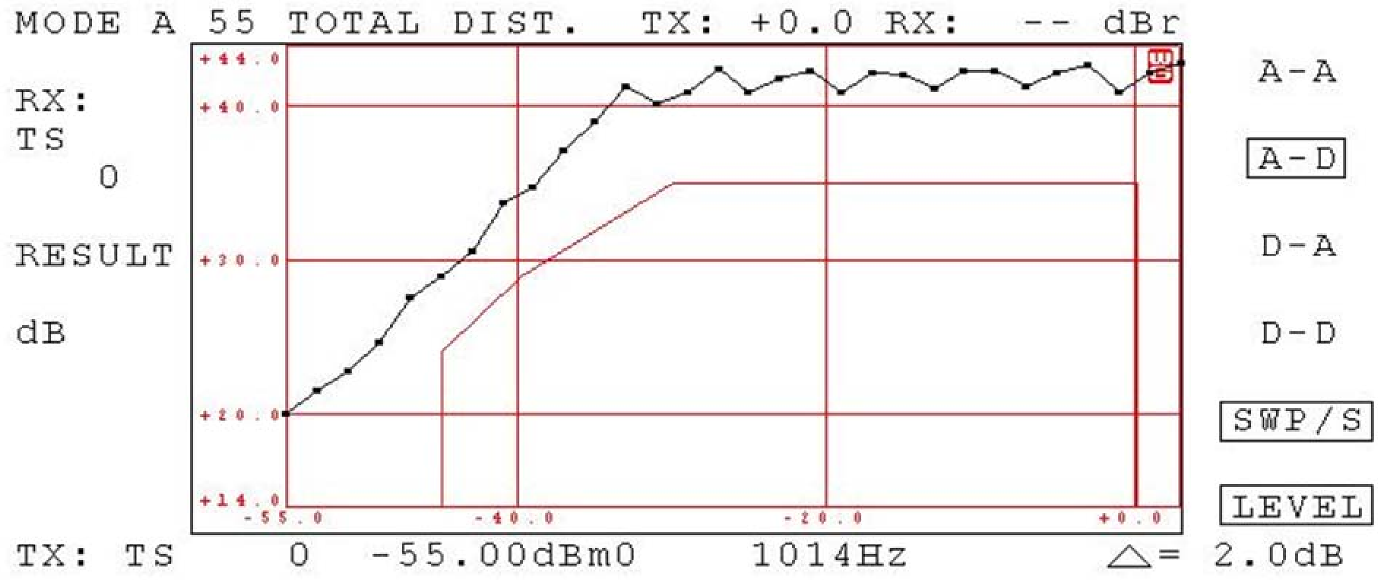


Figure 44: 2-Wire to PCM Signal to Distortion Mask (A-Law)

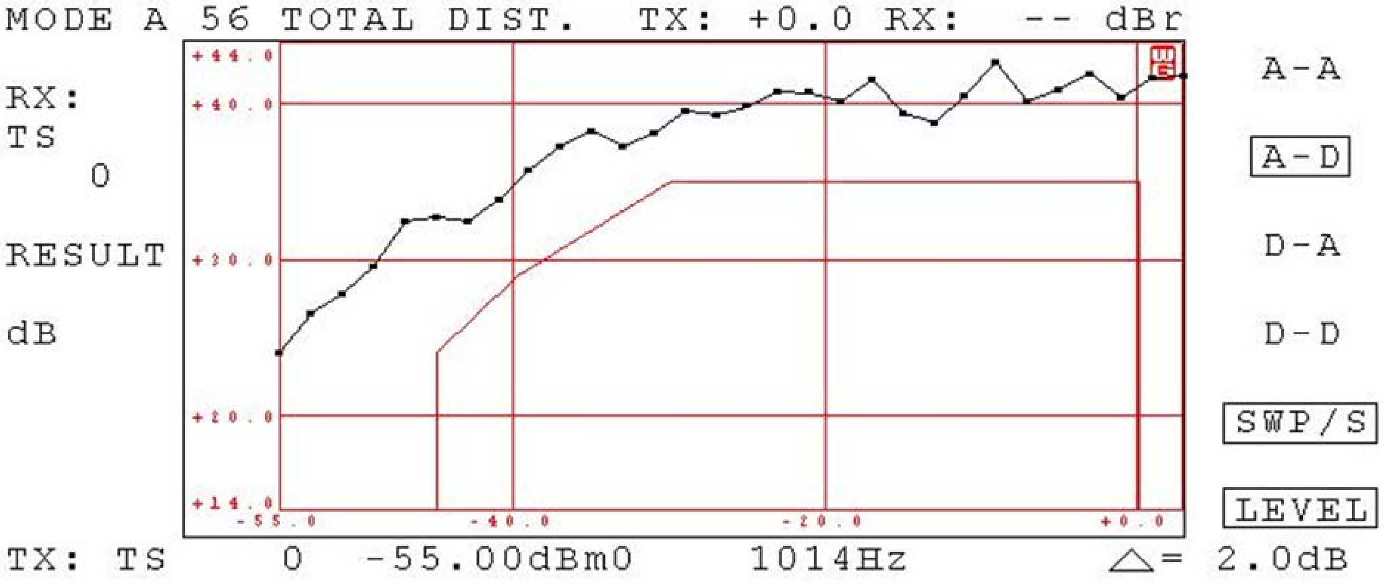


Figure 45: 2-Wire to PCM Signal to Distortion Mask (μ-Law)

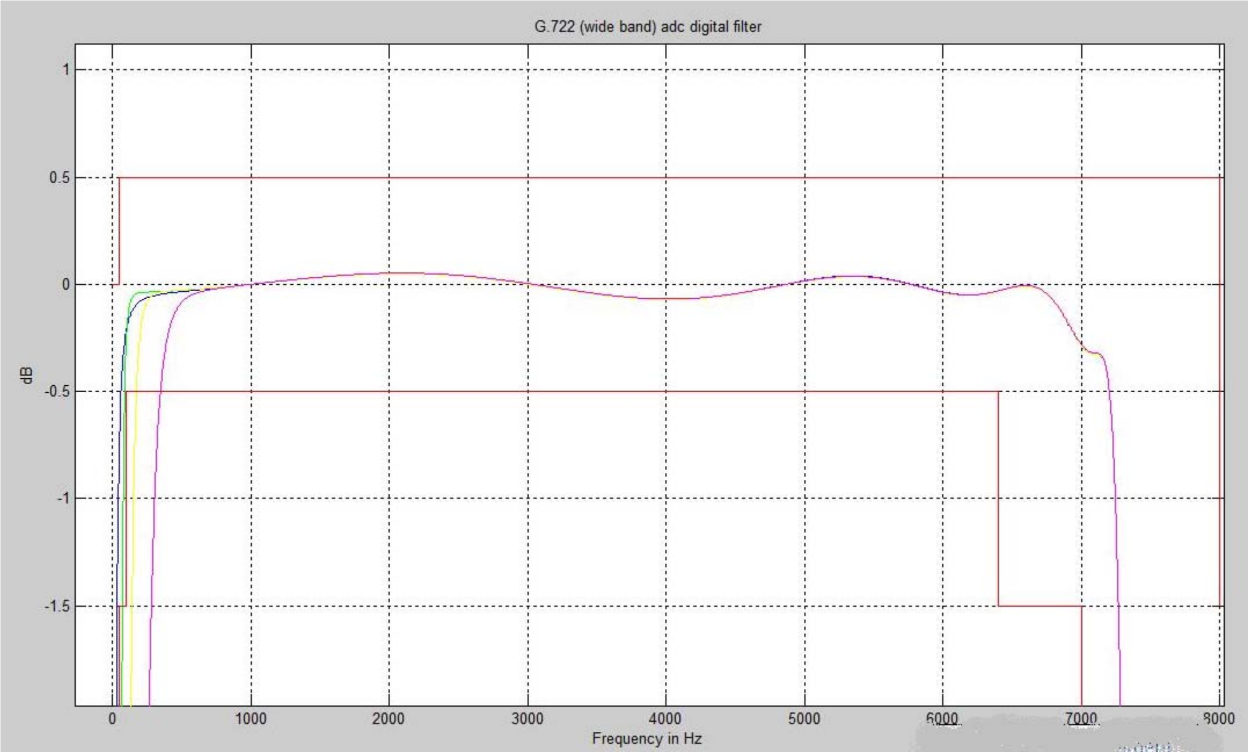


**Figure 46: Wideband In-band Transmit Frequency Response**

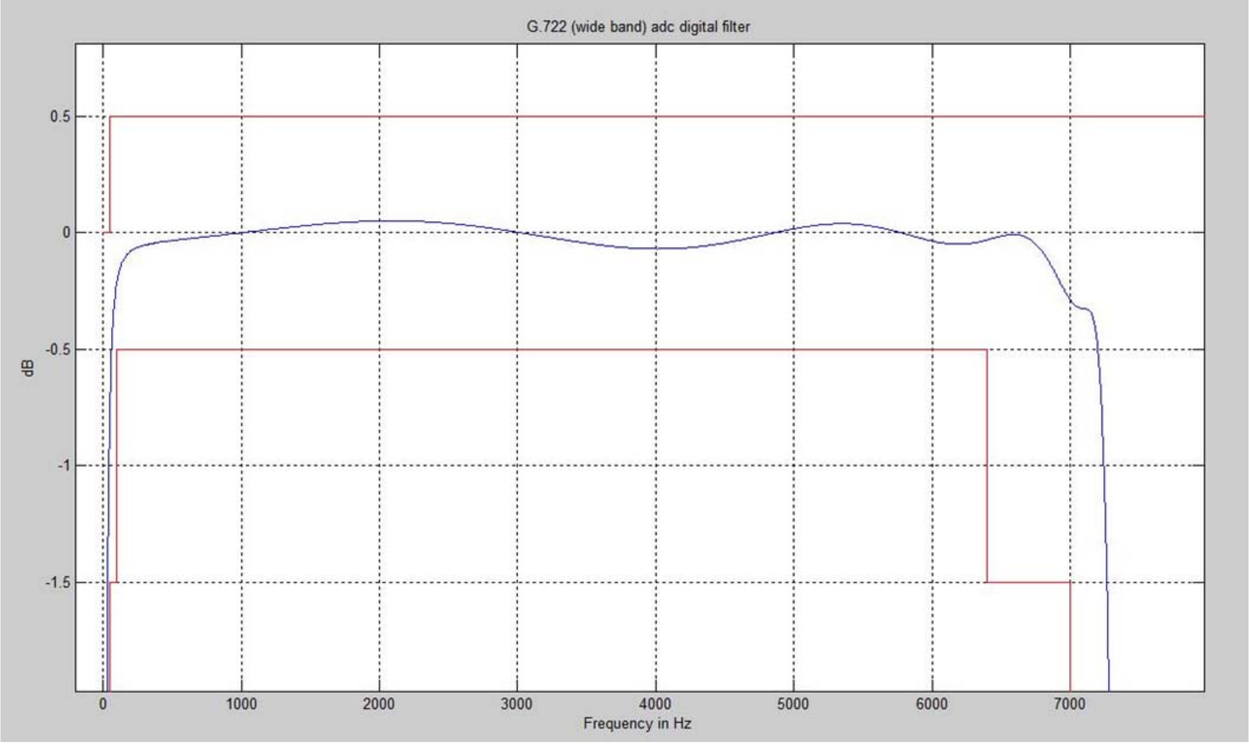


**Figure 47: Wideband Transmit Group Delay Distortion**

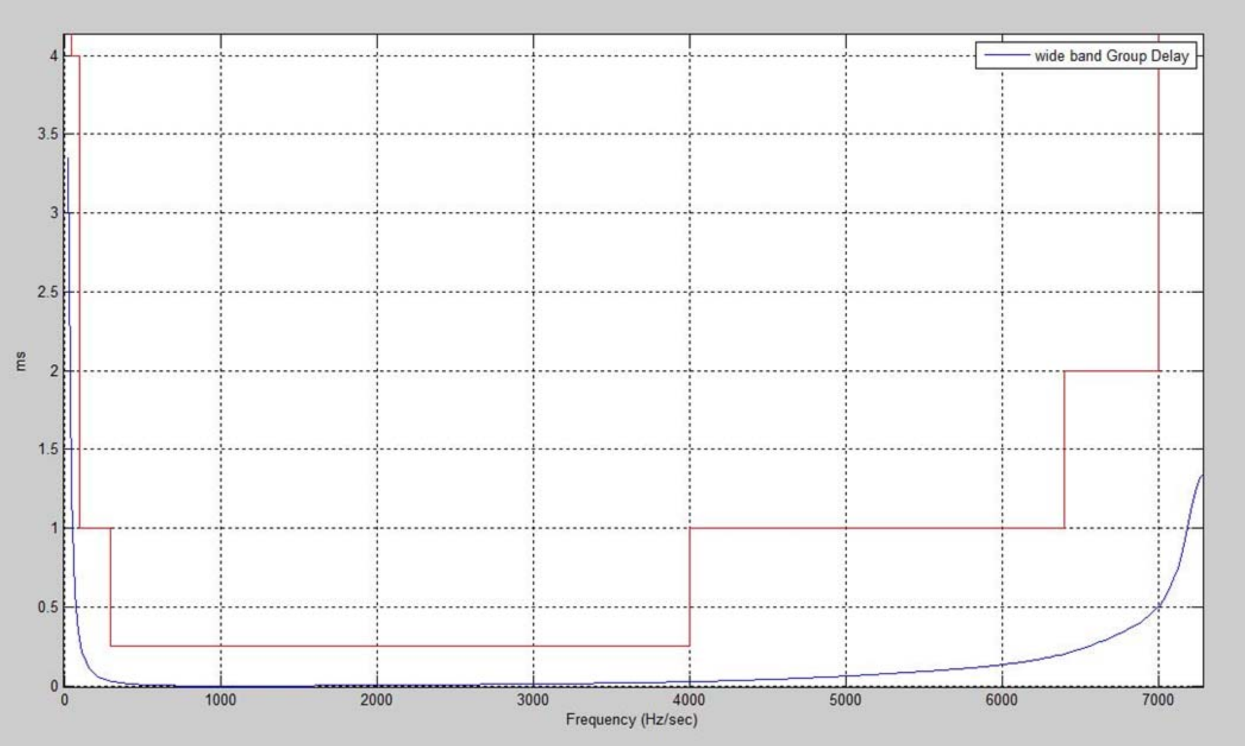


**Figure 48: Wideband Receive Group Delay Distortion**

## 16. DIGITAL I/O

### 16.1.1. μ-LAW ENCODE DECODE CHARACTERISTICS

| Normalized Encode Decision Levels | Digital Code | | | | | | | | Normalized Decode Levels |
|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | Sign | Chord | Chord | Chord | Step | Step | Step | Step | |
| | | | | | | | | | |
| 8159 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8031 |
| 7903<br>: | | | | | | | | | : |
| 4319 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 4191 |
| 4063<br>: | | | | | | | | | : |
| 2143 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 2079 |
| 2015 | | | | | | | | | : |
| : | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1023 |
| 1055 | | | | | | | | | : |
| 991 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 495 |
| :<br>511 | | | | | | | | | : |
| 479 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 231 |
| :<br>239 | | | | | | | | | : |
| 223 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 99 |
| : | | | | | | | | | : |
| 103<br>95 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 33 |
| :<br>35 | | | | | | | | | : |
| 31 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 2 |
| : | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 3<br>1<br>0 | | | | | | | | | |

Notes:

Sign bit = 0 for negative values, sign bit = 1 for positive values

### 16.2. A-LAW ENCODE DECODE CHARACTERISTICS

| Normalized Encode Decision Levels | Digital Code | | | | | | | | Normalized Decode Levels |
|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | Sign | Chord | Chord | Chord | Step | Step | Step | Step | |
| 4096<br>3968<br>:<br>2176<br>2048<br>:<br>1088<br>1024<br>:<br>544<br>512<br>:<br>272<br>256<br>:<br>136<br>128<br>:<br>68<br>64<br>:<br>2<br>0 | | | | | | | | | |
| | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 4032 |
| | | | | | | | | | : |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 2112 |
| | | | | | | | | | : |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1056 |
| | | | | | | | | | : |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 528 |
| | | | | | | | | | : |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 264 |
| | | | | | | | | | : |
| | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 132 |
| | | | | | | | | | : |
| | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 66 |
| | | | | | | | | | : |
| | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| | | | | | | | | | |

Notes:

1. Sign bit = 0 for negative values, sign bit = 1 for positive values
2. Digital code includes inversion of all even number bits

### 16.3. μ-LAW / A-LAW CODES FOR ZERO AND FULL SCALE

| Level | μ-Law | | | A-Law | | |
|---|---|---|---|---|---|---|
| | Sign bit (D7) | Chord bits (D6,D5,D4) | Step bits (D3,D2,D1,D0) | Sign bit (D7) | Chord bits (D6,D5,D4) | Step bits (D3,D2,D1,D0) |
| + Full Scale | 1 | 000 | 0000 | 1 | 010 | 1010 |
| + Zero | 1 | 111 | 1111 | 1 | 101 | 0101 |
| - Zero | 0 | 111 | 1111 | 0 | 101 | 0101 |
| - Full Scale | 0 | 000 | 0000 | 0 | 010 | 1010 |

### 16.3.1. µ-LAW / A-LAW CODES FOR 0DBM0 OUTPUT (DIGITAL MILLIWATT)

| Sample | µ-Law | | | A-Law | | |
|---|---|---|---|---|---|---|
| | Sign bit (D7) | Chord bits (D6,D5,D4) | Step bits (D3,D2,D1,D0) | Sign bit (D7) | Chord bits (D6,D5,D4) | Step bits (D3,D2,D1,D0) |
| 1 | 0 | 001 | 1110 | 0 | 011 | 0100 |
| 2 | 0 | 000 | 1011 | 0 | 010 | 0001 |
| 3 | 0 | 000 | 1011 | 0 | 010 | 0001 |
| 4 | 0 | 001 | 1110 | 0 | 011 | 0100 |
| 5 | 1 | 001 | 1110 | 1 | 011 | 0100 |
| 6 | 1 | 000 | 1011 | 1 | 010 | 0001 |
| 7 | 1 | 000 | 1011 | 1 | 010 | 0001 |
| 8 | 1 | 001 | 1110 | 1 | 011 | 0100 |

## 16.4. 16-BIT LINEAR PCM CODES FOR ZERO AND FULL SCALE

| Level | Sign bit | Magnitude Bits |
|---|---|---|
| + Full Scale | 0 | 111.1111 1111 1111 |
| + One Step | 0 | 000 0000 0000 0001 |
| Zero | 0 | 000 0000 0000 0000 |
| - One Step | 1 | 111 1111 1111 1111 |
| - Full Scale | 1 | 000 0000 0000 0000 |

## 16.5. 16-BIT LINEAR PCM CODES FOR 1 KHZ DIGITAL MILLIWATT

| Phase | Sign bit | Magnitude Bits |
|---|---|---|
| π / 8 | 0 | 010 0001 1110 0011 |
| 3 π / 8 | 0 | 101 0001 1101 0000 |
| 5 π / 8 | 0 | 101 0001 1101 0000 |
| 7 π / 8 | 0 | 010 0001 1110 0011 |
| 9 π / 8 | 1 | 101 1110 0001 1100 |
| 11 π / 8 | 1 | 010 1110 0010 1111 |
| 13 π / 8 | 1 | 010 1110 0010 1111 |
| 15 π / 8 | 1 | 101 1110 0001 1100 |

## 17. TYPICAL APPLICATION CIRCUITS

### 17.1. DC/DC APPLICATION

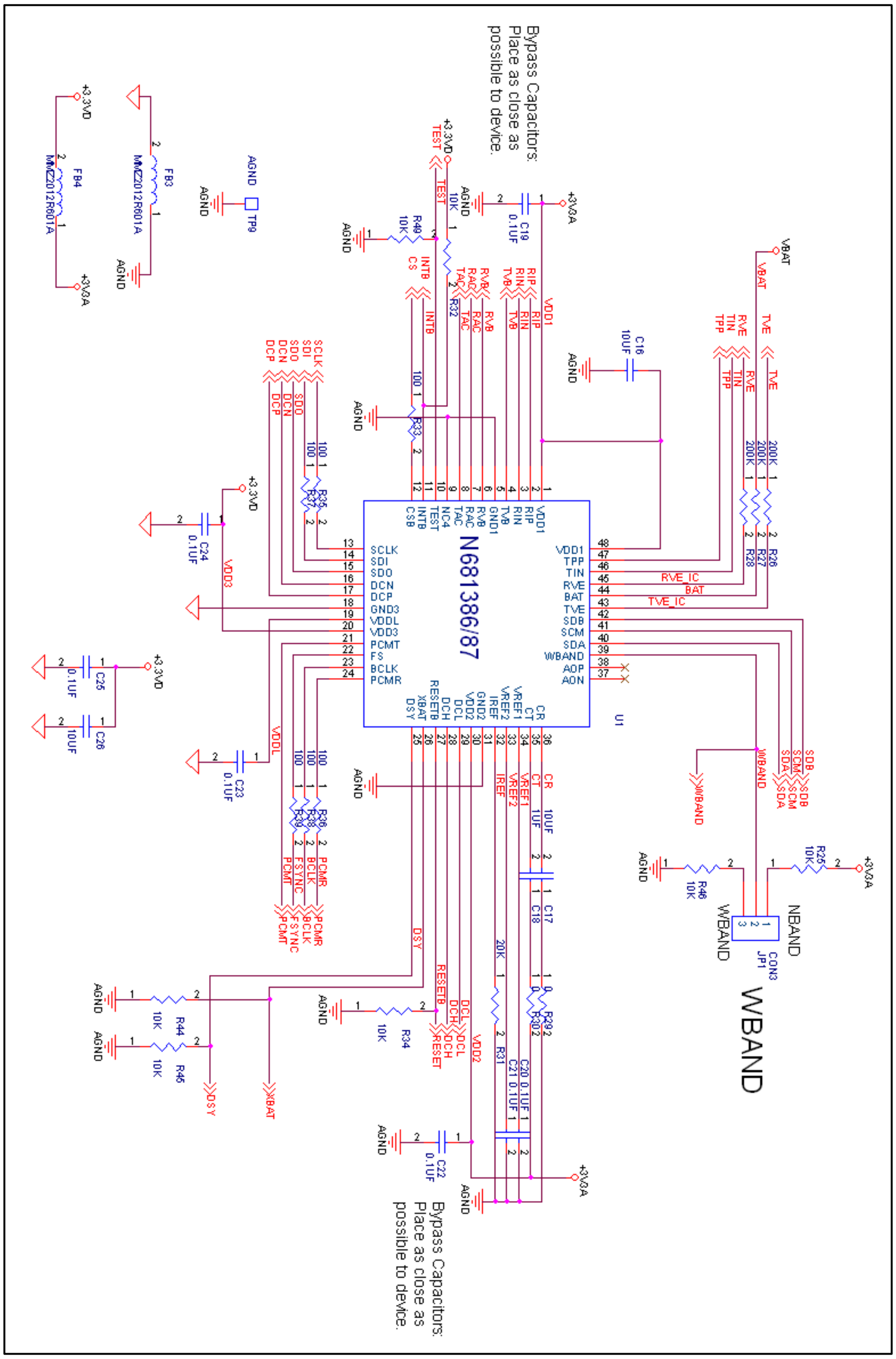


Figure 49: Typical Application Block Diagram

### 17.2. DISCRETE LINE DRIVER

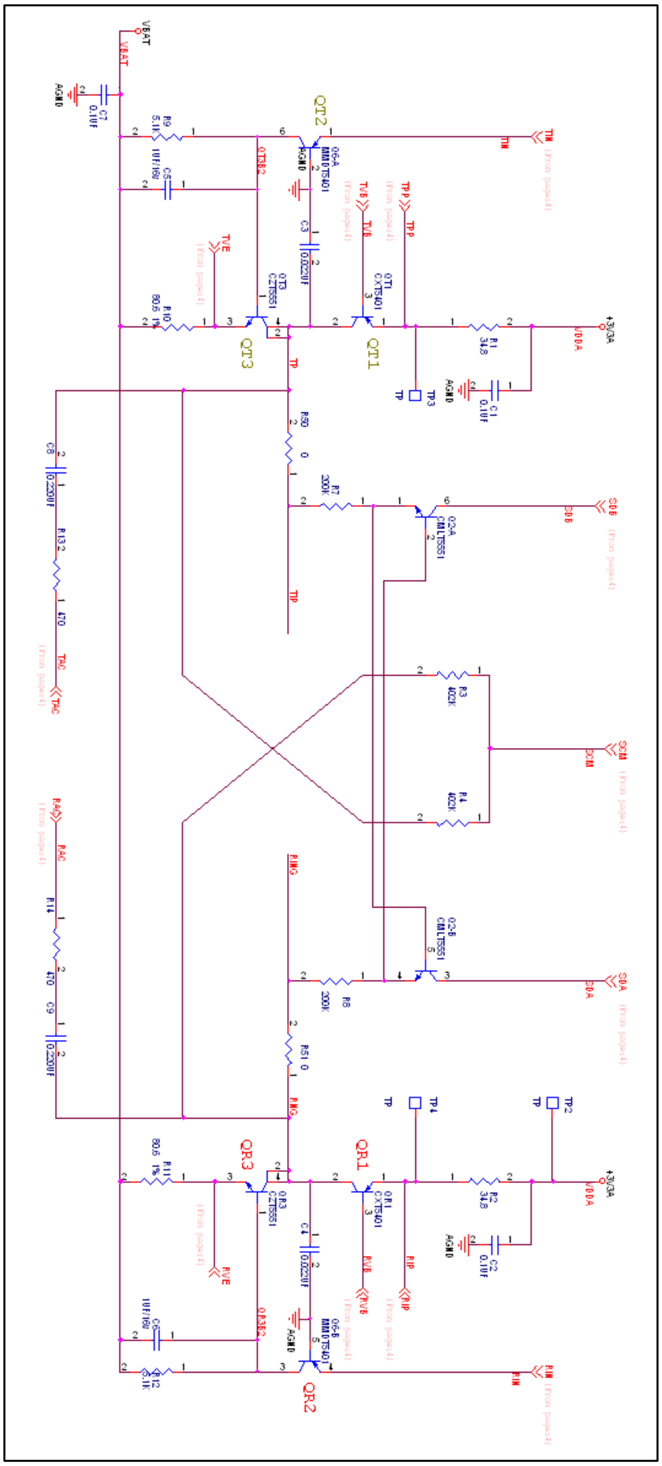


Figure 50: Discrete Line-driver

### 17.3. DC DC

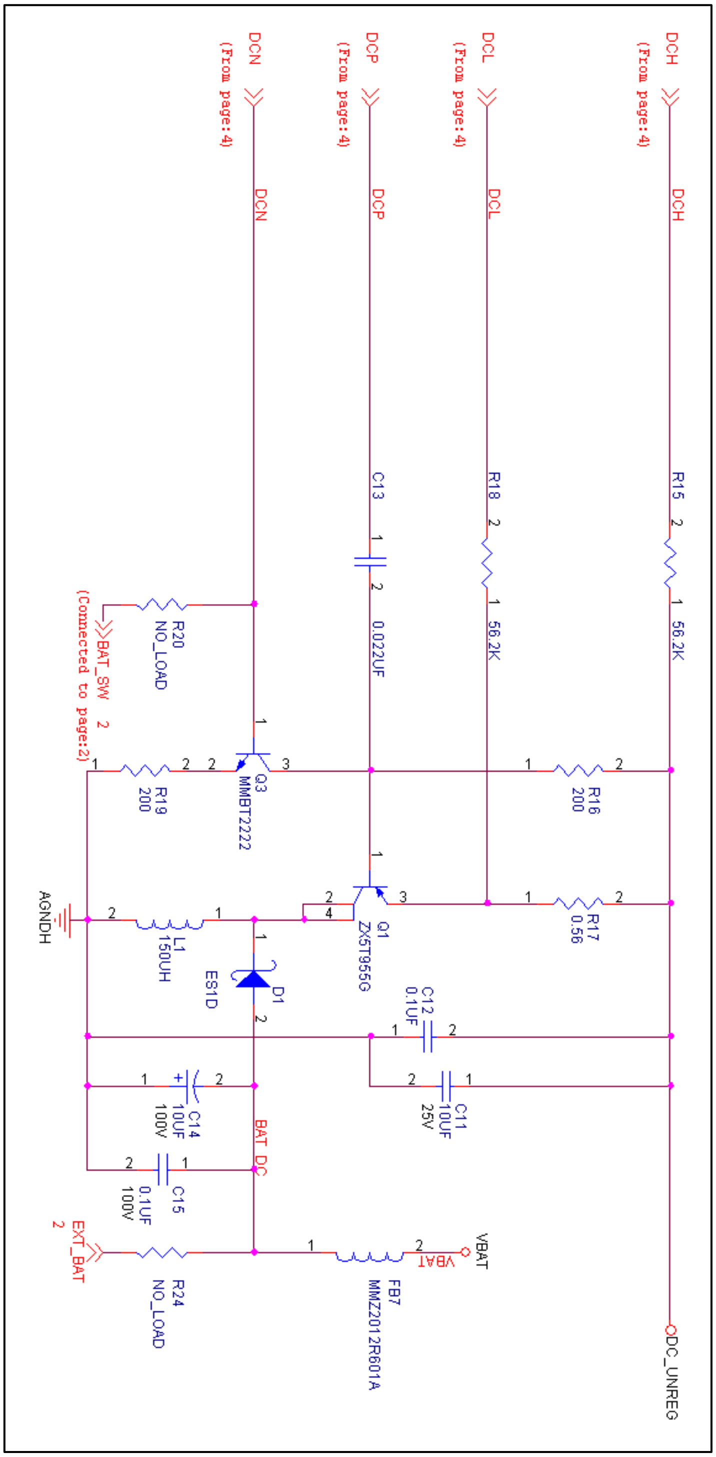


Figure 51: Inductor based circuit 12V supply

### 17.4. TRIPLE BATTERY SWITCH APPLICATION

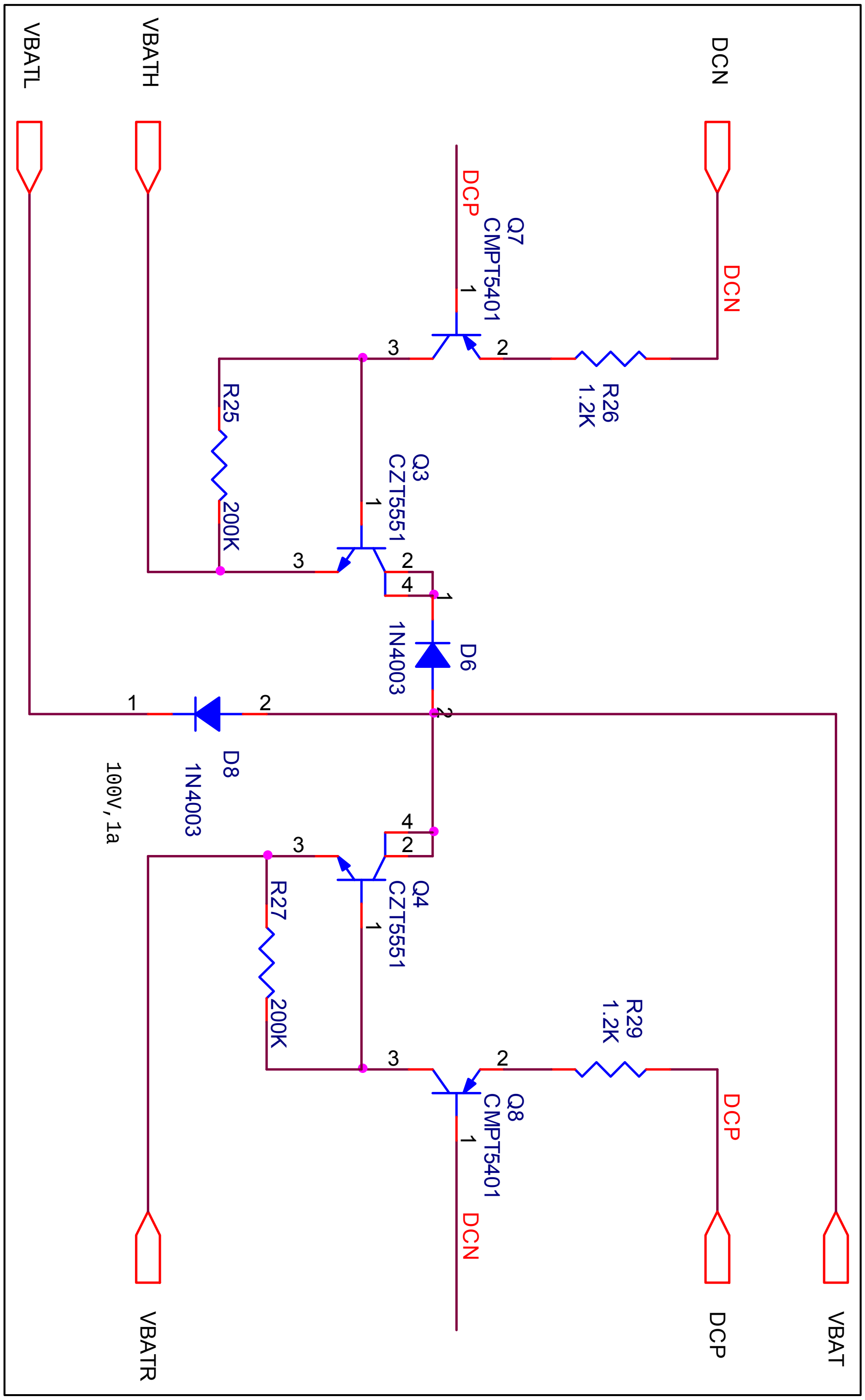


Figure 52: Triple Battery based Switch 1

### 17.5. N681386/87 DCDC APPLICATION USE WITH SLFC N681622

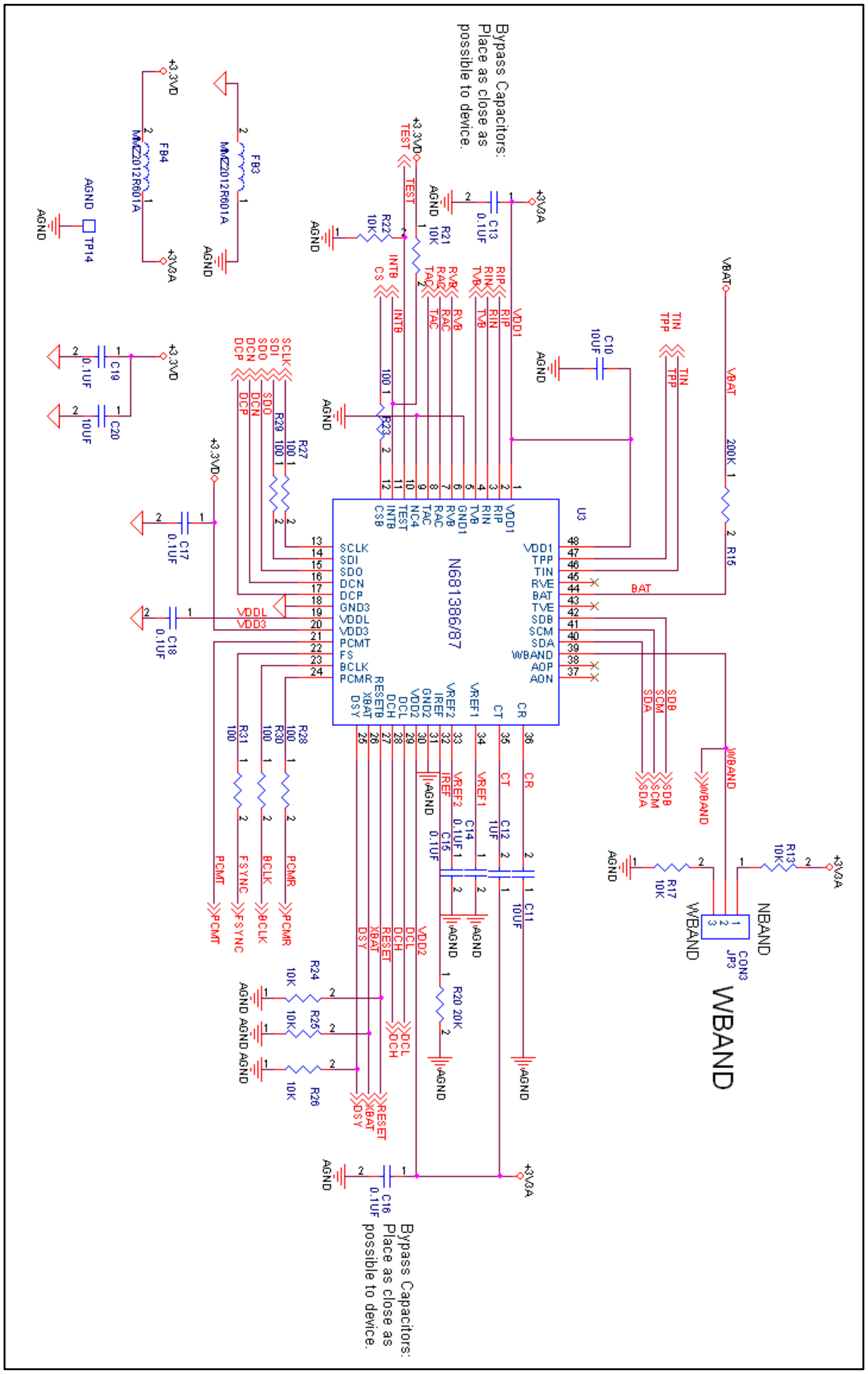


Figure 53: N681386/87 Pro-X Application diagram to be used with N681622

### 17.6. N681622 LINEFEED CIRCUIT

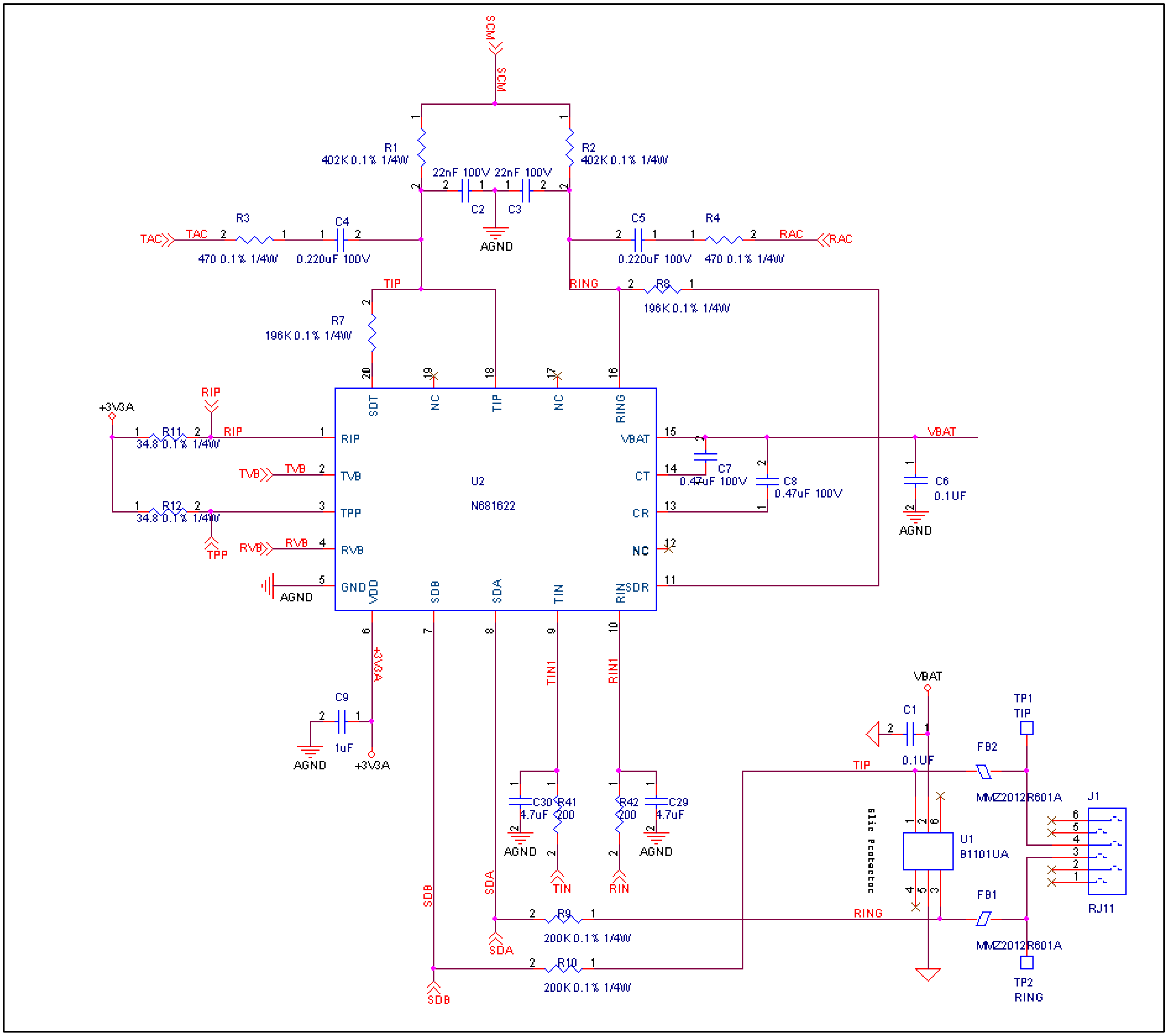
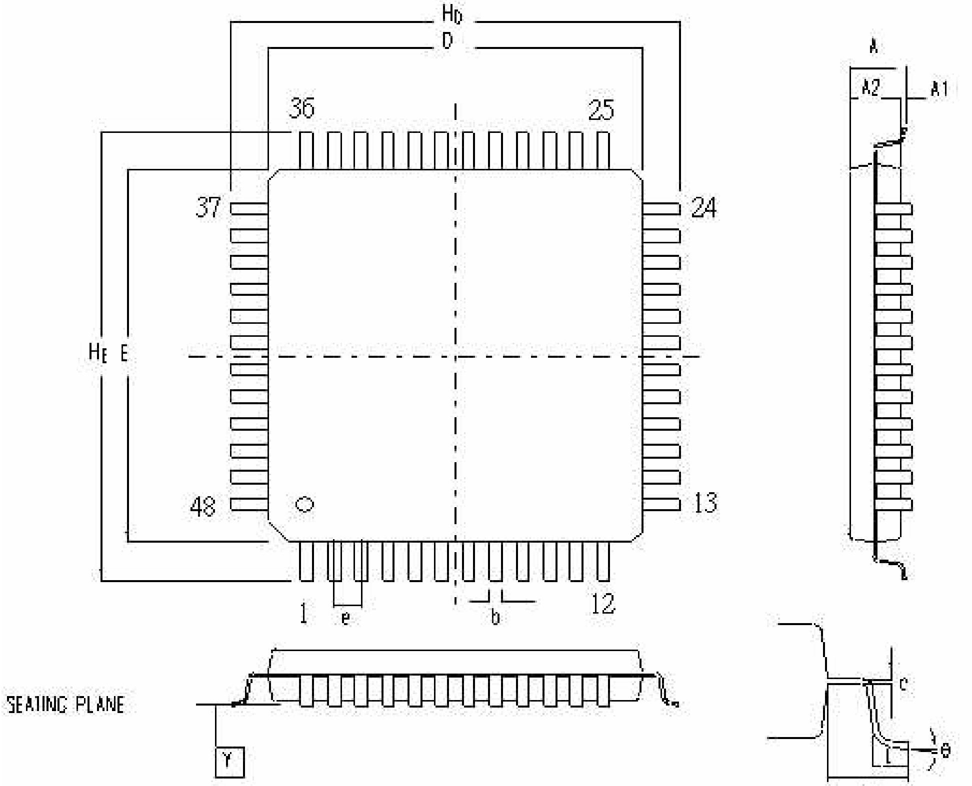


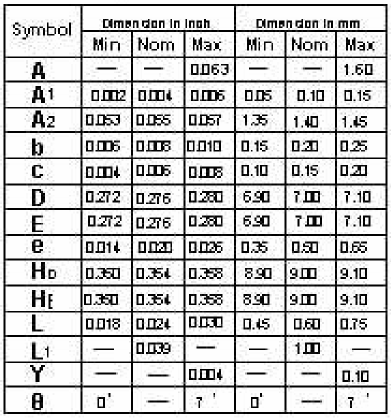
Figure 54: N681622 Linefeed circuit

## 18. PACKAGE SPECIFICATION

### 18.1. LQFP-48 (10X10X1.4mm FOOTPRINT 2.0mm)

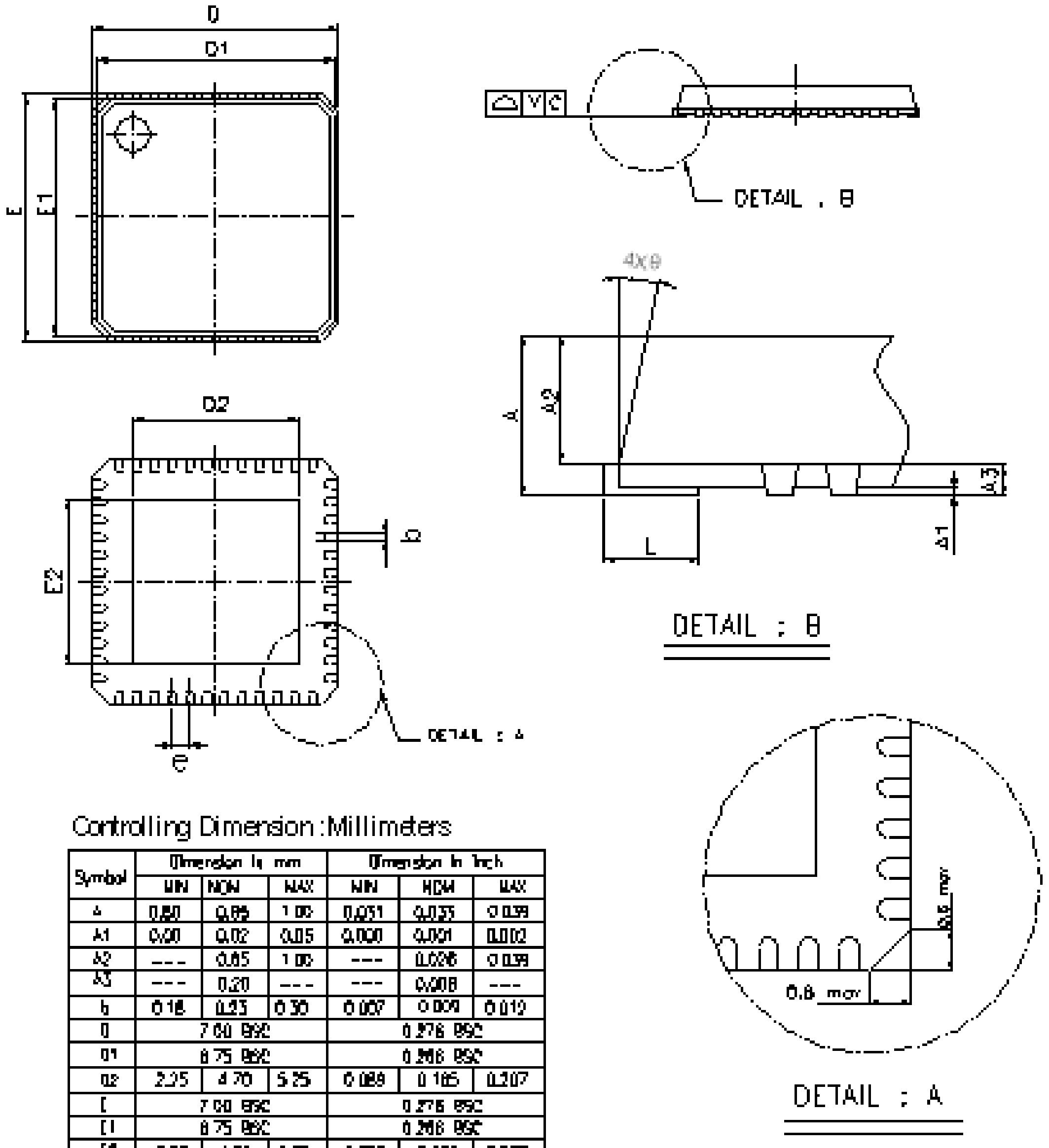


**Controlling dimension : Millimeters**



| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 0.063 | — | — | 1.60 |
| $A_1$ | 0.002 | 0.004 | 0.006 | 0.05 | 0.10 | 0.15 |
| $A_2$ | 0.053 | 0.055 | 0.057 | 1.35 | 1.40 | 1.45 |
| b | 0.006 | 0.008 | 0.010 | 0.15 | 0.20 | 0.25 |
| c | 0.004 | 0.006 | 0.008 | 0.10 | 0.15 | 0.20 |
| D | 0.272 | 0.276 | 0.280 | 6.90 | 7.00 | 7.10 |
| E | 0.272 | 0.276 | 0.280 | 6.90 | 7.00 | 7.10 |
| e | 0.014 | 0.020 | 0.026 | 0.35 | 0.50 | 0.65 |
| $H_D$ | 0.350 | 0.354 | 0.358 | 8.90 | 9.00 | 9.10 |
| $H_E$ | 0.350 | 0.354 | 0.358 | 8.90 | 9.00 | 9.10 |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| $L_1$ | — | 0.039 | — | — | 1.00 | — |
| Y | — | — | 0.004 | — | — | 0.10 |
| θ | 0° | — | 7° | 0° | — | 7° |

### 18.2. QFN-48

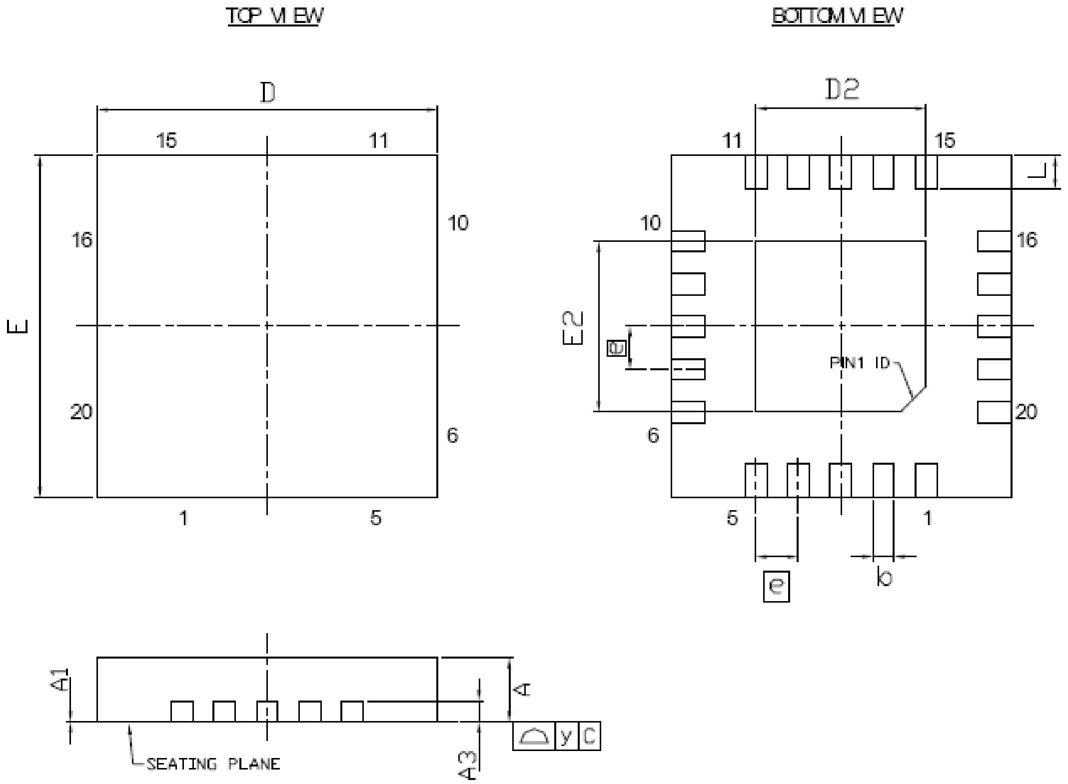


Controlling Dimension : Millimeters

| Symbol | Dimension In mm | | | Dimension In Inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 1.00 | 0.031 | 0.033 | 0.039 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A2 | --- | 0.65 | 1.00 | --- | 0.026 | 0.039 |
| A3 | --- | 0.20 | --- | --- | 0.008 | --- |
| b | 0.18 | 0.23 | 0.30 | 0.007 | 0.009 | 0.012 |
| D | 7.00 BSC | | | 0.276 BSC | | |
| D1 | 6.75 BSC | | | 0.266 BSC | | |
| D2 | 2.25 | 4.70 | 5.25 | 0.089 | 0.185 | 0.207 |
| E | 7.00 BSC | | | 0.276 BSC | | |
| E1 | 6.75 BSC | | | 0.266 BSC | | |
| E2 | 2.25 | 4.70 | 5.25 | 0.089 | 0.185 | 0.207 |
| e | 0.5 BSC | | | 0.020 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| θ | 0° | --- | 12° | 0° | --- | 12° |
| y | --- | --- | 0.08 | --- | --- | 0.003 |

* D2,* E2 :By die size difference

### 18.3. QFN 20L 4X4 mm$^2$, PITCH:0.50 mm



Controlling Dimension :Millimeters

| SYMBOL | DIMENSION (MM) | | | DIMENSION (Inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.02756 | 0.02953 | 0.03150 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.0079 | 0.00197 |
| A3 | 0.203 REF | | | 0.0079 REF | | |
| b | 0.18 | 0.25 | 0.30 | 0.00709 | 0.00984 | 0.01181 |
| D | 3.90 | 4.00 | 4.10 | 0.1535 | 0.1575 | 0.1614 |
| D2 | 1.90 | 2.00 | 2.10 | 0.0748 | 0.0787 | 0.0827 |
| E | 3.90 | 4.00 | 4.10 | 0.1535 | 0.1575 | 0.1614 |
| E2 | 1.90 | 2.00 | 2.10 | 0.0748 | 0.0787 | 0.0827 |
| e | 0.50 BSC | | | 0.01969 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.01181 | 0.01574 | 0.01969 |
| y | 0.08 | | | 0.00315 | | |

Note:D2,E2 by die size difference .

## 19. ORDERING INFORMATION

Nuvoton Part Number Description

N681386/87_ _

Product Family

**Package Material:**
**G** **=** Pb-free Package

**Package Type:**
**D** = LQFP-48
**Y** = QFN-48

When ordering N681386/87 series devices, please refer to the following part numbers:

| Part Number | Temp Range (°C) | Package | Package Material |
|---|---|---|---|
| N681386DG<br>N681387DG | -40 to 85 | 48-LQFP | Pb-Free |
| N681386YG<br>N681387YG | -40 to 85 | 48-QFN | Pb-Free |

N681622_ _

Product Family

**Package Material:**
**G** **=** Pb-free Package

**Package Type:**
**Y** = QFN-20

When ordering N681622 series devices, please refer to the following part numbers:

| Part Number | Temp Range (°C) | Package | Package Material |
|---|---|---|---|
| N681622YG | -40 to 85 | 20-QFN | Pb-Free |

## 20. VERSION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| V0.85 | January 2010 | | Register 0x0F deleted from the document. |
| | | 1 | Package info updated |
| | | 33 | Table 10 updated |
| | | 37 | Table 14 has been deleted from the document |
| | | 50 | Figure 17 updated |
| | | 52 | Equations updated. Table 22 has been deleted from the document |
| | | 62 | External battery switching detail updated |
| | | 67 | General Description for N681622 updated |
| | | 77 & 96 | Register table address 0x24 updated |
| | | 86 | Register 0x10[1] description updated |
| | | 88 & 77 | Register 0x14 updated |
| | | 96 | Register 0x26 info updated |
| | | 102 -103 | Registers 0x36, 0x37, and 0x38 units updated |
| | | 105 | Register 0x41 info updated |
| | | 134 | Register 0xB6 has been deleted from the document |
| | | 135 | Register info updated. Register 0xC0 bit description updated |
| V1.0 | January 2010 | 18 – 24 | Location of the tables were modified |
| | | 18 | Absolute Maximum Ratings table for N681622 updated |
| | | 20 | IPD and ISB maximum values updated |
| | | 21 | Supply parameter for SLFC updated |
| | | 31 | Tables 8 and 9 updated |
| | | 35 | Example updated |
| | | 36 | Table 15 updated |
| | | 40 | Table 15 updated |
| | | 49 | Register 0x60 and 0x61 updated |
| | | 56 | Impedance matching section updated |
| | | 59 | Diagnostics Support description updated |
| | | 64 | PCM Interface description updated |
| | | 67 | PLL and Prescaler in Wideband table updated |
| | | 74 | SPI 12-bits Read sequence diagram updated |
| | | 82 | Register 0x03 default updated |
| | | 85 | Register 0x06 and 0x07 updated |
| | | 86 | Register 0x10[1] description updated |
| | | 88 - 92 | Register 0x15 to 0x1F description updated |
| | | 89 | Register 0x15 to 0x1F updated |

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| | | 93 | Register 0x20 updated |
| | | 94 | Register 0x22 info updated |
| | | 107 | Register 0x43 info updated |
| | | 111 | Register 0x4C info updated |
| | | 115 | Register 0x5E to 0x61 info updated |
| | | 122 - 128 | Register 0x81 to 0x9C updated |
| | | 129 | Register 0x9D and 0x9E deleted from the document |
| | | 131 | Register 0xAD info updated |
| | | 136 | Register 0xDA and 0xDB deleted from the document |
| | | 139 | Register 0xF7 description updated |
| | | 153 | Application Diagrams updated |

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