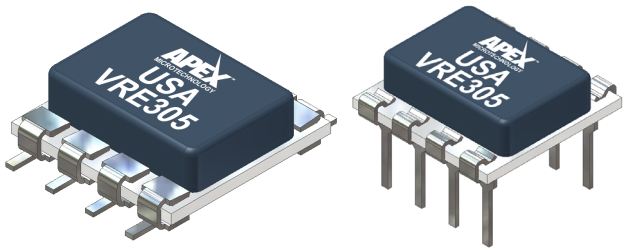
VRE305

Precision Voltage Reference

FEATURES

- +5 V Output, ± 0.5 mV (0.01%)
- Temperature Drift: 0.6 ppm/°C
- Low Noise: 3 μV_{P-P} (0.1-10 Hz)
- Industry Standard Pinout: 8-pin DIP or Surface Mount Package
- Excellent Line Regulation: 6 ppm/V Typical
- Output Trim Capability



APPLICATIONS

The VRE305 is recommended for use as a reference for 14, 16, or 18 bit D/A converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution A/D converters. The VRE305 offers superior performance over monolithic references.

DESCRIPTION

The VRE305 is a low cost, high precision +5 V reference. Packaged in an industry standard 8-pin DIP or SMT, the device is ideal for upgrading systems that use lower performance references.

The device provides ultrastable +5 V output with ±0.5 mV (0.01%) initial accuracy and a temperature coefficient of 0.6 ppm/°C. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE305 series the most accurate reference available in a standard 8-pin DIP or SMT.

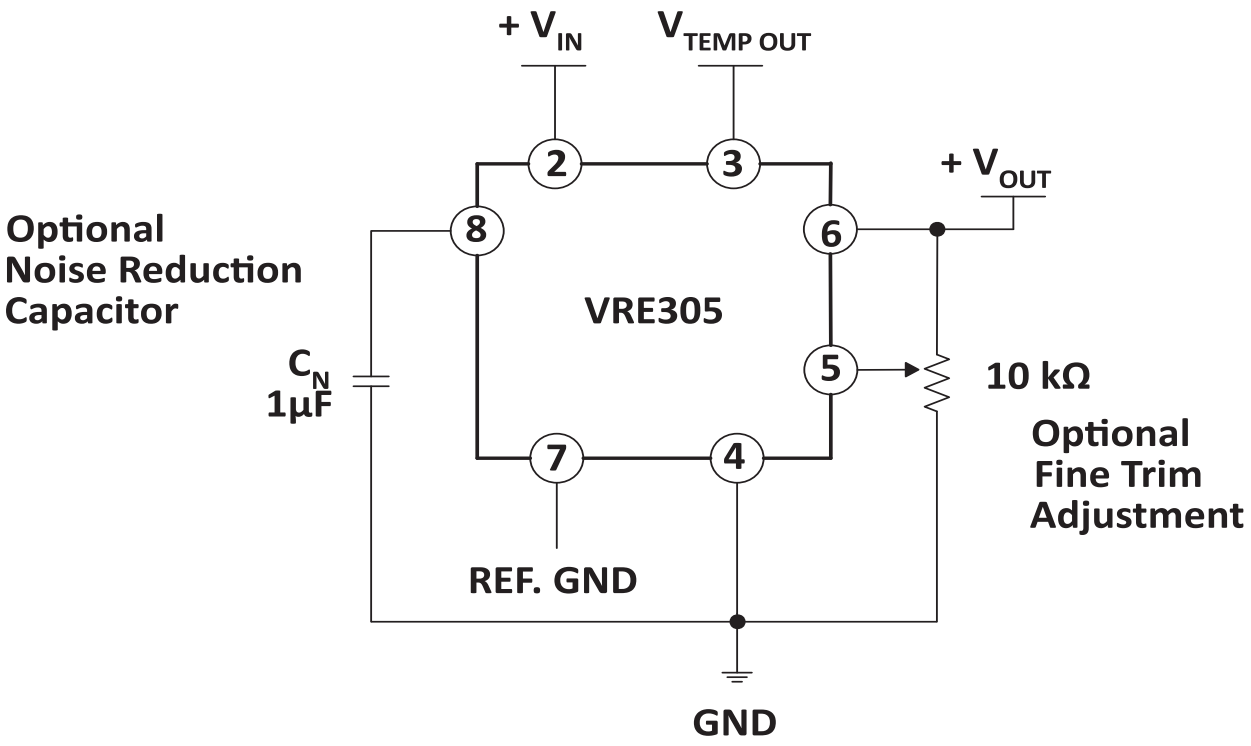
For enhanced performance, the VRE305 has an external trim option for users who want less than 0.01% initial error. For ultra low noise applications, an external capacitor can be attached between the noise reduction pin and the ground pin. A reference ground pin is provided to eliminate socket contact resistance errors.

SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/°C)	Temp Range (°C)	Package Options
VRE305AD	0.5	0.6	0°C to +70°C	DIP8 (KD)
VRE305AS	0.5	0.6	0°C to +70°C	SIP8 (GD)
VRE305CD	1.0	2.0	0°Cto +70°C	DIP8 (KD)
VRE305CS	1.0	2.0	0°C to +70°C	SIP8 (GD)

TYPICAL CONNECTION

Figure 1: Typical Connection



PIN DESCRIPTIONS

Pin Number	Name	Description
1	NC	No connection.
2	V_{IN}	The supply voltage connection.
3	TEMP	Provides voltage proportional to package temperature for monitoring purposes.
4	GND	Ground.
5	TRIM	Optional fine adjustment. Connect to a voltage divider between OUT and GND.
6	OUT	5 V output.
7	REF_GND	Provided for accurate ground sensing. Internally connected to GND.
8	NOISE	Optional noise reduction. Connect a 1µF capacitor between this pin and GND.

SPECIFICATIONS

V_{IN}= +15 V, T = +25°C, R_L = 10 kΩ unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS

Parameter	AS/AD			CS/CD			Units
	Min	Typ	Max	Min	Typ	Max	
Power Supply	+13.5	+15	+22	*	*	*	V
Operating Temperature	0		+70	*		*	°C
Storage Temperature	-65		+150	*		*	°C
Short Circuit Protection	Continuous			*			

ELECTRICAL SPECIFICATIONS

Parameter	AS/AD			CS/CD			Units
	Min	Typ	Max	Min	Typ	Max	
Output Voltage		+5.0			*		V
Temp. Sensor Voltage [1]		630			*		mV
Initial Error [2]			0.5			1.00	mV
Warmup Drift		1			3		ppm
T_{MIN} - T_{MAX} [3]			0.6			2.0	ppm/°C
Long-Term Stability		6			*		ppm/1000hrs.
Noise (0.1 - 10Hz) [4]		3			*		µVpp
Output Current	±10			*			mA
Line Regulation		6	10		*	*	ppm/V
Load Regulation		3			*		ppm/mA
Output Adjustment		10			*		mV
Power Supply Current, +PS [5]		5	7		*	*	mA

1. The temp. reference TC is 2.1 mV/ °C
2. The specified values are without external trim
3. The temperature coefficient (TC) is determined by the box method using the following formula:

$$TC = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

4. The specified values are without the external noise reduction capacitor.
5. The specified values are unloaded.

Note: * Same as AS/AD models.

TYPICAL PERFORMANCE GRAPHS

Figure 2: V_{OUT} vs. Temperature (VRE305A)

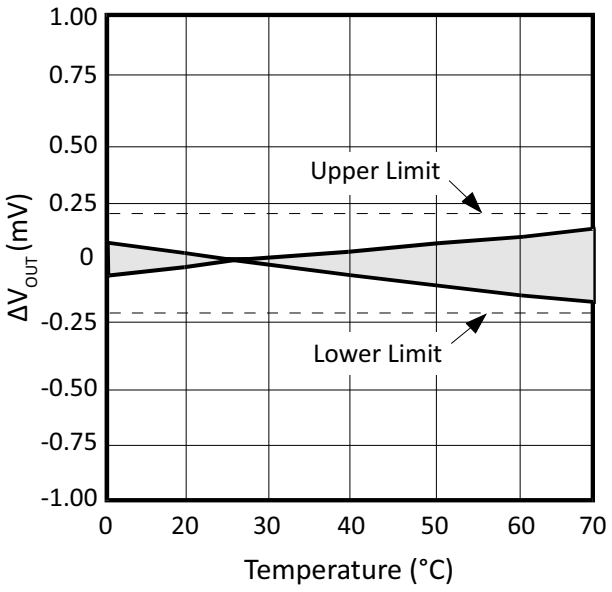


Figure 3: V_{OUT} vs. Temperature (VRE305C)

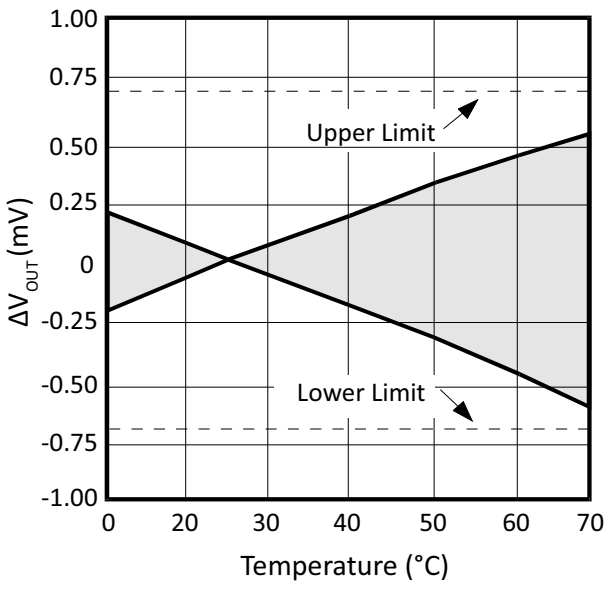


Figure 4: Power Supply Current vs. Temp.

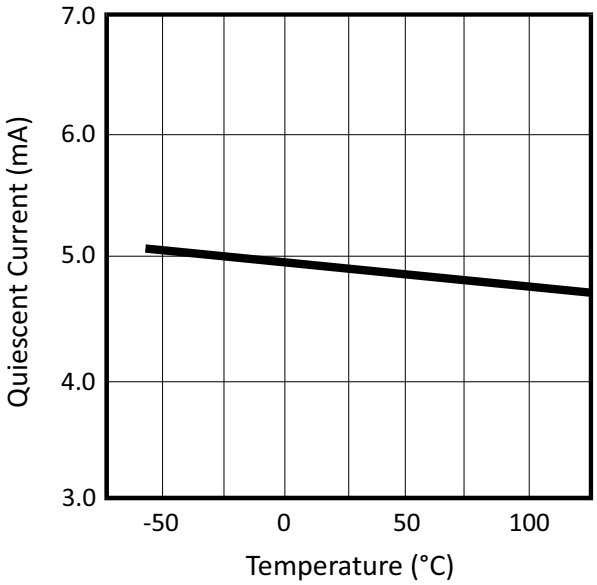


Figure 5: Junction Temp. Rise vs. Output Current

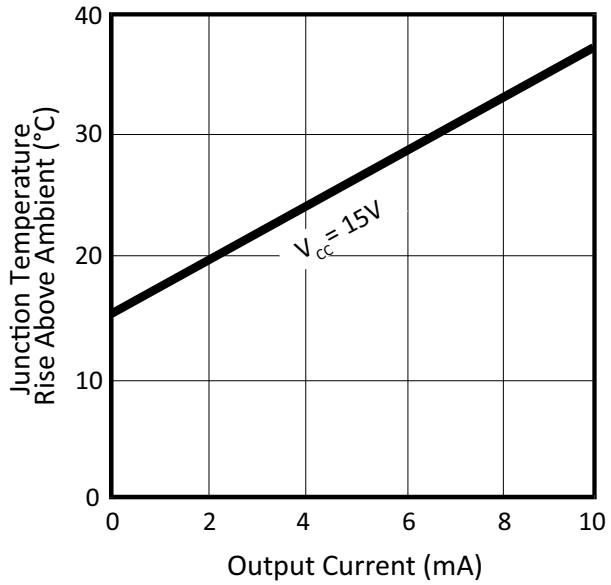
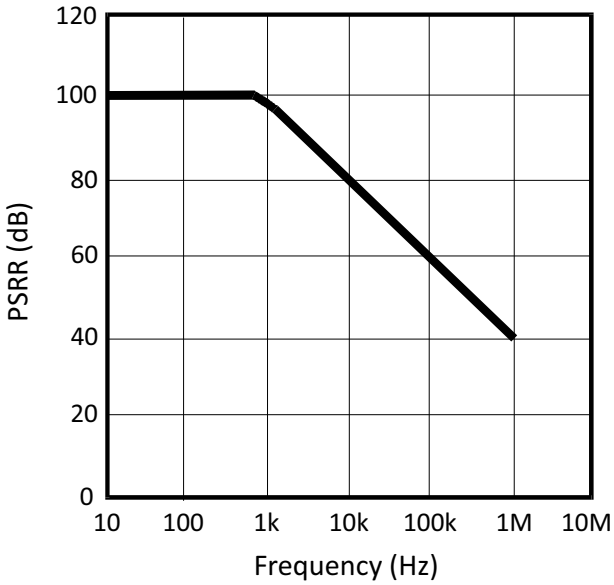
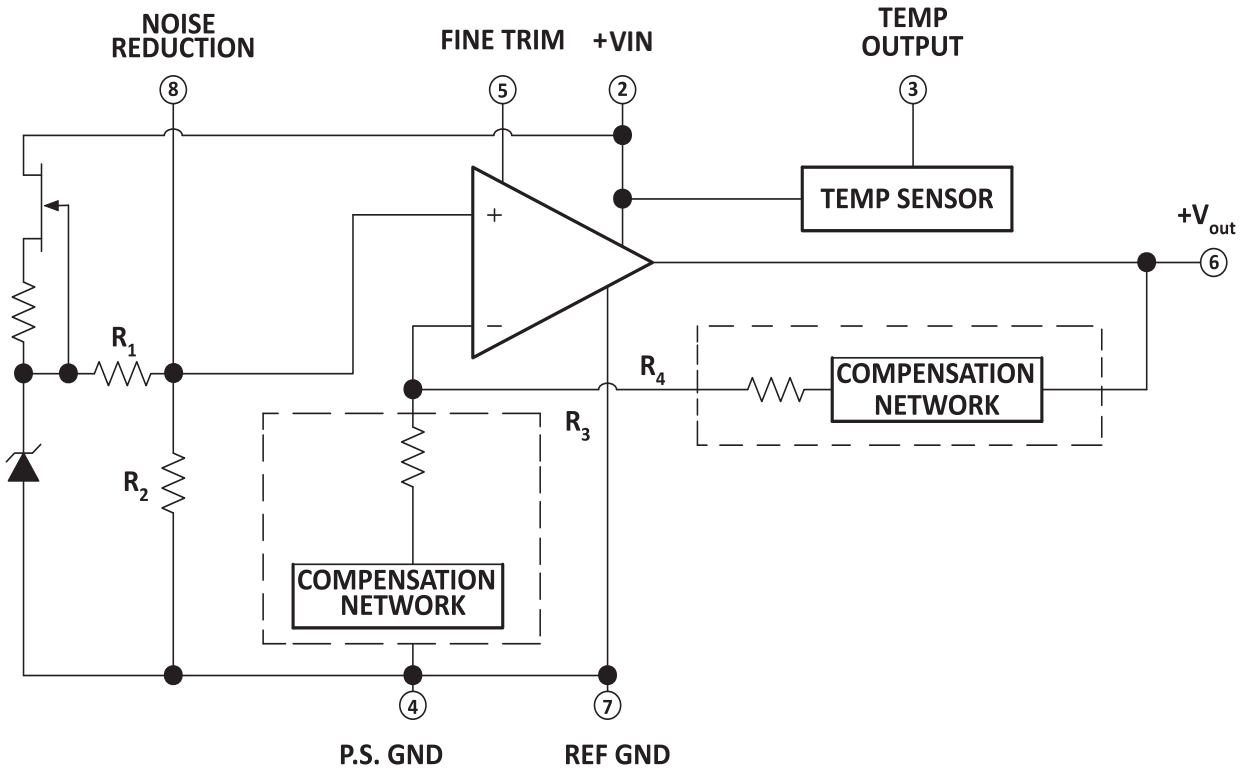


Figure 6: PSRR vs. Frequency



BLOCK DIAGRAM

Figure 7: Block Diagram



THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 8. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

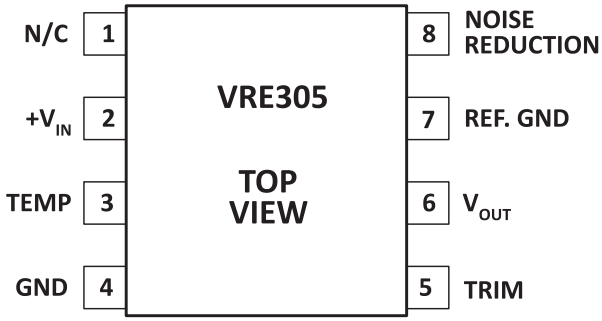
A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By adjusting the slope, a very stable voltage is produced over wide temperature ranges. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

The proper connection of the VRE305 series voltage references with the optional trim resistor for initial error and the optional capacitor for noise reduction is shown in figure 1. The VRE305 reference has the ground terminal brought out on two pins (pin 4 and pin 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop

across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20 ppm. By connecting pin 4 to the power supply ground and pin 7 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place, the contact resistance is sufficiently small that it does not effect performance. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

PIN CONFIGURATION

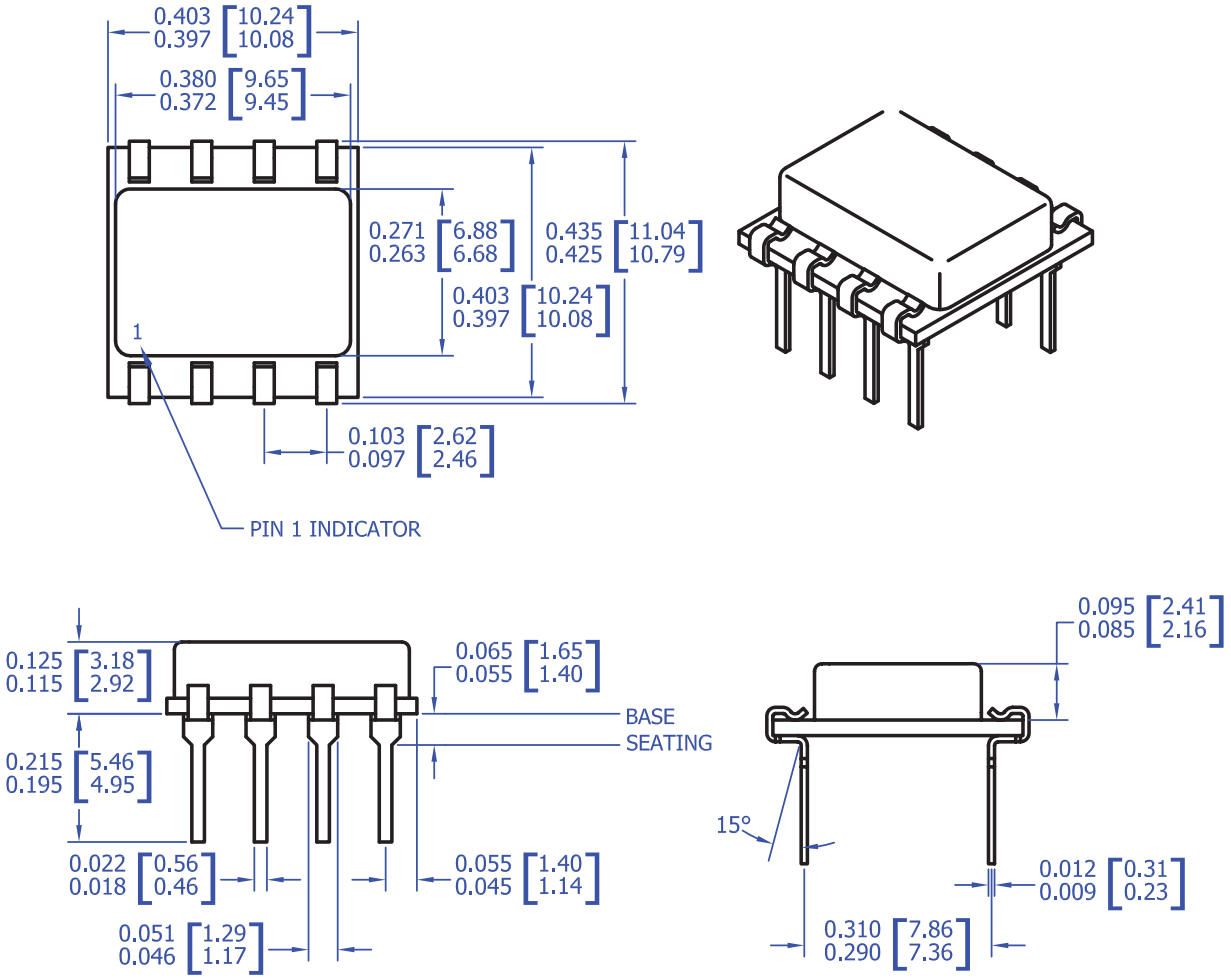
Figure 8: Pin Configuration



PACKAGE OPTIONS

Part Number	Apex Package Style	Description
VRE305AD	KD	8-pin DIP
VRE305AS	GD	8-pin Surface mount DIP
VRE305CD	KD	8-pin DIP
VR305CS	GD	8-pin Surface mount DIP

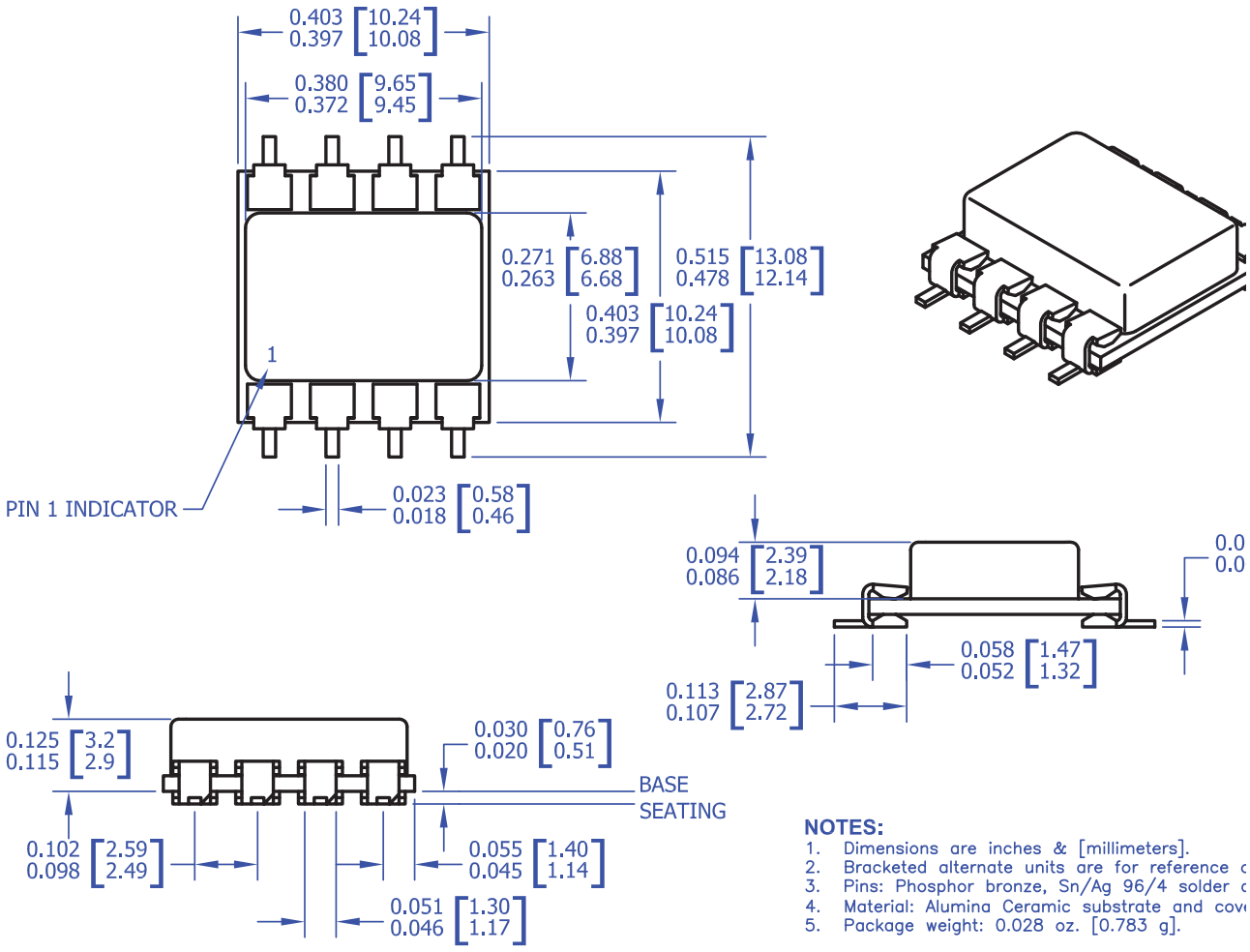
PACKAGE STYLE KD



NOTES:

1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Pins: Phosphor bronze, Sn/Ag 96/4 solder dipped.
4. Material: Alumina Ceramic substrate and cover.
5. Package weight: 0.028 oz. [0.785 g].

PACKAGE STYLE GD



NOTES:
1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference c
3. Pins: Phosphor bronze, Sn/Ag 96/4 solder c
4. Material: Alumina Ceramic substrate and cov
5. Package weight: 0.028 oz. [0.783 g].

NEED TECHNICAL HELP? CONTACT APEX SUPPORT!

For all Apex Microtechnology product questions and inquiries, call toll free 800-546-2739 in North America. For inquiries via email, please contact apex.support@apexanalog.com. International customers can also request support by contacting their local Apex Microtechnology Sales Representative. To find the one nearest to you, go to www.apexanalog.com