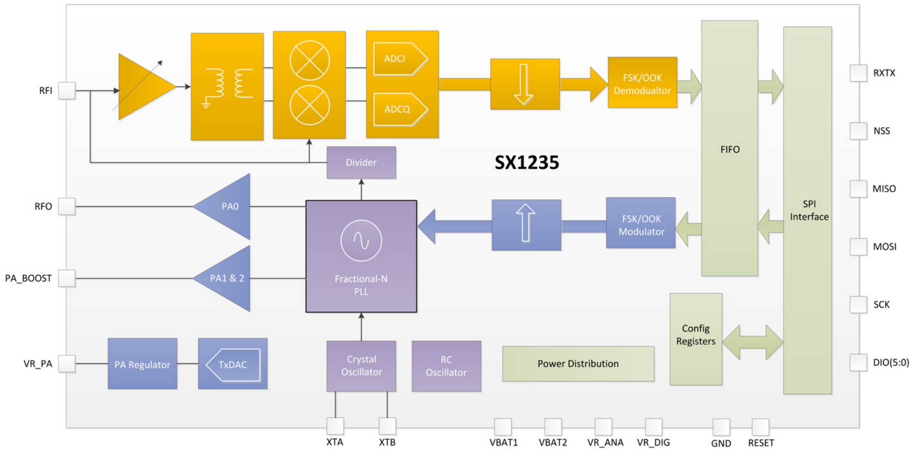
SX1235 Transceiver

EN300 220 Category 1 Compliant Transceiver



GENERAL DESCRIPTION

The SX1235 is a highly integrated RF transceiver optimized for operation compliant with ETSI EN 300 220 receiver category 1. In conjunction with an external SAW filter the SX1235 is designed to pass the category 1 testing with substantial regulatory margin, simplifying end-user production test requirements. The SX1235 retains the highly integrated architecture of the SX123x family, minimizing external components while delivering the highest level of performance. For hybrid systems with non category 1 elements within an alarm system the SX1235 offers the advantage of programmable narrow-band and wide-band communication modes without the need tomodify external components. This makes the SX1235 suitable for integrated home automation, security and alarm systems that require legacy compatibility.

APPLICATIONS

- Category 1 Social Alarm Systems
- Category 1 Fire, Smoke and Toxic Gas Detection
- Category 1 Lone Worker Systems
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control

MARKETS

- Optimised for the EN 300-220-1 Category 1
- North America: FCC Part 15 and Japan: ARIB T-108

KEY PRODUCT FEATURES

- High sensitivity: down to -123 dBm at 1.2 kbps
- High selectivity: 60 dB typ. ACR
- High linearity: 50 dB typ. of adjacent channel saturation
- 80 dB Blocking immunity, 100 dB with SAW
- Image rejection of over 45 dB
- Low current: Rx = 9.3 mA, 100nA register retention
- Programmable output power +20 dBm in 1 dB steps
- Optional high efficiency or fully regulated PA connections for reliable M2M performance and optimal battery lifetime
- Voltage operation from 1.8 to 3.7 V
- Narrowband integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK modulation
- Automated, fast frequency correction & timing recovery
- Over 115 dB Dynamic Range RSSI
- Packet engine with CRC 64 byte FIFO
- Preamble and RSSI based channel activity detection

ORDERING INFORMATION

Part Number	Package	Delivery	MOQ / Multiple
SX1235IMLTRT	QFN24	Tape & Reel	3000 pieces

Table of contents

Section **Page**

Table of contents

Section **Page**

Table of contents

Section **Page**

Table of contents

Section **Page**

List of Figures

List of Tables

This product datasheet contains a detailed description of the SX1235 performance and functionality. Please consult the Semtech website for the latest updates or errata.

1. General Description

The SX1235 is a single-chip integrated transceiver circuit that is optimized for EN 300 220-1 category 1 receiver applications. The fully integrated architecture of the transceiver is combined with an automated packet engine and top level sequencer. In conjunction with a 64 byte FIFO these automate the entire process of packet transmission, reception and acknowledgement without incurring the consumption penalty common to many transceivers that feature an on-chip MCUs. Being easily configurable, it greatly simplifies system design and reduces external MCU workload to a minimum. The small external BOM is limited to a quartz crystal frequency reference, passive decoupling, matching and filtering components.

SX1235 is intended for use as a high-performance, low-cost, FSK and OOK RF transceiver for robust, frequency agile, half-duplex, bidirectional RF links. Where stable and constant RF performance is required over the full operating range of the device down to 1.8 V the receiver and PA are fully regulated. For transmit intensive applications - a high efficiency PA can be selected to optimize the current consumption.

The SX1235 features high receiver sensitivity and low receive current, equating to a high link budget, 143dB (-123dBm sensitivity in conjunction with +20dBm Pout) and long battery life. The SX1235 complies with both ETSI and FCC regulatory requirements and is available in a 5 x 5 mm QFN 24 lead package.

1.1. Simplified Block Diagram

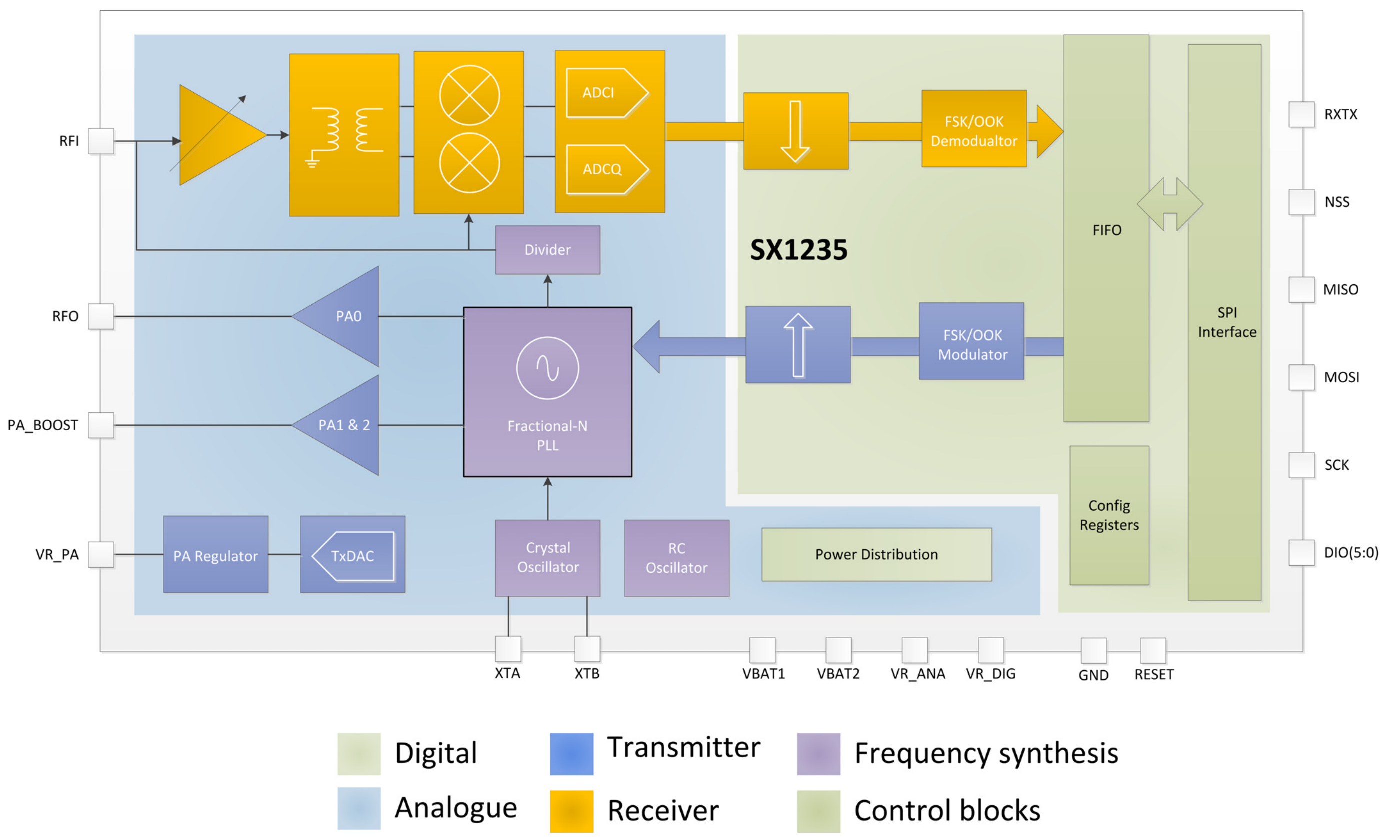


Figure 1. Block Diagram

1.2. Pin and Marking Diagram

The following diagram shows the pin arrangement of the QFN package, top view.

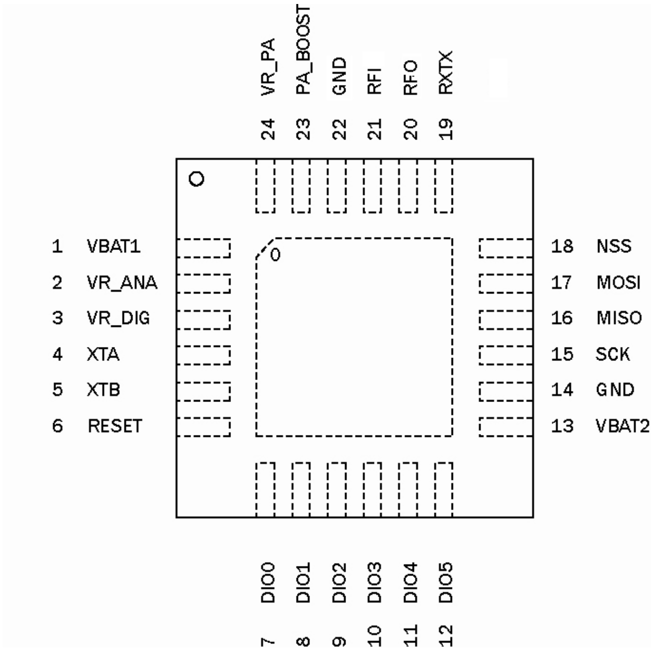


Figure 2. Pin Diagram

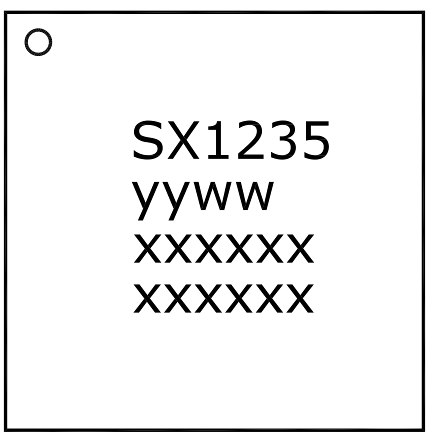


Figure 3. Marking Diagram

Notes yyww indicates the date code

xxxxxx.xxxxxx refers to the lot number

1.3. Pin Description

Table 1 SX1235 Pinouts

Number	Name	Type	Description
0	GROUND	-	Exposed ground pad
1	VBAT1	-	Supply voltage
2	VR_ANA	-	Regulated supply voltage for analogue circuitry
3	VR_DIG	-	Regulated supply voltage for digital blocks
4	XTA	I/O	XTAL connection or TCXO input
5	XTB	I/O	XTAL connection
6	RESET	I/O	Reset trigger input
7	DIO0	I/O	Digital I/O, software configured
8	DIO1/DCLK	I/O	Digital I/O, software configured
9	DIO2/DATA	I/O	Digital I/O, software configured
10	DIO3	I/O	Digital I/O, software configured
11	DIO4	I/O	Digital I/O, software configured
12	DIO5	I/O	Digital I/O, software configured
13	VBAT2	-	Supply voltage
14	GND	-	Ground
15	SCK	I	SPI Clock input
16	MISO	O	SPI Data output
17	MOSI	I	SPI Data input
18	NSS	I	SPI Chip select input
19	RXTX	O	Rx/Tx switch control: high in Tx
20	RFO	O	RF output
21	RFI	I	RF input
22	GND	O	Ground
23	PA_BOOST	O	Optional high-power PA output
24	VR_PA	O	Regulated supply for the PA

2. Electrical Characteristics

2.1. ESD Notice

The SX1235 is a high performance radio frequency device. It satisfies:

- Class 2 of the JEDEC standard JESD22-A114-B (Human Body Model) on all pins.
- Class B of the JEDEC standard JESD22-A115-A (Machine Model) on all pins.
- Class IV of the JEDEC standard JESD22-C101C (Charged Device Model) on pins VR_ANA, VR_DIG, RFIO, PA_BOOST, VR_PA, Class III on all other pins.

ESD Precautions must be taken to avoid permanent damage.

2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Temperature	-55	+115	° C
Tj	Junction temperature	-	+125	° C
Pmr	RF Input Level	-	+10	dBm

2.3. Operating Range

Table 3 Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply voltage	1.8	3.7	V
Top	Operational temperature range	-40	+85	°C
Clop	Load capacitance on digital ports	-	25	pF
ML	RF Input Level	-	+10	dBm

2.4. ETSI Category 1 Specification

Functionality that complies with the ETSI EN300 220 Category 1 is only possible in conjunction with an external SAW filter. To this end the specification of the SAW filter and the corresponding overall system performance is given here.

2.4.1. SAW Filter Specification

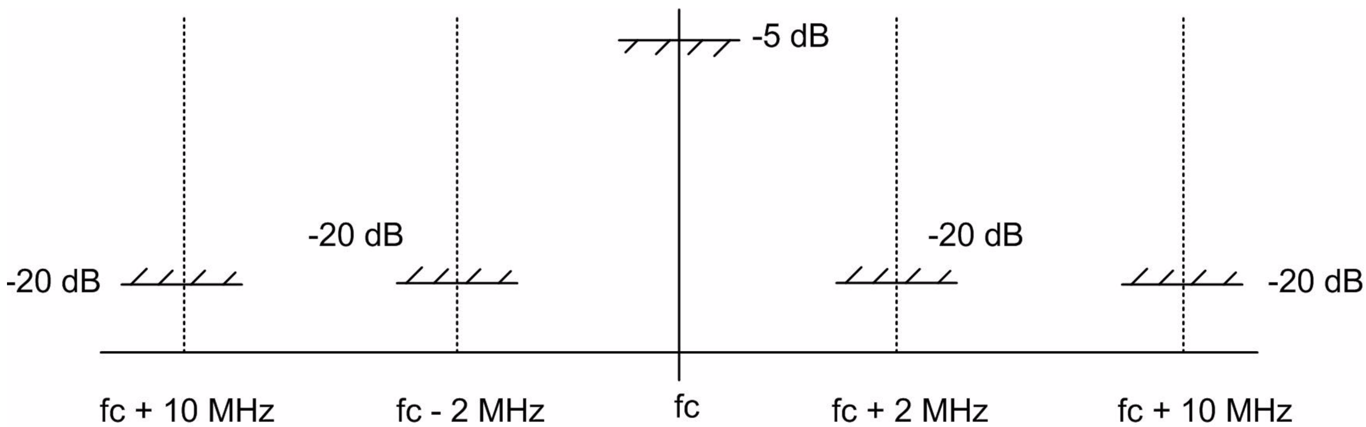


Figure 4. SAW Filter Performance Mask for Guaranteed Category 1 Compliance.

2.4.2. Category 1 Test Conditions

All receiver tests are performed with receiver bandwidth = 3.9 kHz (Single Side Bandwidth) as programmed in RegRxBw, an AFC SSBW of 7.81 kHz (corresponds to a declared 18.7 kHz $DSBW_{-20\ dB}$) receiving a 3 kbps PN15 sequence with 2 kHz frequency deviation for a BER of 1% (bit synchronizer is enabled). The RF centre frequency is 869.21250 MHz.

Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity and ACR tests is set to -103.3 dBm (3 dB above the calculated sensitivity limit of -106.3 dBm). Saturation testing in both the adjacent channel and higher offsets is performed at -63.3 dBm (43 dB above the sensitivity limit of -106.3 dBm). PLL settings are as described in Section 7.8.1.

The reference circuit of Section 2.4.6 is used with a SAW filter for all measurements that respects the mask requirements of Figure 4. Category 1 performances are specified with a regulated 3.3 V supply and for operation at room temperature only.

2.4.3. System Performance (Absolute Units) with a SAW as Defined in 2.4.1

Table 4 Absolute Performance of the SX1235 Reference Design.

Symbol	Description	Conditions	Min	Typ	Max	Unit
C1_RFS_F	RF Sensitivity FSK		-	-110	-	dBm
C1_ACR	Adjacent Channel Rejection	±25 kHz	-47	-44	-	dBm
C1_ACS	Adjacent Channel Saturation	±25 kHz	-16.3	-13.3	-	dBm
C1_BI	Blocking Immunity	±2 MHz ±10 MHz	-16.3 -14.3	-7.5 -7.5	- -	dBm dBm

Symbol	Description	Conditions	Min	Typ	Max	Unit
C1_BS	Receiver Saturation	±2 MHz ±10 MHz	-14.3 -9.3	-7.5 -7.5	- -	dBm dBm
C1_IMG	Image Rejection	(BW= 3.9 kHz or 7.81 kHz) -500 kHz	-58.3	-	-	dBm

2.4.4. System Performance (Regulatory Margin)

Table 5 SX1235 Reference Design Regulatory Margin to the Category 1 Test Limits.

Symbol	Description	Conditions	Min	Typ	Max	Unit
MC1_RFS_F	Margin to Sensitivity Limit		-	3.7	-	dB
MC1_ACR	Margin to ACR Limit	±25 kHz	3	6	-	dB
MC1_ACS	Margin to ACS Limit	±25 kHz	3	6	-	dB
MC1_BI	Margin to Blocking Limit	±2 MHz ±10 MHz	3 5	12.5 12.5	- -	dB dB
MC1_BS	Margin to Saturation Limit	±2 MHz ±10 MHz	5 10	12.5 12.5	- -	dB dB
MC1_IMG	Margin to Image Rejection Limit	(BS = 3.9 kHz or 7.81 kHz) -500 kHz	10	-	-	dB

2.4.5. Measurement Configuration for Category 1 Testing

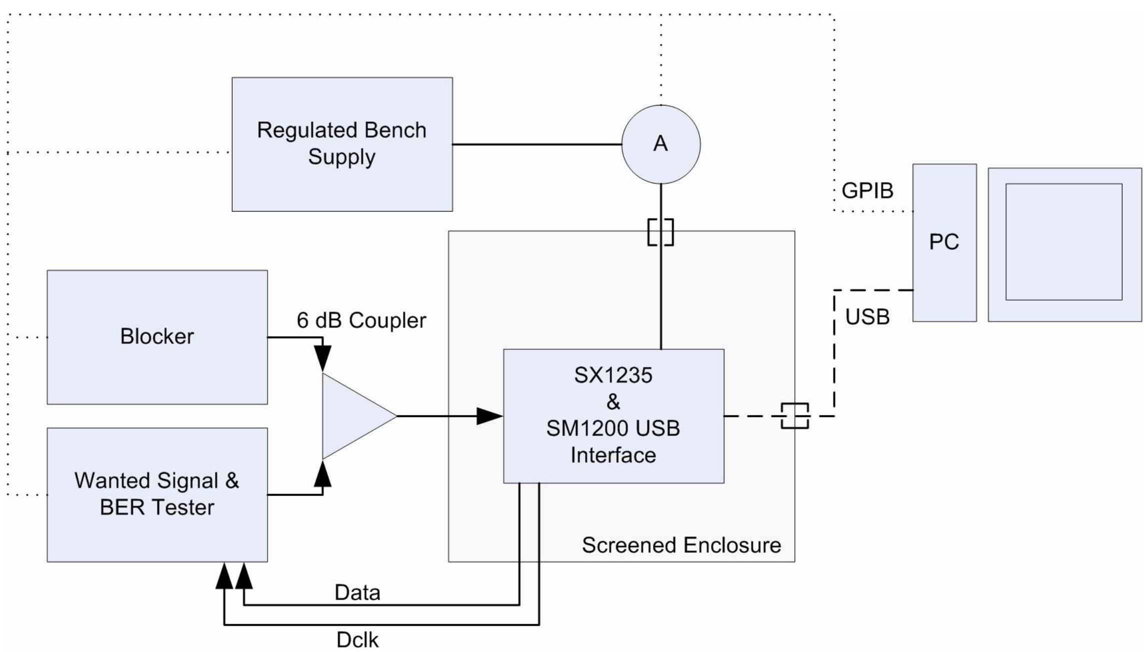


Figure 5. Measurement configuration used for testing of the SX1235 reference design.

2.4.6. 869 MHz Category 1 Reference Design Module SM1235

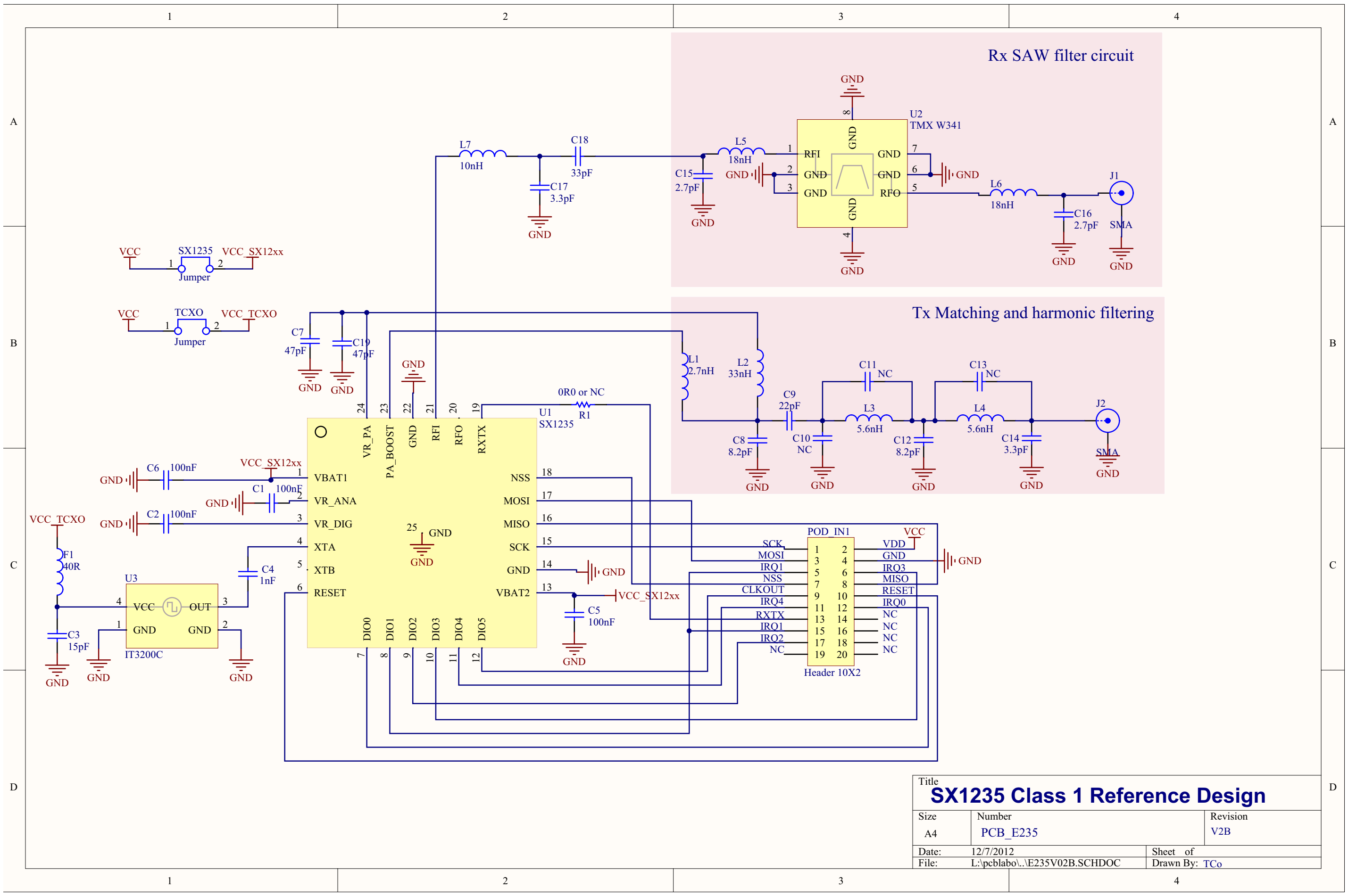


Figure 6. Circuit schematic of the SX1235 reference design used for regulatory testing.

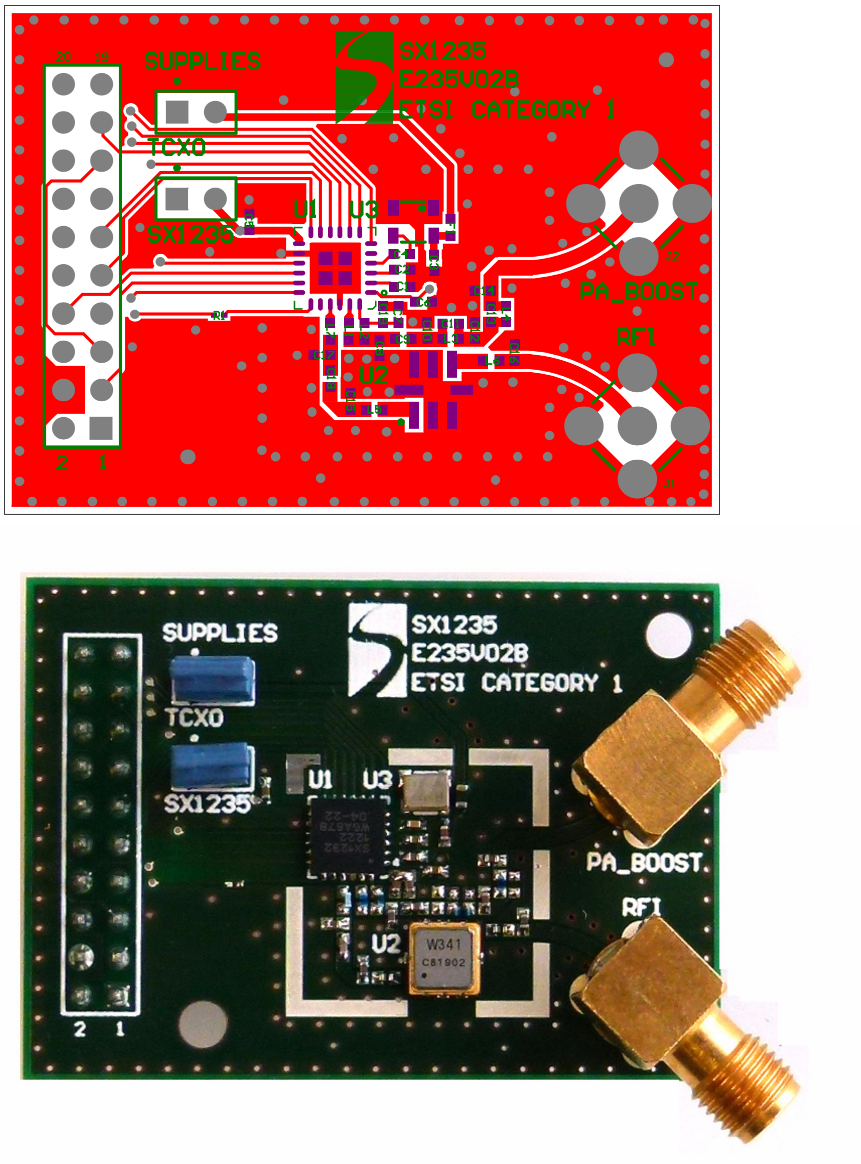


Figure 7. SX1235 Reference Design PCB Layout, Gives both +20 dBm RF Output Tx and Category 1 Rx.

2.5. Circuit Specification

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VBAT1= VBAT2 = VDD = 3.3 V, temperature = 25 °C, F_{XOSC} = 32 MHz, F_{RF} = 868 MHz, Pout = +13 dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kbps and terminated in a matched 50 ohm impedance, unless otherwise specified.

Note Unless otherwise specified, the performance in the 915 MHz band is identical.

2.5.1. Power Consumption

Table 6 Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in Sleep mode		-	0.1	1	uA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	-	1.2	-	uA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	-	1.3	1.5	mA
IDDFS	Supply current in Synthesizer mode	FSRx	-	4.5	-	mA
IDDR	Supply current in Receive mode	*LnaBoost* = 00	-	9.3	-	mA
IDDT	Supply current in Transmit mode with impedance matching	RFOP = +20 dBm, on PA_BOOST RFOP = +17 dBm, on PA_BOOST RFOP = +13 dBm, on RFO pin RFOP = + 7 dBm, on RFO pin	- - - -	125 93 28 18	- - - -	mA mA mA mA

2.5.2. Frequency Synthesis

Table 7 Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer frequency range	Programmable	862	-	1020	MHz
FXOSC	Crystal oscillator frequency	See section 7.1	-	32	-	MHz
TS_OSC	Crystal oscillator wake-up time	With crystal specified in section 7.1	-	250	-	us
TS_FS	Frequency synthesizer wake-up time to Pll Lock signal	From Standby mode	-	60	-	us
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target frequency	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	- - - - - - -	20 20 50 50 50 50 50	- - - - - - -	us us us us us us us
FSTEP	Frequency synthesizer step	$FSTEP = FXOSC/2^{19}$	-	61.0	-	Hz
FRC	RC Oscillator frequency	After calibration	-	62.5	-	kHz

BRF	Bit rate, FSK	Programmable values (1)	1.2	-	300	kbps
BRO	Bit rate, OOK	Programmable	1.2	-	32.768	kbps
BRA	Bit Rate Accuracy	ABS (wanted BR - available BR)	-	-	250	ppm
FDA	Frequency deviation, FSK (1)	Programmable FDA + BRF/2 =< 250 kHz	0.6	-	200	kHz

Note For Maximum Bit rate the maximum modulation index is 1.

2.5.3. Receiver

All receiver tests are performed with RxBw = 10 kHz (Single Side Bandwidth) as programmed in *RegRxBw*, receiving a PN15 sequence. Sensitivities are reported for a 0.1% BER (with Bit Synchronizer enabled), unless otherwise specified. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the receiver sensitivity level.

Table 8 Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	Direct tie of RFI and RFO pins, as shown in Figure 43. FSK sensitivity, highest LNA gain.	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s* FDA = 20 kHz, BR = 38.4 kb/s** FDA = 62.5 kHz, BR = 250 kb/s***	- - - - -	-119 -115 -105 -106 -92	- - - - -	dBm dBm dBm dBm dBm
	Split RF paths, as shown in Figure 44, LnaBoost is turned on, the RF switch insertion loss is not accounted for.	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s* FDA = 20 kHz, BR = 38.4 kb/s** FDA = 62.5 kHz, BR = 250 kb/s***	- - - - -	-123 -119 -110 -110 -97	- - - - -	dBm dBm dBm dBm dBm
RFS_O	OOK sensitivity, highest LNA gain Conditions of Figure 43	BR = 4.8 kb/s BR = 32 kb/s	- -	-117 -108	- -	dBm dBm
CCR	Co-Channel Rejection		-	-8	-	dB
ACR	Adjacent Channel Rejection	FDA = 2 kHz, BR = 1.2kb/s, RxBw = 5.2kHz Offset = +/- 25 kHz	-	54	-	dB
		FDA = 5 kHz, BR=4.8kb/s Offset = +/- 25 kHz Offset = +/- 50 kHz	- -	50 50	- -	dB dB
BI	Blocking Immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	73 78 87	- - -	dB dB dB
AMR	AM Rejection, AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	73 78 87	- - -	dB dB dB

IIP2	2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Highest LNA gain	-	+57	-	dBm
IIP3	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Highest LNA gain G1 LNA gain G2, 4 dB sensitivity hit	- -	-12 -8	- -	dBm dBm
BW_SSB	Single Side channel filter BW	Programmable	2.7	-	250	kHz
IMR	Image Rejection	Wanted signal 3dB over sens BER=0.1%	-	48	-	dB
IMA	Image Attenuation		-	56	-	dB
DR_RSSI	RSSI Dynamic Range	AGC enabled Min Max	- -	-127 0	- -	dBm dBm

* *RxBw = 83 kHz (Single Side Bandwidth)*

** *RxBw = 50 kHz (Single Side Bandwidth)*

*** *RxBw = 250 kHz (Single Side Bandwidth)*

2.5.4. Transmitter

Table 9 Transmitter Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RF_OP	RF output power in 50 ohms on RFO pin (High efficiency PA).	Programmable with steps Max Min	 +11 -	 +14 -1	 - -	 dBm dBm
ΔRF_OP_V	RF output power stability on RFO pin versus voltage supply.	VDD = 2.5 V to 3.3 V VDD = 1.8 V to 3.7 V	- -	3 8	- -	dB dB
RF_OPH	RF output power in 50 ohms, on PA_BOOST pin (Regulated PA).	Programmable with 1 dB steps Max Min	- -	+17 +2	- -	dBm dBm
RF_OPH_MAX	Max RF output power, on PA_BOOST pin	High power mode	-	+20	-	dBm
ΔRF_OPH_V	RF output power stability on PA_BOOST pin versus voltage supply.	VDD = 2.4 V to 3.7 V	-	±1	-	dB
ΔRF_T	RF output power stability versus temperature on both RF pins.	From T = -40 °C to +85 °C	-	+/-1	-	dB
PHN	Transmitter Phase Noise	Low Consumption PLL, 915 MHz 50 kHz Offset 400 kHz Offset 1 MHz Offset	 - - -	 -102 -114 -120	 - - -	 dBc/Hz
		Low Phase Noise PLL, 915 MHz 50 kHz Offset 400 kHz Offset 1 MHz Offset	 - - -	 -106 -117 -122	 - - -	 dBc/Hz

ACP	Transmitter adjacent channel power (measured at 25 kHz off-set)	BT=1. Measurement conditions as defined by EN 300 220-1 V2.4.1	-	-	-37	dBm
TS_TR	Transmitter wake up time, to the first rising edge of DCLK	Frequency Synthesizer enabled, *PaRamp* = 10us, BR = 4.8 kb/s	-	120	-	us

2.5.5. Digital Specification

Conditions: Temp = 25°C, VDD = 3.3V, FXOSC = 32 MHz, unless otherwise specified.

Table 10 Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Digital input level high		0.8	-	-	VDD
V_{IL}	Digital input level low		-	-	0.2	VDD
V_{OH}	Digital output level high	Imax = 1 mA	0.9	-	-	VDD
V_{OL}	Digital output level low	Imax = -1 mA	-	-	0.1	VDD
F_{SCK}	SCK frequency		-	-	10	MHz
t_{ch}	SCK high time		50	-	-	ns
t_{cl}	SCK low time		50	-	-	ns
t_{rise}	SCK rise time		-	5	-	ns
t_{fall}	SCK fall time		-	5	-	ns
t_{setup}	MOSI setup time	from MOSI change to SCK rising edge	30	-	-	ns
t_{hold}	MOSI hold time	from SCK rising edge to MOSI change	20	-	-	ns
t_{nsetup}	NSS setup time	from NSS falling edge to SCK rising edge	30	-	-	ns
t_{nhold}	NSS hold time	from SCK falling edge to NSS rising edge, normal mode	100	-	-	ns
t_{nhigh}	NSS high time between SPI accesses		20	-	-	ns
T_DATA	DATA hold and setup time		250	-	-	ns

3. Chip Description

This section describes in depth the architecture of the SX1235 low-power, highly integrated ETSI category 1 compatible transceiver. The following figure shows a simplified block diagram of the SX1235.

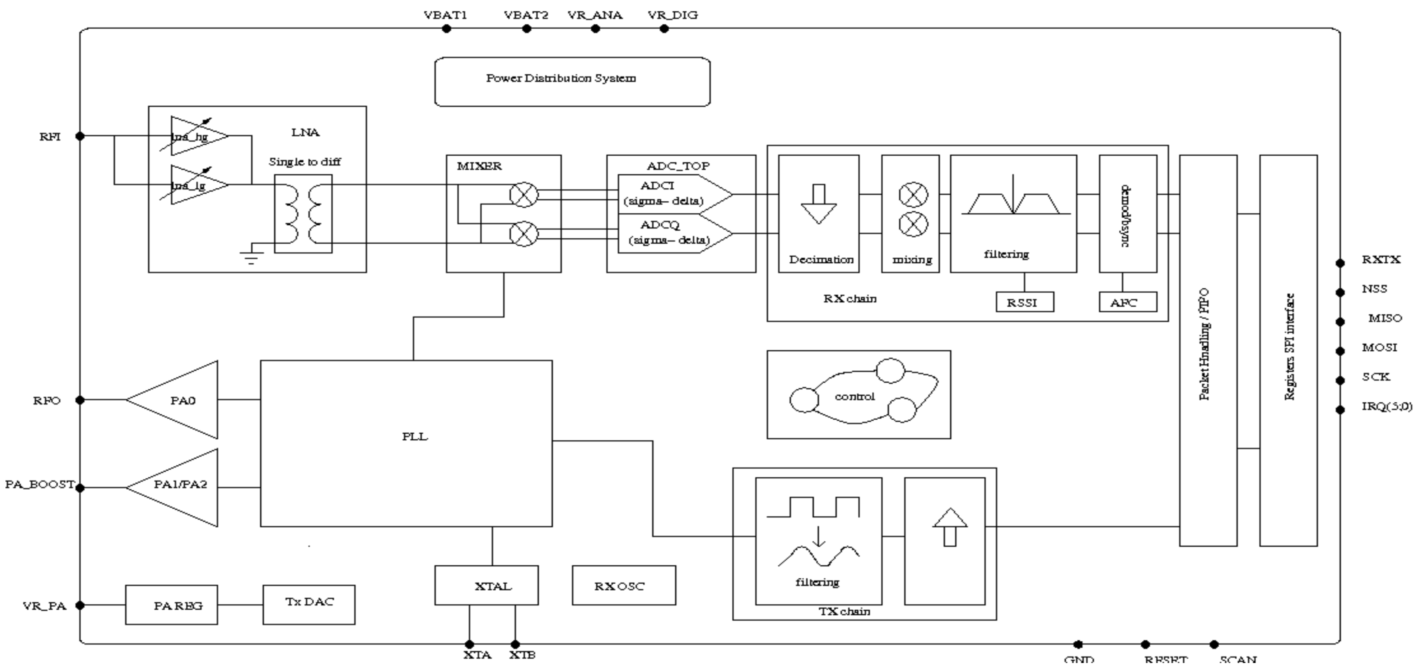


Figure 8. Simplified SX1235 Block Schematic Diagram

SX1235 is a half-duplex, low-IF transceiver. Here the received RF signal is first amplified by the LNA. The LNA input is single ended to minimise the external BoM and for ease of design. Following the LNA output the conversion to differential is made to improve the second order linearity and harmonic rejection. The signal is then down-converted to in-phase (I) and quadrature (Q) components at the intermediate frequency (IF) by the mixer stage. A pair of sigma delta ADCs then perform data conversion, with all subsequent signal processing and demodulation performed in the digital domain. The digital state machine also controls the automatic frequency correction (AFC), received signal strength indicator (RSSI) and automatic gain control (AGC). It also features the higher-level packet and protocol level functionality of the top level sequencer.

In the receiver operating mode two states of functionality are defined. Upon initial transition to receiver operating mode the receiver is in the 'receiver-enabled' state. In this state the receiver awaits for either the user defined valid preamble or RSSI detection criterion to be fulfilled. Once met the receiver enters 'receiver-active' state. In this second state the received signal is processed by the packet engine and top level sequencer.

The frequency synthesiser generates the local oscillator (LO) frequency for both receiver and transmitter. The PLL is optimized for user-transparent, low lock time, fast auto-calibrating operation. In transmission, frequency modulation is performed digitally within the PLL bandwidth. SX1235 Also features optional pre-filtering of the bit stream to improve spectral purity.

SX1235 features a pair of RF power amplifiers. The first, connected to RFO, can deliver up to +14 dBm, is unregulated for high power efficiency and can be connected directly to the RF receiver input via a pair of passive components to form a single antenna port high efficiency transceiver. The second PA, connected to the PA_BOOST pin and can deliver up to +20 dBm via a dedicated matching network.

SX1235 also includes two timing references: an RC oscillator and a 32 MHz crystal oscillator.

All major parameters of the RF front end and digital state machine are fully configurable via an SPI interface which gives access to internal registers. This includes a mode auto sequencer that oversees the transition and calibration of the SX1235 between intermediate modes of operation in the fastest time possible.

3.1. Power Supply Strategy

The SX1235 employs an advanced power supply scheme, which provides stable operating characteristics over the full temperature and voltage range of operation. This includes the full output power of +17dBm which is maintained from 1.8 to 3.7 V.

The SX1235 can be powered from any low-noise voltage source via pins VBAT1 and VBAT2. Decoupling capacitors should be connected, as suggested in the reference design, on VR_PA, VR_DIG and VR_ANA pins to ensure a correct operation of the built-in voltage regulators.

3.2. Low Battery Detector

A low battery detector is also included allowing the generation of an interrupt signal in response to passing a programmable threshold adjustable through the register *RegLowBat*. The interrupt signal can be mapped to any of the DIO pins, by programming *RegDioMapping*.

3.3. Frequency Synthesis

3.3.1. Reference Oscillator

The crystal oscillator is the main timing reference of the SX1235. It is used as a reference for the frequency synthesizer and as a clock for the digital processing.

The XO startup time, TS_OSC, depends on the actual XTAL being connected on pins XTA and XTB. The SX1232 optimizes the startup time and automatically triggers the PLL when the XO signal is stable.

An external clock can be used to replace the crystal oscillator, for instance a tight tolerance TCXO. To do so, *TcxoInputOn* in *RegTcxo* should be set to 1, and the external clock has to be provided on XTA (pin 4). XTB (pin 5) should be left open.

The peak-peak amplitude of the input signal must never exceed 1.8 V. Please consult your TCXO supplier for an appropriate value of decoupling capacitor, C_D.

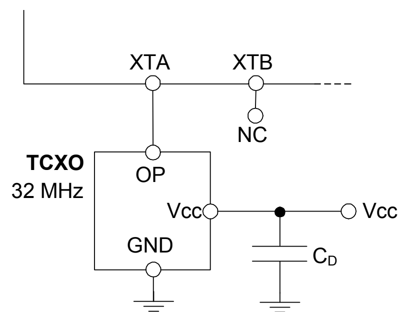


Figure 9. TCXO Connection

3.3.2. CLKOUT Output

The reference frequency, or a fraction of it, can be provided on DIO5 (pin 12) by modifying bits *ClkOut* in *RegDioMapping2*. Two typical applications of the CLKOUT output include:

- To provide a clock output for a companion processor, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode except Sleep mode and is automatically enabled at power on reset.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note to minimize the current consumption of the SX1235, please ensure that the CLKOUT signal is disabled when not required.

3.3.3. PLL Architecture

The local oscillator of the SX1235 is derived from a fractional-N PLL that is referenced to the crystal oscillator circuit. Two PLLs are available for transmit mode operation - either low phase noise or low current consumption to maximize either transmit power consumption or transmit spectral purity. Both PLLs feature a programmable bandwidth setting where one of four discrete preset bandwidths may be accessed. For reference the relative performance of both low consumption and low phase noise PLL, for each programmable bandwidth setting, is shown in the following figure.

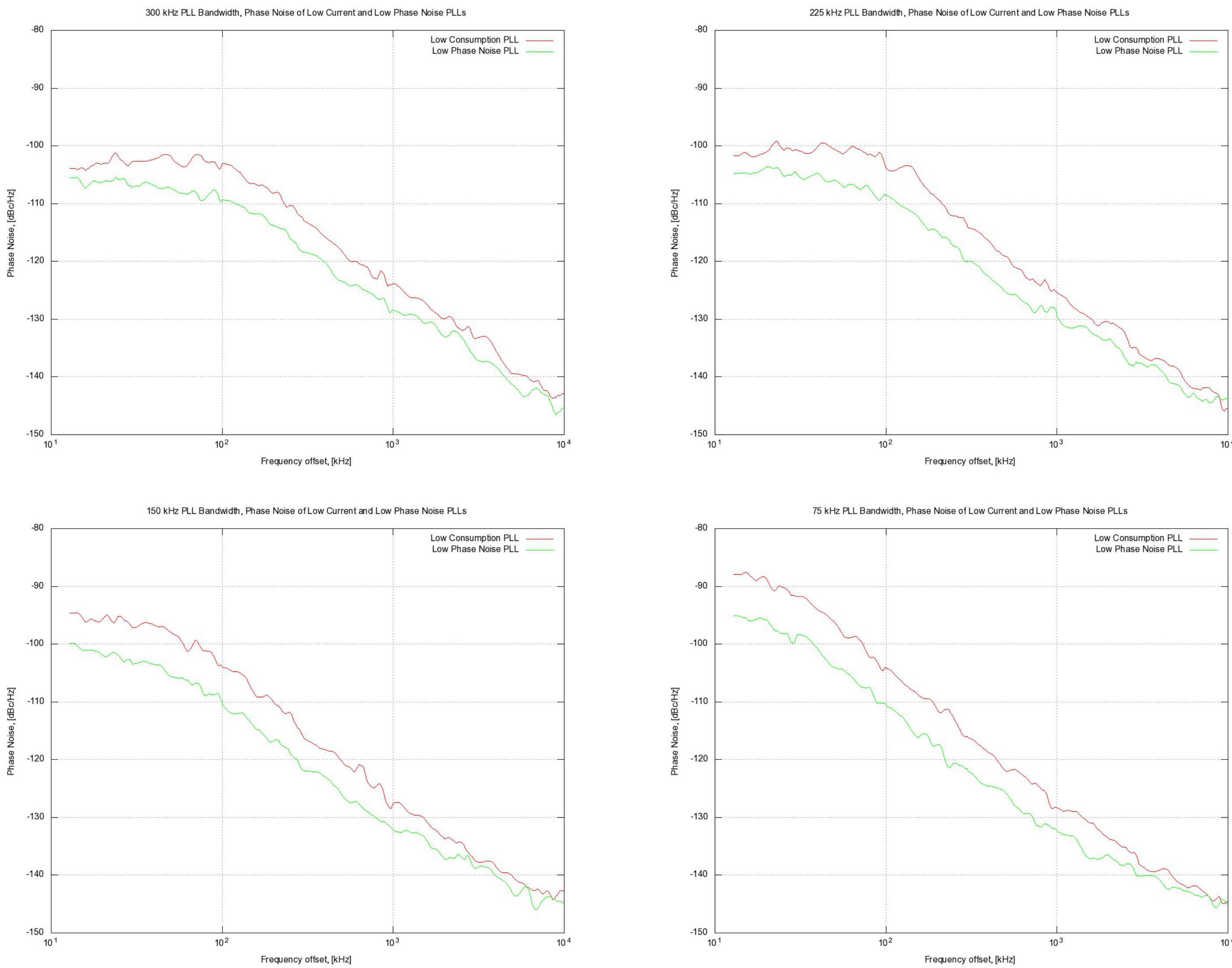


Figure 10. Typical Phase Noise Performances of the Low Consumption and Low Phase Noise PLLs.

Note in receive mode, only the low consumption PLL is available.

The SX1235 PLL embeds a 19-bit sigma-delta modulator and its frequency resolution, constant over the whole frequency range, and is given by:

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

The carrier frequency is programmed through *RegFrf*, split across addresses 0x06 to 0x08:

$$F_{RF} = F_{STEP} \times Frf(23,0)$$

Note The Frf setting is split across 3 bytes. A change in the center frequency will only be taken into account when the least significant byte FrfLsb in RegFrfLsb is written. This allows for more complex modulation schemes such as m-ary FSK, where frequency modulation is achieved by changing the programmed RF frequency.

3.3.4. RC Oscillator

All timings in the low-power state of the Top Level Sequencer rely on the accuracy of the internal low-power RC oscillator. This oscillator is automatically calibrated at the device power-up, and it is a user-transparent process.

For applications enduring large temperature variations, and for which the power supply is never removed, RC calibration can be performed upon user request. *RcCalStart* in *RegOsc* triggers this calibration, and the flag *RcCalDone* will be set automatically when the calibration is over.

3.4. Transmitter Description

The transmitter of SX1235 comprises the frequency synthesizer, modulator and power amplifier blocks, together with the DC biasing and ramping functionality that is provided through the VR_PA block.

3.4.1. Architecture Description

The architecture of the RF front end is shown in the following diagram. Here we see that the unregulated PA0 is connected to the RFO pin features a single low power amplifier device. The PA_BOOST pin is connected to the internally regulated PA1 and PA2 circuits. Here PA2 is a high power amplifier that permits continuous operation up to +17 dBm and duty cycled operation up to +20 dBm. For full details of operation at +20 dBm please consult Section 3.4.7.

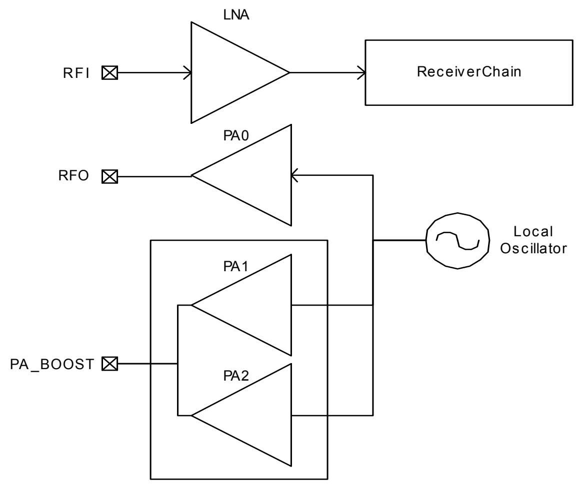


Figure 11. RF Front-end Architecture Shows the Internal PA Configuration.

3.4.2. Bit Rate Setting

The bit rate setting is referenced to the crystal oscillator and provides a precise means of setting the bit (or equivalently chip) rate of the radio. In continuous transmit mode (Section 5.1.2) the data stream to be transmitted can be input directly to the modulator via pin 9 (DIO2/DATA) in an asynchronous manner, unless Gaussian filtering is used, in which case the DCLK signal on pin 10 (DIO1/DCLK) is used to synchronize the data stream. See section 3.4.5 for details on the Gaussian filter.

In Packet mode or in Continuous mode with Gaussian filtering enabled, the Bit Rate (BR) is controlled by bits *Bitrate* in *RegBitrateMsb and RegBitrateLsb*

$$BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{BitrateFrac}{16}}$$

*Note BitrateFrac bits have **no effect** (i.e may be considered equal to 0) **in OOK** modulation mode*

The quantity *BitrateFrac* is hence designed to allow very high precision (max. 250 ppm calculation error) for any bitrate in the programmable range. Table 11 below shows a range of standard bit rates and the accuracy to within which they may be reached.

Table 11 Bit Rate Examples

Type	BitRate (15:8)	BitRate (7:0)	(G)FSK (G)MSK	OOK	Actual BR (b/s)
Classical modem baud rates (multiples of 1.2 kbps)	0x68	0x2B	1.2 kbps	1.2 kbps	1200.015
	0x34	0x15	2.4 kbps	2.4 kbps	2400.060
	0x1A	0x0B	4.8 kbps	4.8 kbps	4799.760
	0x0D	0x05	9.6 kbps	9.6 kbps	9600.960
	0x06	0x83	19.2 kbps	19.2 kbps	19196.16
	0x03	0x41	38.4 kbps		38415.36
	0x01	0xA1	76.8 kbps		76738.60
	0x00	0xD0	153.6 kbps		153846.1
Classical modem baud rates (multiples of 0.9 kbps)	0x02	0x2C	57.6 kbps		57553.95
	0x01	0x16	115.2 kbps		115107.9
Round bit rates (multiples of 12.5, 25 and 50 kbps)	0x0A	0x00	12.5 kbps	12.5 kbps	12500.00
	0x05	0x00	25 kbps	25 kbps	25000.00
	0x80	0x00	50 kbps		50000.00
	0x01	0x40	100 kbps		100000.0
	0x00	0xD5	150 kbps		150234.7
	0x00	0xA0	200 kbps		200000.0
	0x00	0x80	250 kbps		250000.0
	0x00	0x6B	300 kbps		299065.4
Watch Xtal frequency	0x03	0xD1	32.768 kbps	32.768 kbps	32753.32

3.4.3. FSK Modulation

FSK modulation is performed inside the PLL bandwidth, by changing the fractional divider ratio in the feedback loop of the PLL. The large resolution of the sigma-delta modulator, allows for very narrow frequency deviation. The frequency deviation F_{DEV} is given by:

$$F_{DEV} = F_{STEP} \times Fdev(13,0)$$

To ensure a proper modulation, the following limit applies:

$$F_{DEV} + \frac{BR}{2} \leq (250)kHz$$

Note no constraint applies to the modulation index of the transmitter, but the frequency deviation must be set between 600 Hz and 200 kHz.

3.4.4. OOK Modulation

OOK modulation is applied by switching on and off the Power Amplifier. Digital control and smoothing are available to improve the transient power response of the OOK transmitter.

3.4.5. Modulation Shaping

Modulation shaping can be applied in both OOK and FSK modulation modes, to improve the narrowband response of the transmitter. Both shaping features are controlled with *PaRamp* bits in *RegPaRamp*.

- In FSK mode, a Gaussian filter with BT = 0.5 or 1 is used to filter the modulation stream, at the input of the sigma-delta modulator. If the Gaussian filter is enabled when the SX1232 is in Continuous mode, DCLK signal on pin 10 (DIO1/DCLK) will trigger an interrupt on the uC each time a new bit has to be transmitted. Please refer to section 5.4.2 for details.
- When OOK modulation is used, the PA bias voltages are ramped up and down smoothly when the PA is turned on and off, to reduce spectral splatter.

Note *the transmitter must be restarted if the ModulationShaping setting is changed, in order to recalibrate the built-in filter.*

3.4.6. RF Power Amplifiers

Three power amplifier blocks are embedded in the SX1235. The first one herein referred to as PA0, can generate high efficiency RF power into a 50 ohm load. The RF power is programmable between -1dBm and +14dBm. PA0 is connected to pin RFO (pin 22).

PA1 and PA2 are both connected to pin PA_BOOST (pin 23). They can deliver up to +17 dBm in programmable step of 1dB to the antenna, a specific impedance matching / harmonic filtering design is required to ensure impedance transformation and regulatory compliance. The RF power is programmable between +2 dBm and +17 dBm. The high power mode allows to achieve fixed output power of +20 dBm.

Table 12 Power Amplifier Mode Selection Truth Table

PaSelect	Mode	Power Range	Pout Formula
0	PA0 output on pin RFO	-1 to +14 dBm	-1 dBm + *OutputPower*
1	PA1 and PA2 combined on pin PA_BOOST	+2 to +17 dBm	+2 dBm + *OutputPower*
1	PA1+PA2 on PA_BOOST with high output power +20dBm settings (see 3.4.7)	+5 to +20 dBm	+5 dBm + *OutputPower*

Notes *- For +20 dBm restrictions of operation, please consult the following section*

- To ensure correct operation at the highest power levels, please make sure to adjust the OcpTrim accordingly in RegOcp.

- If PA_BOOST pin is not used the pin can be left floating.

3.4.7. High Power +20 dBm Operation

The SX1235 has a high power +20 dBm capability on PA_BOOST pin, with the following settings:

Table 13 High Power Settings

Register	*Address*	*Value for High Power*	*Default value PA0 or +17dBm*	Description
RegPaDac	0x5A	0x87	0x84	High power PA control

Note - High Power settings must be turned off when using PA0

- The Over Current Protection limit should be adapted to the actual power level, in RegOcp

Specific Absolute Maximum Ratings and Operating Range restrictions apply to the +20dBm operation. They are listed in Table 14 and Table 15.

Table 14 Absolute Maximum Rating, +20 dBm Operation

Symbol	Description	Min	Max	Unit
DC_20dBm	Duty Cycle of transmission at +20 dBm output	-	1	%
VSWR_20dBm	Maximum VSWR at antenna port, +20 dBm output	-	3:1	-

Table 15 Operating Range, +20dBm Operation

Symbol	Description	Min	Max	Unit
VDDop_20dBm	Supply voltage, +20 dBm output	2.4	3.7	V

The Duty Cycle of transmission at +20 dBm is limited to 1%, with a maximum VSWR of 3:1 at antenna port, over the standard operating range [-40;+85° C]. For any other operating condition, contact your Semtech representative.

3.4.8. Over Current Protection

An over current protection block is built-in the chip. It helps preventing surge currents required when the transmitter is used at its highest power levels, thus protecting the battery that may power the application. The current clamping value is controlled by *OcpTrim* bits in *RegOcp*, and is calculated with the following formulas:

Table 16 Trimming of the OCP Current

OcpTrim	I_{MAX}	Imax Formula
0 to 15	45 to 120 mA	45 + 5**OcpTrim* [mA]
16 to 27	130 to 240 mA	-30 + 10**OcpTrim* [mA]
27+	240 mA	*240 mA*

Note Imax sets a limit on the current drain of the Power Amplifier only, hence the maximum current drain of the SX1235 is equal to Imax + I_{FS}

3.5. Receiver Description

3.5.1. Overview

The SX1235 features a digital receiver with the analog to digital conversion process being performed directly following the LNA-Mixers block. The Low-IF receiver is able to handle ASK, OOK, (G)FSK and (G)MSK modulation. All the filtering, demodulation, gain control, synchronization and packet handling is performed digitally, which allows a very wide range of bit rates and frequency deviations to be selected. The receiver is also capable of automatic gain calibration to improve precision on RSSI measurement and enhanced image rejection.

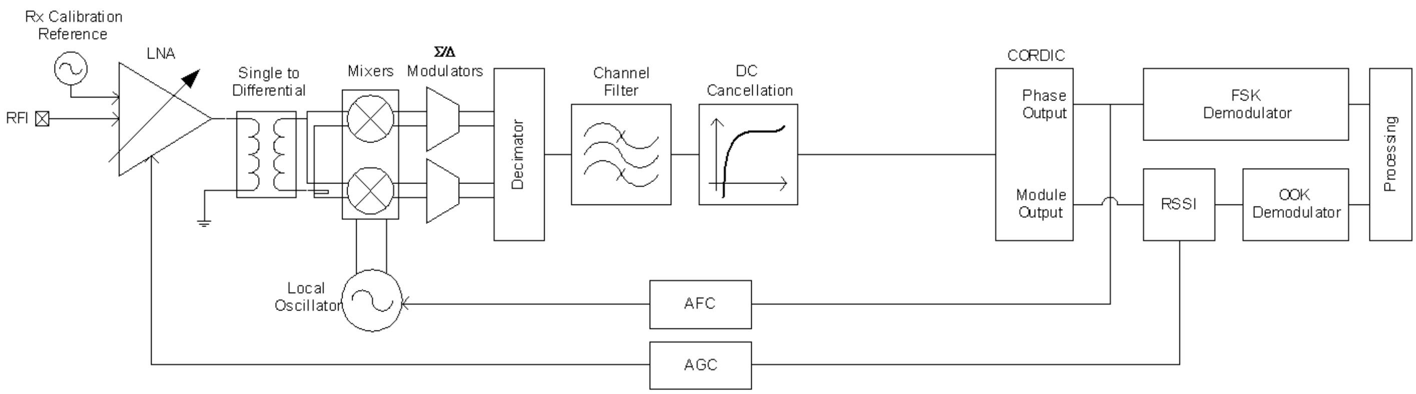


Figure 12. Receiver Block Diagram

3.5.2. Automatic Gain Control - AGC

The AGC feature allows receiver to handle a wide Rx input dynamic range from the sensitivity level up to maximum input level of 0dBm or more, whilst optimizing the system linearity.

Table 17 hereafter shows typical NF and IIP3 performances for the different LNA gains.

Table 17 LNA Gain Control and Performances

RX input level (Pin)	*Gain Setting*	*LnaGain*	*Relative LNA Gain [dB]*	NF [dB]	IIP3 [dBm]
Pin <= AgcThresh1	G1	‘001’	0 dB	7	-12
AgcThresh1 < Pin <= AgcThresh2	G2	‘010’	-6 dB	11	-8
AgcThresh2 < Pin <= AgcThresh3	G3	‘011’	-12 dB	16	-5
AgcThresh3 < Pin <= AgcThresh4	G4	‘100’	-24 dB	26	5
AgcThresh4 < Pin <= AgcThresh5	G5	‘110’	-26 dB	34	10
AgcThresh5 < Pin	G6	‘111’	-48 dB	44	10

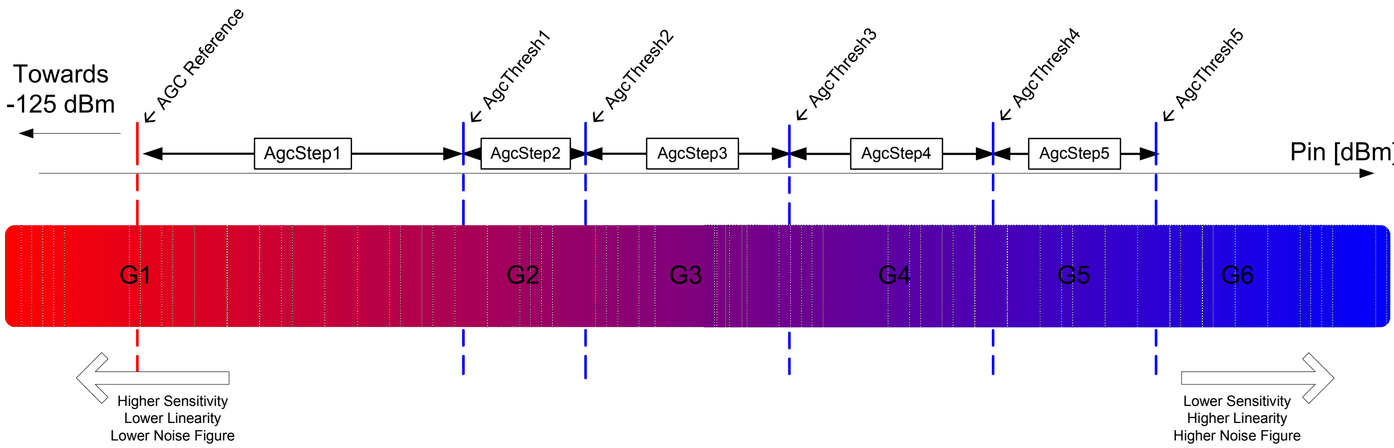


Figure 13. AGC Steps Definition

The global AGC reference, reference all AGC thresholds, is determined as follows:

AGC Reference[dBm]=-174dBm+10*log(2**RxBw*)+SNR+*AgcReferenceLevel*

with SNR = 8dB, fixed value

A detailed description of the receiver setup to enable the AGC is provided in section 4.3.

3.5.3. RSSI

The RSSI value reflects the incoming signal power provided at antenna port within the receiver bandwidth. The signal power is available in *RssiValue*. This value is absolute and its unit is in dBm with a resolution of 0.5dB. The formula hereafter gives the relationship between the register value and the absolute input signal level in dBm at antenna port:

$$RssiValue = -2 \cdot RF\ level\left[dBm\right] + RssiOffset\ \left[dB\right]$$

The RSSI value can be compensated for to take into account the loss in the matching network or the gain of an additional LNA, by using *RssiOffset*. The offset can be chosen in 1dB steps from -16 to +15dB. When compensation is applied, the effective signal strength is read as follows:

$$RSSI\left[dBm\right] = -\frac{RssiValue}{2}$$

The RSSI value is smoothed on a given number of measured RSSI samples. The precision of the RSSI value is related to the number of RSSI samples used. *RssiSmoothing* selects the number of RSSI samples from a minimum of 2 samples up to 256 samples in increments of power of 2. Table 18 hereafter gives the estimation of the RSSI accuracy for a 10dB SNR and the response time versus the number of RSSI samples selected in *RssiSmoothing*.

Table 18 RssiSmoothing Options

RssiSmoothing	Number of Samples	Estimated Accuracy	Response Time
'000'	2	± 6 dB	$\frac{2^{(RssiSmoothing+1)}}{4 \cdot RxBw[kHz]}[ms]$
'001'	4	± 5 dB	
'010'	8	± 4 dB	
'011'	16	± 3 dB	
'100'	32	± 2 dB	
'101'	64	± 1.5 dB	
'110'	128	± 1.2 dB	
'111'	256	± 1.1 dB	

The RSSI is calibrated, up the RFI pin, when Image and RSSI calibration is launched; please see section 3.5.12 for details.

3.5.4. Channel Filter

The role of the channel filter is to filter out the noise and interferers outside of the channel. Channel filtering on the SX1232 is implemented with a 16-tap Finite Impulse Response (FIR) filter, providing an outstanding Adjacent Channel Rejection performance, even for narrowband applications.

Note to respect oversampling rules in the decimation chain of the receiver, the Bit Rate cannot be set at a higher value than 2 times the single-side receiver bandwidth (BitRate < 2 x RxBw)

The single-side channel filter bandwidth *RxBw* is controlled by the parameters *RxBwMant* and *RxBwExp* in *RegRxBw:*

$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp + 2}}$$

The Rx bandwidth mantissa ($RxBwMant$) also sets the intermediate Freudians of the receiver. Note that as a consequence, a different IF may be used in AFC and ensuing communication phases. The table below summarizes the available channel filter bandwidths and the corresponding receiver intermediate frequency. (Crystal oscillator at 32 MHz):

Table 19 Available RxBw Settings

RxBwMant (binary/value)	*RxBwExp* (decimal)	*RxBw (kHz)* FSK / OOK	*Intermediate Frequency (kHz)*
10b / 24	7	2.6	166.66
01b / 20	7	3.1	200
00b / 16	7	3.9	250
10b / 24	6	5.2	166.66
01b / 20	6	6.3	200
00b / 16	6	7.8	250
10b / 24	5	10.4	166.66
01b / 20	5	12.5	200
00b / 16	5	15.6	250
10b / 24	4	20.8	166.66
01b / 20	4	25.0	200
00b / 16	4	31.3	250
10b / 24	3	41.7	166.66

01b / 20	3	50.0	200
00b / 16	3	62.5	250
10b / 24	2	83.3	166.66
01b / 20	2	100.0	200
00b / 16	2	125.0	250
10b / 24	1	166.7	166.66
01b / 20	1	200.0	200
00b / 16	1	250.0	250
Other settings		reserved	N/A

3.5.5. FSK Demodulator

The FSK demodulator of the SX1235 is designed to demodulate FSK, GFSK, MSK and GMSK modulated signals. It is most efficient when the modulation index of the signal is greater than 0.5 and below 10:

$$0.5 \le \beta = \frac{2 \times F_{DEV}}{BR} \le 10$$

The output of the FSK demodulator can be fed to the Bit Synchronizer to provide the companion processor with a synchronous data stream in Continuous mode.

3.5.6. OOK Demodulator

The OOK demodulator performs a comparison of the RSSI output and a threshold value. Three different threshold modes are available, configured through bits *OokThreshType* in *RegOokPeak*.

The recommended mode of operation is the "Peak" threshold mode, illustrated in Figure 14:

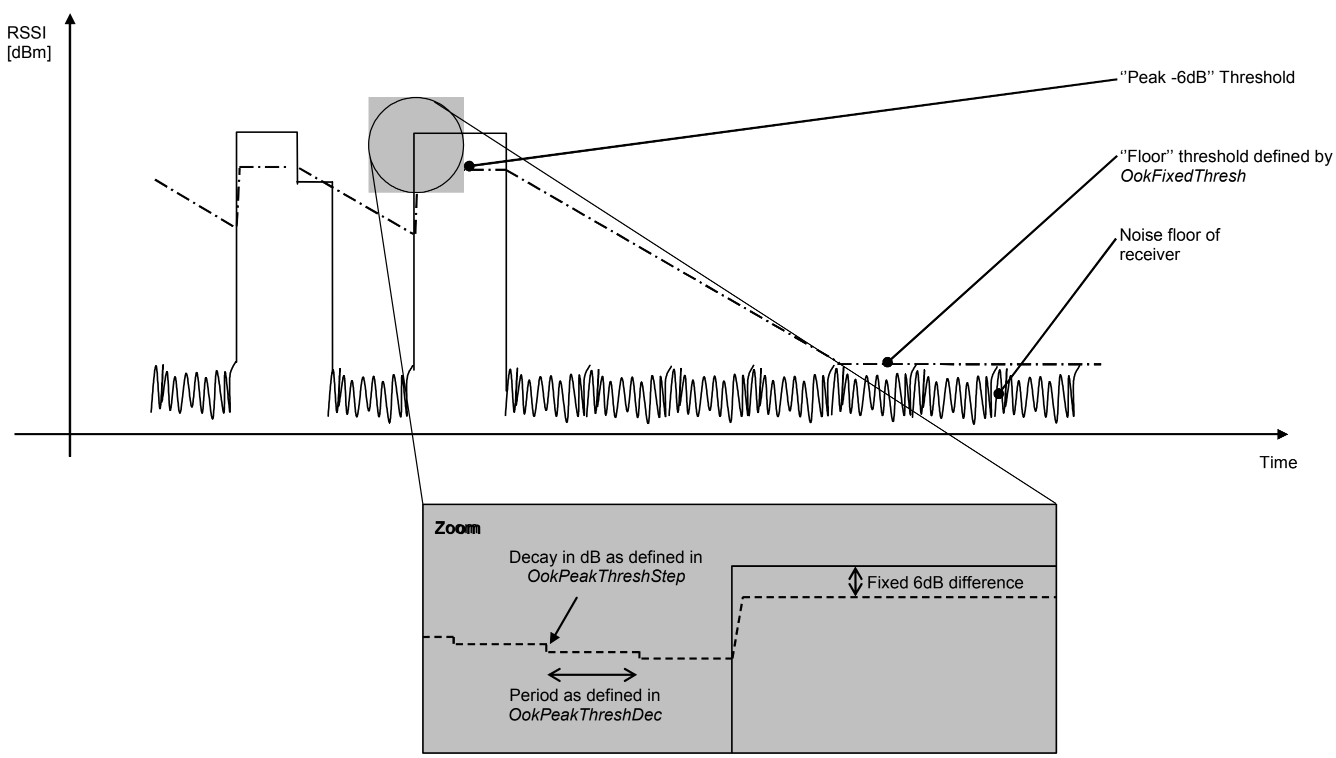


Figure 14. OOK Peak Demodulator Description

In peak threshold mode the comparison threshold level is the peak value of the RSSI, reduced by 6dB. In the absence of an input signal, or during the reception of a logical "0", the acquired peak value is decremented by one *OokPeakThreshStep* every *OokPeakThreshDec* period.

When the RSSI output is null for a long time (for instance after a long string of "0" received, or if no transmitter is present), the peak threshold level will continue falling until it reaches the "Floor Threshold", programmed in *OokFixedThresh*.

The default settings of the OOK demodulator lead to the performance stated in the electrical specification. However, in applications in which sudden signal drops are awaited during a reception, the three parameters should be optimized accordingly.

3.5.6.1. Optimizing the Floor Threshold

OokFixedThresh determines the sensitivity of the OOK receiver, as it sets the comparison threshold for weak input signals (i.e. those close to the noise floor). Significant sensitivity improvements can be generated if configured correctly.

Note that the noise floor of the receiver at the demodulator input depends on:

- The noise figure of the receiver.
- The gain of the receive chain from antenna to base band.
- The matching - including SAW filter if any.
- The bandwidth of the channel filters.

It is therefore important to note that the setting of *OokFixedThresh* will be application dependant. The following procedure is recommended to optimize *OokFixedThresh*.

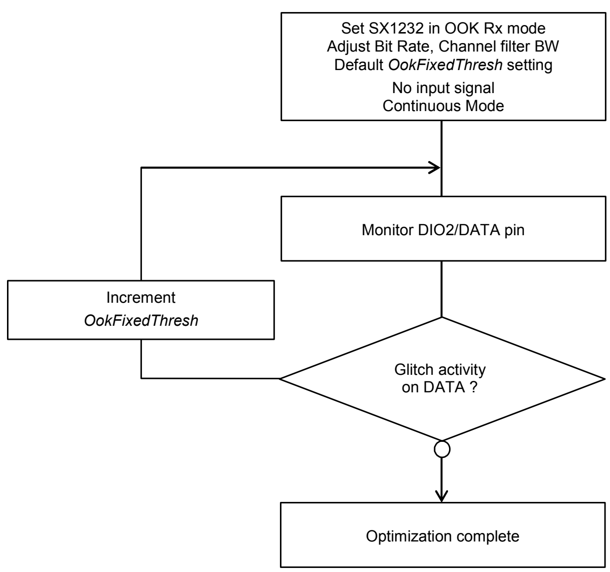


Figure 15. Floor Threshold Optimization

The new floor threshold value found during this test should be used for OOK reception with those receiver settings.

3.5.6.2. Optimizing OOK Demodulator for Fast Fading Signals

A sudden drop in signal strength can cause the bit error rate to increase. For applications where the expected signal drop can be estimated, the following OOK demodulator parameters *OokPeakThreshStep* and *OokPeakThreshDec* can be optimized as described below for a given number of threshold decrements per bit. Refer to *RegOokPeak* to access those settings.

3.5.6.3. Alternative OOK Demodulator Threshold Modes

In addition to the Peak OOK threshold mode, the user can alternatively select two other types of threshold detectors:

- Fixed Threshold: The value is selected through *OokFixedThresh*
- Average Threshold: Data supplied by the RSSI block is averaged, and this operation mode should only be used with DC-free encoded data.

3.5.7. Bit Synchronizer

The Bit Synchronizer is a block that provides a clean and synchronized digital output, free of glitches. Its output is made available on pin DIO1/DCLK in Continuous mode and can be disabled through register settings. However, for optimum receiver performance its use when running Continuous mode is strongly advised.

The Bit Synchronizer is automatically activated in Packet mode. Its bit rate is controlled by *BitRateMsb* and *BitRateLsb* in *RegBitrate.*

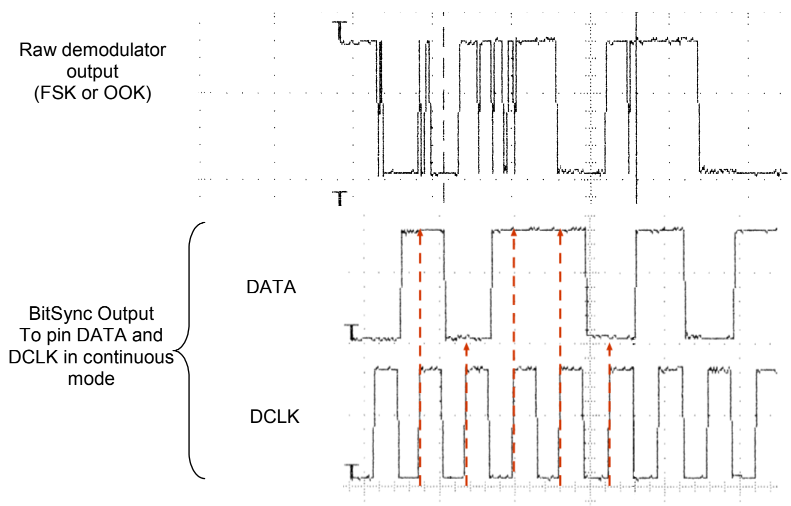


Figure 16. Bit Synchronizer Description

To ensure correct operation of the Bit Synchronizer, the following conditions have to be satisfied:

- A preamble (0x55 or 0xAA) of at least 12 bits is required for synchronization, the longer the synchronization the better the packet success rate
- The subsequent payload bit stream must have at least one transition form '0' to '1' or '1' to '0 every 16 bits during data transmission
- The bit rate matching between the transmitter and the receiver must be better than 6.5%.

3.5.8. Frequency Error Indicator

This function provides information about the frequency error of the local oscillator (LO) compared with the carrier frequency of a modulated signal at the input of the receiver. When the FEI block is launched, the frequency error is measured and the signed result is loaded in *FeiValue* in *RegFei*, in 2's complement format. The time required for an FEI evaluation is 4 times the bit period.

To ensure a proper behavior of the FEI:

- The operation must be done during the reception of preamble
- The sum of the frequency offset and the 20 dB signal bandwidth must be lower than the base band filter bandwidth

The 20 dB bandwidth of the signal can be evaluated as follows (double-side bandwidth):

$$BW_{20dB} = 2 \times \left(F_{DEV} + \frac{BR}{2}\right)$$

The frequency error, in Hz, can be calculated with the following formula:

$$FEI = F_{STEP} \times FeiValue$$

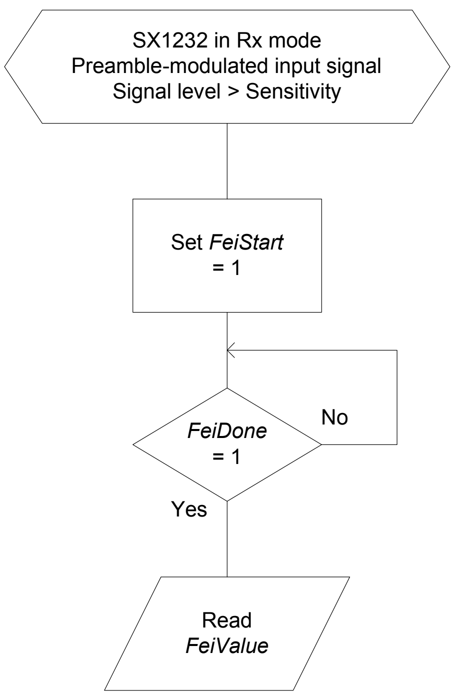


Figure 17. FEI Process

3.5.9. AFC

The AFC is based on the FEI block, and therefore the same input signal and receiver setting conditions apply. When the AFC procedure is done, *AfcValue* is directly subtracted to the register that defines the frequency of operation of the chip, F_{RF}. The AFC is executed each time the receiver is enabled, if *AfcAutoOn* = 1.

When the AFC is enabled (*AfcAutoOn* = 1), the user has the option to:

- Clear the former AFC correction value, if *AfcAutoClearOn* = 1
- Start the AFC evaluation from the previously corrected frequency. This may be useful in systems in which the LO keeps on drifting in the “same direction”. Ageing compensation is a good example.

The SX1232 offers an alternate receiver bandwidth setting during the AFC phase, to accommodate large LO drifts. If the user considers that the received signal may be out of the receiver bandwidth, a higher channel filter bandwidth can be programmed in *RegAfcBw*, at the expense of the receiver noise floor, which will impact upon sensitivity.

The FEI is valid only during preamble, and therefore the *PreambleDetect* flag can be used to validate the current FEI result and add it to the AFC register. The link between *PreambleDetect* interrupt and the AFC is controlled by *StartDemodOnPreamble* in *RegRxConfig*.

A detailed description of the receiver setup to enable the AFC is provided in section 4.3.

3.5.10. Preamble Detector

The Preamble Detector indicates the reception of a carrier modulated with a 0101...sequence. It is insensitive to the frequency offset, as long as the receiver bandwidth is large enough. The size of detection can be programmed from 1 to 3 bytes with *PreambleDetectorSize* in *RegPreambleDetect* as defined in the next table.

Table 20 Preamble Detector Settings

PreambleDetectorSize	**# of Bytes**
00	1
01	2 (recommended)
10	3
11	reserved

For proper operation, *PreambleDetectTol* should be set to be set to 10 (0x0A), with a qualifying preamble size of 2 bytes.

PreambleDetect interrupt (either in *RegIrqFlags1* or mapped to a specific DIO) goes high every time a valid preamble is detected, assuming *PreambleDetectorOn*=1.

The preamble detector can also be used as a gate to ensure that AFC and AGC are performed on valid preamble. See section 4.3 for details.

3.5.11. Image Rejection Mixer

The SX1235 embeds a state of the art Image Rejection Mixer (IRM). Its default rejection, with no calibration, is 35dB typ.

The IQ signals can be calibrated by an embedded source, pushing the image rejection to typically 48dB. This process is fully automated and self-contained.

3.5.12. Image and RSSI Calibration

Calibration of the I and Q signal is required to improve the RSSI precision, as well as good Image Rejection performance. On the SX1232, IQ calibration is seamless and user-transparent. Calibration is launched:

- Automatically at Power On Reset or after a Manual Reset of the chip (refer to section 7.2). For applications where the temperature remains stable, or if the Image Rejection is not a major concern, this one-shot calibration will suffice
- Automatically when a pre-defined temperature change is observed
- Upon User request, by setting bit *ImageCalStart* in *RegImageCal*, when the device is in Standby mode.

A selectable temperature change, set with *TempThreshold* (5, 10, 15 or 20°C), is detected and reported in *TempChange*, if the temperature monitoring is turned On with *TempMonitorOff*=0.

This interrupt flag can be used by the application to launch a new Image Calibration at a convenient time if *AutoImageCalOn*=0, or immediately when this temperature variation is detected, if *AutoImageCalOn*=1.

The calibration process takes approximately 10ms.

3.6. Temperature Measurement

A stand alone temperature measurement block is used in order to measure the temperature in any mode except Sleep and Standby. It is enabled by default, and can be stopped by setting *TempMonitorOff* to 1. The result of the measurement is stored in *TempValue* in *RegTemp*.

Due to process variations, the absolute accuracy of the result is +/- 10 °C. A more precise result needs initial calibration to be done externally.

Example temperature curve, typical device

		Correction Factor	15
Actual Temp [Celsius]	RegTemp [Dec]	Temp before calibration [°C]	Temp after calibration [°C]
85	181	74	89
75	190	65	80
65	201	54	69
55	211	44	59
45	222	33	48
35	232	23	38
25	245	10	25
15	0	0	15
5	10	-10	5
-5	21	-21	-6
-15	33	-33	-18
-25	44	-44	-29
-35	56	-56	-41
-40	63	-63	-48

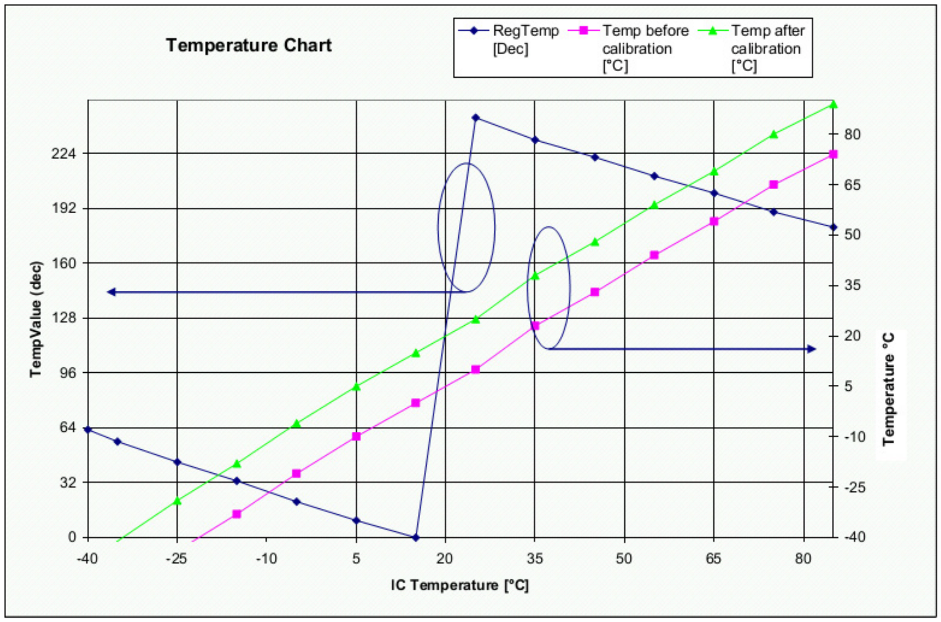


Figure 18. Temperature Sensor Response

An example code for the conversion to be applied to *TempValue* to obtain the reading in °C is shown in Section 7.

3.7. Timeout Function

The SX1235 includes a Timeout function, which allows it to automatically shut-down the receiver after a receive sequence and therefore save energy.

- *Timeout* interrupt is generated *TimeoutRxRssi x 16 x Tbit* after switching to Rx mode if the *Rssi* flag does not raise within this time frame (*RssiValue* > *RssiThreshold*)
- *Timeout* interrupt is generated *TimeoutRxPreamble x 16 x Tbit* after switching to Rx mode if the *PreambleDetect* flag does not raise within this time frame
- *Timeout* interrupt is generated *TimeoutSignalSync x 16 x Tbit* after switching to Rx mode if the *SyncAddress* flag does not raise within this time frame

This timeout interrupt can be used to warn the companion processor to shut down the receiver and return to a lower power mode. To become active, these timeouts must also be enabled by setting the correct *RxTrigger* parameters in *RegRxConfig:*

Table 21 RxTrigger Settings to Enable Timeout Interrupts

Receiver Triggering Event	RxTrigger (2:0)	Timeout on Rssi	Timeout on Preamble	Timeout on SyncAddress
None	000	Off	Off	Active
Rssi Interrupt	001	Active	Off	
PreambleDetect	110	Off	Active	
Rssi Interrupt & *PreambleDetect*	111	Active	Active	

4. Operating Modes

4.1. General Overview

The SX1235 has several working modes, manually programmed in *RegOpMode*. Fully automated mode selection, packet transmission and reception is also possible using the Top Level Sequencer described in Section 4.5.

Table 22 Basic Transceiver Modes

Mode	Selected mode	Symbol	Enabled blocks
000	Sleep mode	Sleep	None
001	Standby mode	Stdby	Top regulator and crystal oscillator
010	Frequency synthesiser to Tx frequency	FSTx	Frequency synthesizer at Tx frequency (Frf)
011	Transmit mode	Tx	Frequency synthesizer and transmitter
100	Frequency synthesiser to Rx frequency	FSRx	Frequency synthesizer at frequency for reception (Frf-IF)
101	Receive mode	Rx	Frequency synthesizer and receiver

When switching from a mode to another, the sub-blocks are woken up according to a pre-defined and optimized sequence.

4.2. Startup Times

The startup time of the transmitter or the receiver is dependant upon which mode the transceiver was in at the beginning. For a complete description, Figure 19 below shows a complete startup process, from the lower power mode “Sleep”.

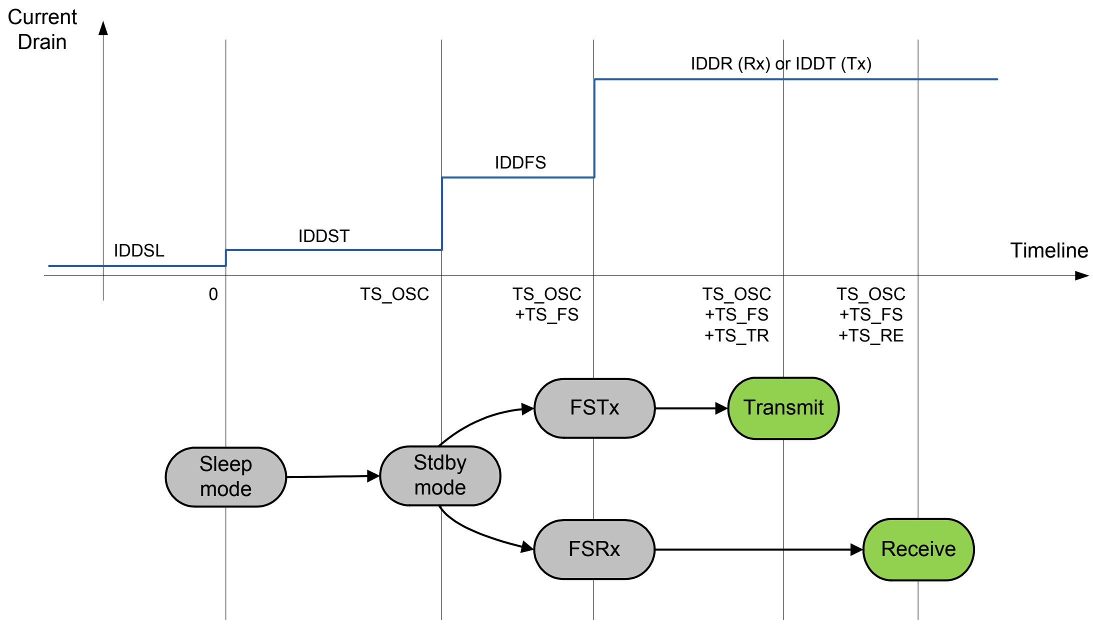


Figure 19. Startup Process

TS_OSC is the startup time of the crystal oscillator, and mainly depends on the characteristics of the crystal itself. TS_FS is the startup time of the PLL, and it includes a systematic calibration of the VCO.

Typical values of TS_OSC and TS_FS are given in section 2.3.

4.2.1. Transmitter Startup Time

The transmitter startup time, TS_TR, is calculated as follows, in when FSK modulation is selected:

$$TS\_TR = 5\mu s + 1.25 \times PaRamp + \frac{1}{2} \times Tbit$$,

where *PaRamp* is the ramp-up time programmed in *RegPaRamp* and *Tbit* is the bit time.

In OOK mode, this equation can be simplified to the following:

$$TS\_TR = 5\mu s + \frac{1}{2} \times Tbit$$

4.2.2. Receiver Startup Time

The receiver startup time, TS_RE, only depends upon the receiver bandwidth effective at the time of startup. When AFC is enabled (*AfcAutoOn*=1), *AfcBw* should be used instead of *RxBw* to extract the receiver startup time:

Table 23 Receiver Startup Time Summary

RxBw **if** ***AfcAutoOn=0*** ***RxBwAfc*** **if** ***AfcAutoOn=1***	**TS_RE** **(+/-5%)**
2.6 kHz	2.33ms
3.1 kHz	1.94ms
3.9 kHz	1.56ms
5.2 kHz	1.18ms
6.3 kHz	984us
7.8 kHz	791us
10.4 kHz	601us
12.5 kHz	504us
15.6 kHz	407us
20.8 kHz	313us
25.0 kHz	264us
31.3 kHz	215us
41.7 kHz	169us
50.0 kHz	144us
62.5 kHz	119us
83.3 kHz	97us
100.0 kHz	84us
125.0 kHz	71us
166.7 kHz	85us
200.0 kHz	74us
250.0 kHz	63us

TS_RE or later after setting the device in Receive mode, any incoming packet will be detected and demodulated by the transceiver.

4.2.3. Time to RSSI Evaluation

The first RSSI sample will be available TS_RSSI after the receiver is ready, in other words TS_RE + TS_RSSI after the receiver was requested to turn on.

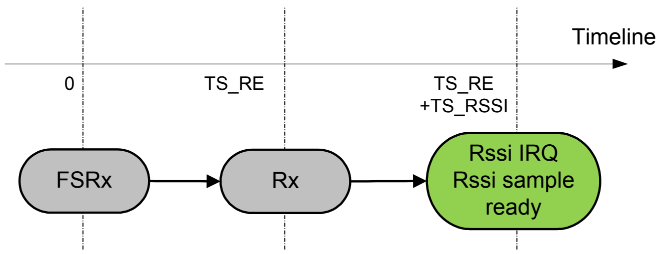


Figure 20. Time to Rssi Sample

TS_RSSI depends on the receiver bandwidth, as well as the *RssiSmoothing* option that was selected. The formula used to calculate TS_RSSI is provided in section 3.5.3.

4.2.4. Tx to Rx Turnaround Time

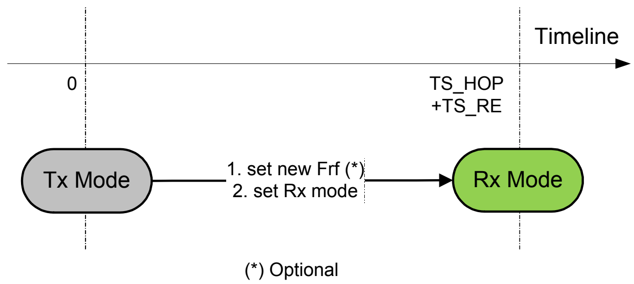


Figure 21. Tx to Rx Turnaround

Note the SPI instruction times are omitted, as they can generally be very small as compared to other timings (up to 10MHz SPI clock)

4.2.5. Rx to Tx

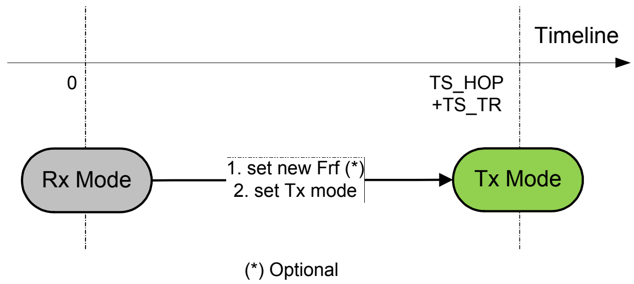


Figure 22. Rx to Tx Turnaround

4.2.6. Receiver Hopping, Rx to Rx

Two methods are possible:

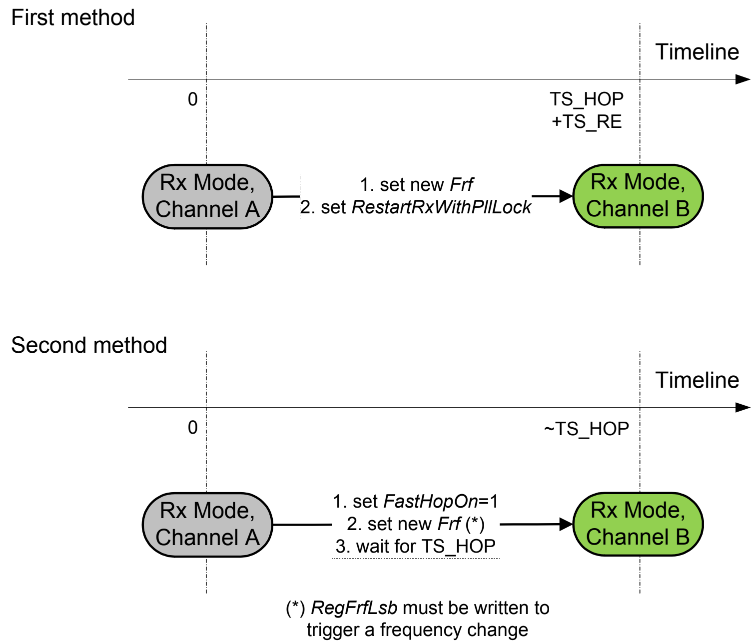


Figure 23. Receiver Hopping

The second method is quicker, and should be used if a very quick RF sniffing mechanism is implemented.

4.2.7. Tx to Tx

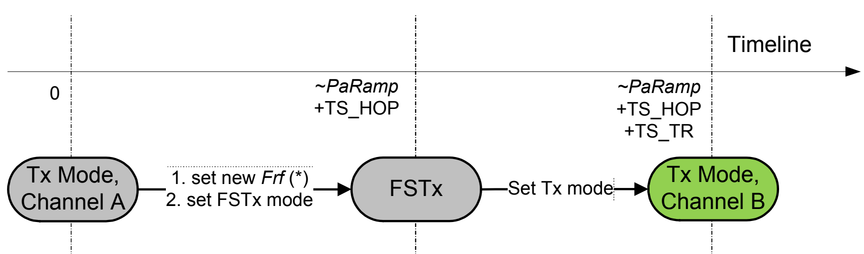


Figure 24. Transmitter Hopping

4.3. Receiver Startup Options

The SX1235 receiver can automatically control the gain of its receiver chain (AGC) and adjust its receiver LO frequency (AFC). Those processes are carried out on a packet-by-packet basis, and they occur:

- when the receiver is turned On
- when the Receiver is restarted upon user request, through the use of trigger bits *RestartRxWithoutPllLock* or *RestartRxWithPllLock*, in *RegRxConfig.*
- when the receiver is automatically restarted after the reception of a valid packet, or after a packet collision.

Automatic restart capabilities are detailed in section 4.4.

Several receiver startup options are offered in the state machine of the SX1235, and they are described in Table 24:

Table 24 Receiver Startup Options

Triggering Event	Realized Function	*AgcAutoOn*	*AfcAutoOn*	*RxTrigger (2:0)*
None	None	0	0	000
Rssi Interrupt	AGC	1	0	001
	AGC & AFC	1	1	001
PreambleDetect	AGC	1	0	110
	AGC & AFC	1	1	110
Rssi Interrupt & *PreambleDetect*	AGC	1	0	111
	AGC & AFC	1	1	111

When *AgcAutoOn*=0, the LNA gain is manually selected by choosing *LnaGain* bits in *RegLna.*

4.4. Receiver Restarting Methods

It may be useful to restart the receiver, for emayxample to prepare for the reception of a new signal whose strength may widely differ from the previous packet receiver, or whose carrier frequency may be different, required a new AFC. A few options are proposed:

4.4.1. Restart Upon User Request

At any point in time, when the device is in Receive mode, the user can restart the receiver; this is particularly useful in conjunction with the use of a Timeout, whereby the receiver would need restarting if it had not detected any incoming packet after a few milliseconds of channel scanning. Two options are available:

- No change in the Local Oscillator upon restart: the AFC is disabled, and the *Frf* register has not been changed through SPI before the restart instruction: set bit *RestartRxWithoutPllLock* in *RegRxConfig* to 1.
- Local Oscillator change upon restart: if AFC is enabled (*AfcAutoOn*=1), and/or the *Frf* register had been changed during the last Rx period: set bit *RestartRxWithPllLock* in *RegRxConfig* to 1.

Note ModeReady must be at logic level 1 for a new RestartRx command to be taken into account

4.4.2. Automatic Restart after valid Packet Reception

The bits *AutoRestartRxMode* in *RegSyncConfig* control the automatic restart feature of the SX1235 receiver, when a valid packet has been received:

- If *AutoRestartRxMode* = 00, the function is off, and the user should manually restart the receiver upon valid packet reception (see section 4.4.1).
- If *AutoRestartRxMode* = 01, after the user has emptied the FIFO following a *PayloadReady* interrupt, the receiver will automatically restart itself after a delay of *InterPacketRxDelay*, allowing for the distant transmitter to ramp down, hence avoiding a false RSSI detection on the “tail” of the previous packet.
- If *AutoRestartRxMode* = 10 should be used if the next reception is expected on a new frequency, i.e. *Frf* is changed after the reception of the previous packet. An additional delay is systematically added, in order for the PLL to lock at a new frequency.

4.4.3. Automatic Restart when Packet Collision is Detected

At any stage during reception, the receiver is able to spontaneously detect a packet collision, and restart itself. Collisions are detected by a sudden rise in received signal strength, detected by the RSSI blocks. This function can be useful in star network configurations, where a master node may be transmitted packet at random times, from different end-points located at various distances.

The collision detector is enabled by setting bit *RestartRxOnCollision* to 1.

The decision to restart the receiver is based on the detection of RSSI change. The sensitivity of the system can be adjusted in 1dB steps, with *RssiCollisionThreshold* in *RegRxConfig*.

4.5. Top Level Sequencer

Depending on the application, it is desirable to be able to change the mode of the circuit according to a predefined sequence without access to the serial interface. In order to define different sequences or scenarios, a user-programmable state machine, called Top Level Sequencer (Sequencer in short), can automatically control the chip modes.

The Sequencer is activated by setting the *SequencerStart* bit in *RegSeqConfig1* to 1 in Sleep or Standby mode (called initial mode).

It is also possible to force the Sequencer off by setting the *Stop* bit in *RegSeqConfig1* to 1 at any time.

Note SequencerStart and Stop bit must never be set at the same time.

4.5.1. Sequencer States

The Sequencer takes control of the chip operation over 4 possible states and 3 transitory states:

Table 25 Sequencer States

Sequencer State	Description
SequencerOff State	The Sequencer is not activated. Sending a *SequencerStart* command will launch it. When coming from **LowPowerSelection** state, the Sequencer will be Off, whilst the chip will return to its initial mode (either Sleep or Standby mode).
Idle State	The chip is in low-power mode, either *Standby* or *Sleep*, as defined by *IdleMode* in *RegSeqConfig1*. The Sequencer waits only for the *T1* interrupt.
Transmit State	The transmitter in on.
Receive State	The receiver in on.
PacketReceived	The receiver is on and a packet has been received. It is stored in the FIFO.
LowPowerSelection	Selects low power state (**SequencerOff** or **Idle** State)
RxTimeout	Defines the action to be taken on a RxTimeout interrupt. RxTimeout interrupt can be a *TimeoutRxRssi*, *TimeoutRxPreamble* or *TimeoutSignalSync* interrupt.

4.5.2. Sequencer Transitions

The transitions between sequencer states are listed in the forthcoming table.

Table 26 Sequencer Transition Options

Variable	Transition
IdleMode	Selects the chip mode during **Idle** state: 0: *Standby* mode 1: *Sleep* mode
FromStart	Controls the Sequencer transition when the *SequencerStart* bit is set to 1 in *Sleep* or *Standby* mode: 00: to **LowPowerSelection** 01: to **Receive** state 10: to **Transmit** state 11: to **Transmit** state on a *FifoThreshold* interrupt
LowPowerSelection	Selects Sequencer LowPower state after a *to LowPowerSelection* transition 0: **SequencerOff** state with chip on Initial mode 1: **Idle** state with chip on *Standby* or *Sleep* mode depending on **IdleMode** Note: Initial mode is the chip LowPower mode at Sequencer start.
FromIdle	Controls the Sequencer transition from the **Idle** state on a *T1* interrupt: 0: to **Transmit** state 1: to **Receive** state
FromTransmit	Controls the Sequencer transition from the **Transmit** state: 0: to **LowPowerSelection** on a *PacketSent* interrupt 1: to **Receive** state on a *PacketSent* interrupt
FromReceive	Controls the Sequencer transition from the **Receive** state: 000 and 111: unused 001: to **PacketReceived** state on a *PayloadReady* interrupt 010: to **LowPowerSelection** on a *PayloadReady* interrupt 011: to **PacketReceived** state on a *CrcOk* interrupt. If CRC is wrong (corrupted packet, with CRC on but CrcAutoClearOn is off), the PayloadReady interrupt will drive the sequencer to RxTimeout state. 100: to **SequencerOff** state on a *Rssi* interrupt 101: to **SequencerOff** state on a *SyncAddress* interrupt 110: to **SequencerOff** state on a *PreambleDetect* interrupt Irrespective of this setting, transition to **LowPowerSelection** on a *T2* interrupt
FromRxTimeout	Controls the state-machine transition from the **Receive** state on a *RxTimeout* interrupt (and on *PayloadReady* if **FromReceive** = 011): 00: to **Receive** state via *ReceiveRestart* 01: to **Transmit** state 10: to **LowPowerSelection** 11: to **SequencerOff** state Note: RxTimeout interrupt is a *TimeoutRxRssi*, *TimeoutRxPreamble* or *TimeoutSignalSync* interrupt.
FromPacketReceived	Controls the state-machine transition from the **PacketReceived** state: 000: to **SequencerOff** state 001: to **Transmit** on a *FifoEmpty* interrupt 010: to **LowPowerSelection** 011: to **Receive** via *FS* mode, if frequency was changed 100: to **Receive** state (no frequency change)

4.5.3. Timers

Two timers (Timer1 and Timer2) are also available in order to define periodic sequences. These timers are used to generate interrupts, which can trigger transitions of the Sequencer.

T1 interrupt is generated (Timer1Resolution * Timer1Coefficient) after ***T2* interrupt** or ***SequencerStart***. command.
T2 interrupt is generated (Timer2Resolution * Timer2Coefficient) after ***T1* interrupt**.

The timers' mechanism is summarized on the following diagram.

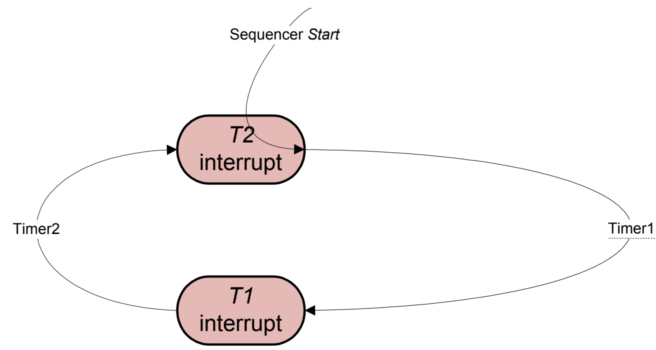


Figure 25. Timer1 and Timer2 Mechanism

Note The timer sequence is completed independently of the actual Sequencer state. Thus, both timers need to be on to achieve a periodic cycling.

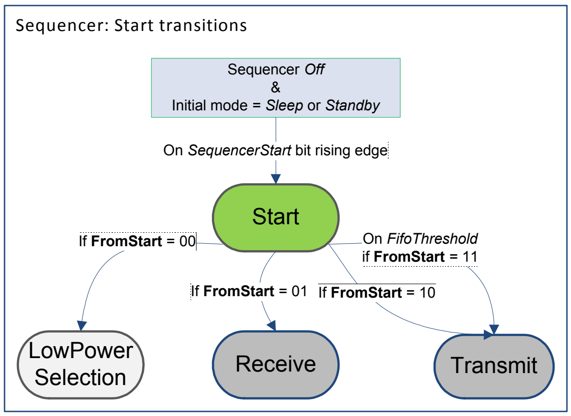
Table 27 Sequencer Timer Settings

Variable	**Description**
Timer1Resolution	Resolution of Timer1 00: disabled 01: 64 us 10: 4.1 ms 11: 262 ms
Timer2Resolution	Resolution of Timer2 00: disabled 01: 64 us 10: 4.1 ms 11: 262 ms
Timer1Coefficient	Multiplying coefficient for Timer1
Timer2Coefficient	Multiplying coefficient for Timer2

4.5.4. Sequencer State Machine

The following graphs summarize every possible transition between each Sequencer state. The Sequencer states are highlighted in grey. The transitions are represented by arrows. The condition activating them is described over the transition arrow. For better readability, the start transitions are separated from the rest of the graph.

Transitory states are highlighted in light grey, and exit states are represented in red. It is also possible to force the Sequencer off by setting the *Stop* bit in *RegSeqConfig1* to 1 at any time.



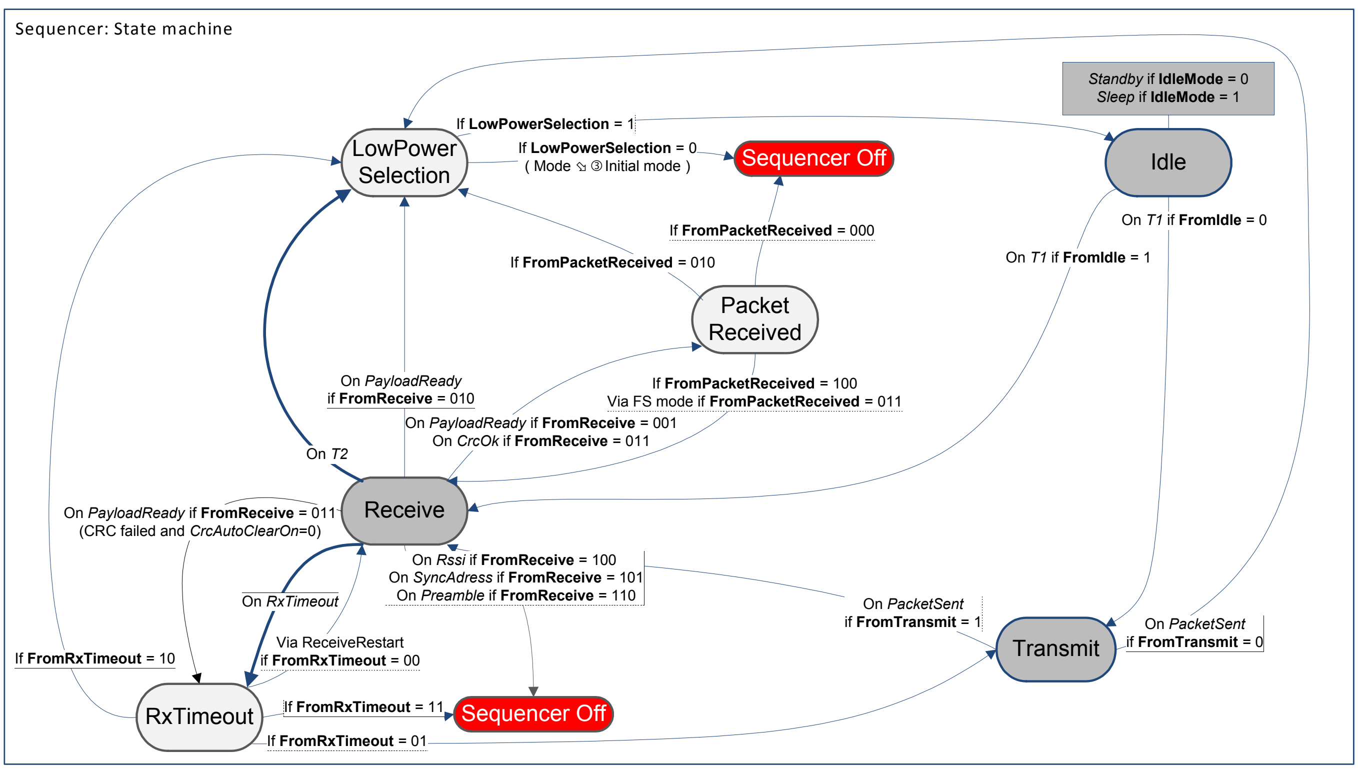


Figure 26. Sequencer State Machine

Use cases of the Top Sequencer are detailed in Section 7.

5. Data Processing

5.1. Overview

5.1.1. Block Diagram

Figure below illustrates the SX1235 data processing circuit. Its role is to interface the data to/from the modulator/demodulator and the uC access points (SPI and DIO pins). It also controls all the configuration registers.

The circuit contains several control blocks which are described in the following paragraphs.

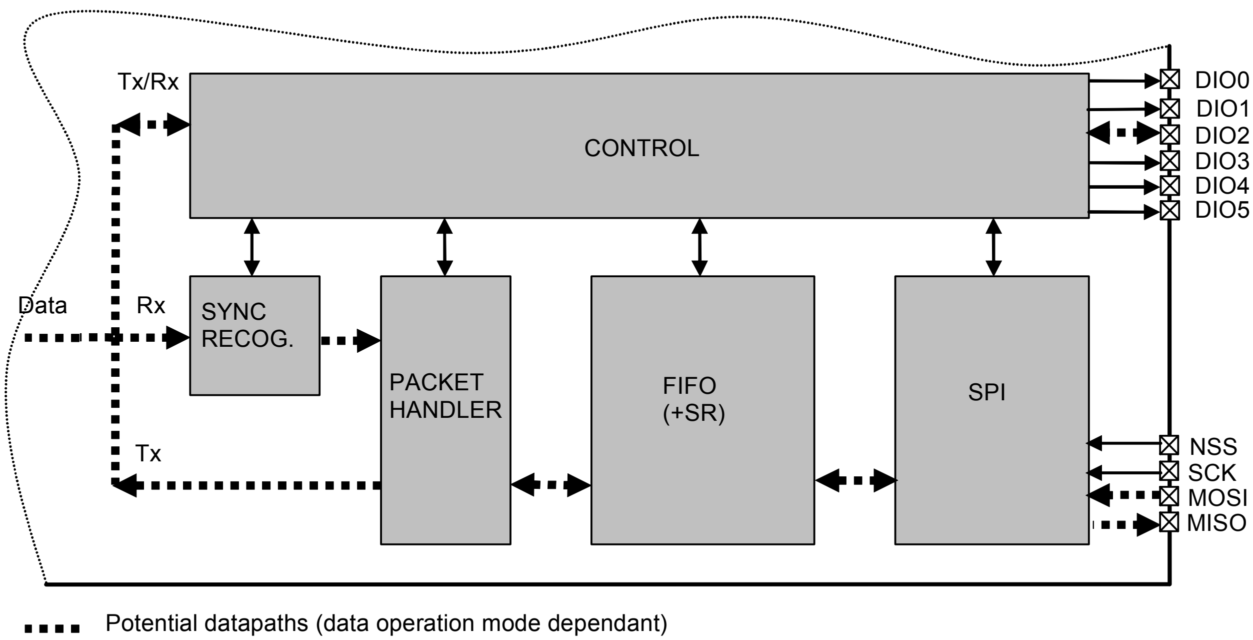


Figure 27. SX1235 Data Processing Conceptual View

The SX1235 implements several data operation modes, each with their own data path through the data processing section. Depending on the data operation mode selected, some control blocks are active whilst others remain disabled.

5.1.2. Data Operation Modes

The SX1235 has two different data operation modes selectable by the user:

- Continuous mode: each bit transmitted or received is accessed in real time at the DIO2/DATA pin. This mode may be used if adequate external signal processing is available.
- Packet mode (recommended): user only provides/retrieves payload bytes to/from the FIFO. The packet is automatically built with preamble, Sync word, and optional CRC and DC-free encoding schemes The reverse operation is performed in reception. The uC processing overhead is hence significantly reduced compared to Continuous mode. Depending on the optional features activated (CRC, etc) the maximum payload length is limited to 255, 2047 bytes or unlimited.

Each of these data operation modes is fully described in the following sections.

5.2. Control Block Description

5.2.1. SPI Interface

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implemented.

Three access modes to the registers are provided:

- SINGLE access: an address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the begin of the frame and goes high after the data byte.
- BURST access: the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. This mode is available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.
- FIFO access: if the address byte corresponds to the address of the FIFO, then succeeding data byte will address the FIFO. The address is not automatically incremented but is memorized and does not need to be sent between each data byte. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.

Figure below shows a typical SPI single access to a register.

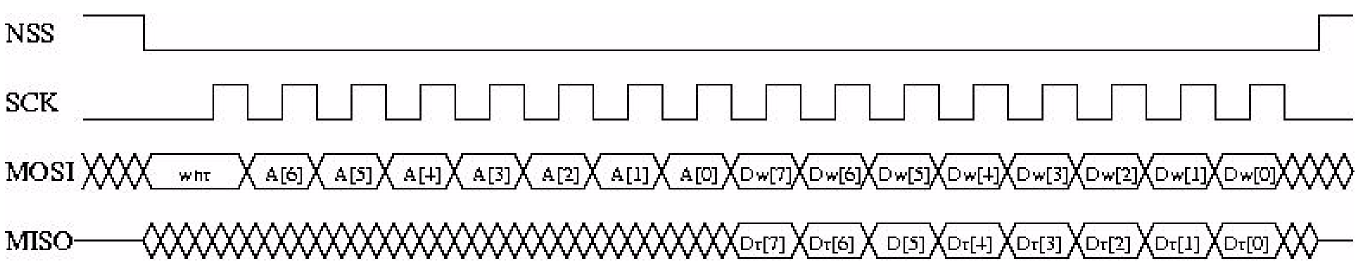


Figure 28. SPI Timing Diagram (single access)

MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.

A transfer always starts by the NSS pin going low. MISO is high impedance when NSS is high.

The first byte is the address byte. It is made of:

- wnr bit, which is 1 for write access and 0 for read access
- 7 bits of address, MSB first

The second byte is a data byte, either sent on MOSI by the master in case of a write access, or received by the master on MISO in case of read access. The data byte is transmitted MSB first.

Proceeding bytes may be sent on MOSI (for write access) or received on MISO (for read access) without rising NSS and re-sending the address. In FIFO mode, if the address was the FIFO address then the bytes will be written / read at the FIFO address. In Burst mode, if the address was not the FIFO address, then it is automatically incremented at each new byte received.

The frame ends when NSS goes high. The next frame must start with an address byte. The SINGLE access mode is actually a special case of FIFO / BURST mode with only 1 data byte transferred.

During the write access, the byte transferred from the slave to the master on the MISO line is the value of the written register before the write operation.

5.2.2. FIFO

5.2.2.1. Overview and Shift Register (SR)

In packet mode of operation, both data to be transmitted and that has been received are stored in a configurable FIFO (First In First Out) device. It is accessed via the SPI interface and provides several interrupts for transfer management.

The FIFO is 1 byte wide hence it only performs byte (parallel) operations, whereas the demodulator functions serially. A shift register is therefore employed to interface the two devices. In transmit mode it takes bytes from the FIFO and outputs them serially (MSB first) at the programmed bit rate to the modulator. Similarly, in Rx the shift register gets bit by bit data from the demodulator and writes them byte by byte to the FIFO. This is illustrated in figure below.

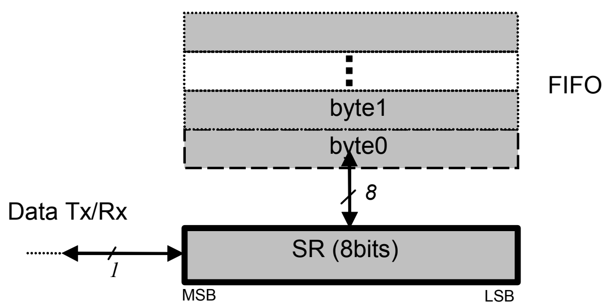


Figure 29. FIFO and Shift Register (SR)

Note *When switching to Sleep mode, the FIFO can only be used once the ModeReady flag is set (quasi immediate from all modes except from Tx)*

5.2.2.2. Size

The FIFO size is fixed to 64 bytes.

5.2.2.3. Interrupt Sources and Flags

- *FifoEmpty*: *FifoEmpty* interrupt source is high when byte 0, i.e. whole FIFO, is empty. Otherwise it is low. Note that when retrieving data from the FIFO, *FifoEmpty* is updated on NSS falling edge, i.e. when *FifoEmpty* is updated to low state the currently started read operation must be completed. In other words, *FifoEmpty* state must be checked after each read operation for a decision on the next one (*FifoEmpty* = 0: more byte(s) to read; *FifoEmpty* = 1: no more byte to read).
- *FifoFull*: *FifoFull* interrupt source is high when the last FIFO byte, i.e. the whole FIFO, is full. Otherwise it is low.
- *FifoOverrunFlag*: *FifoOverrunFlag* is set when a new byte is written by the user (in Tx or Standby modes) or the SR (in Rx mode) while the FIFO is already full. Data is lost and the flag should be cleared by writing a 1, note that the FIFO will also be cleared.
- *PacketSent*: *PacketSent* interrupt source goes high when the SR's last bit has been sent.
- *FifoLevel*: Threshold can be programmed by *FifoThreshold* in *RegFifoThresh*. Its behavior is illustrated in figure below.

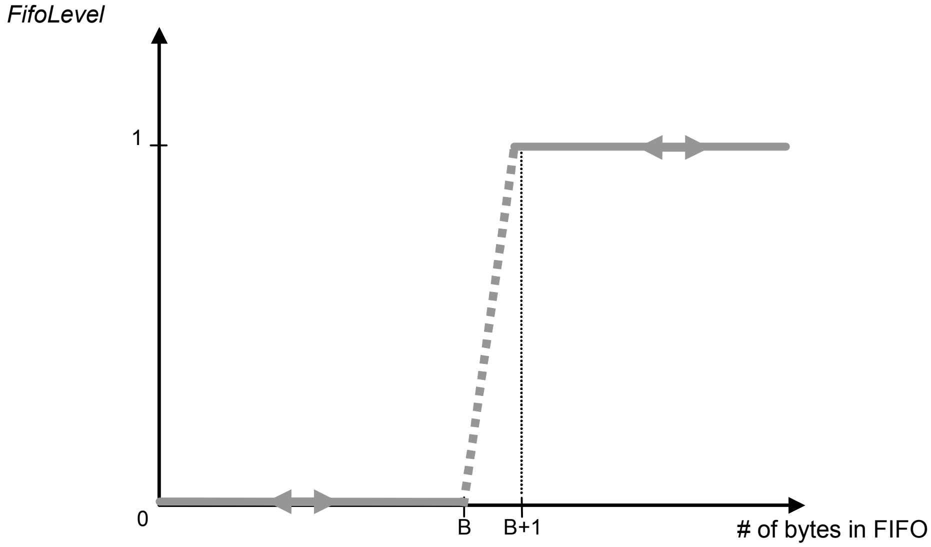


Figure 30. FifoLevel IRQ Source Behavior

Note - FifoLevel interrupt is updated only after a read or write operation on the FIFO. Thus the interrupt cannot be dynamically updated by only changing the FifoThreshold parameter

- FifoLevel interrupt is valid as long as FifoFull does not occur. An empty FIFO will restore its normal operation

5.2.2.4. FIFO Clearing

Table below summarizes the status of the FIFO when switching between different modes

Table 28 Status of FIFO when Switching Between Different Modes of the Chip

From	To	FIFO status	Comments
Stdby	Sleep	Not cleared	
Sleep	Stdby	Not cleared	
Stdby/Sleep	Tx	Not cleared	To allow the user to write the FIFO in Stdby/Sleep before Tx
Stdby/Sleep	Rx	Cleared	
Rx	Tx	Cleared	
Rx	Stdby/Sleep	Not cleared	To allow the user to read FIFO in Stdby/Sleep mode after Rx
Tx	Any	Cleared	

5.2.3. Sync Word Recognition

5.2.3.1. Overview

Sync word recognition (also called Pattern recognition) is activated by setting *SyncOn* in *RegSyncConfig*. The bit synchronizer must also be activated in Continuous mode (automatically done in Packet mode).

The block behaves like a shift register; it continuously compares the incoming data with its internally programmed Sync word and sets *SyncAddressMatch* when a match is detected. This is illustrated in Figure 31 below.

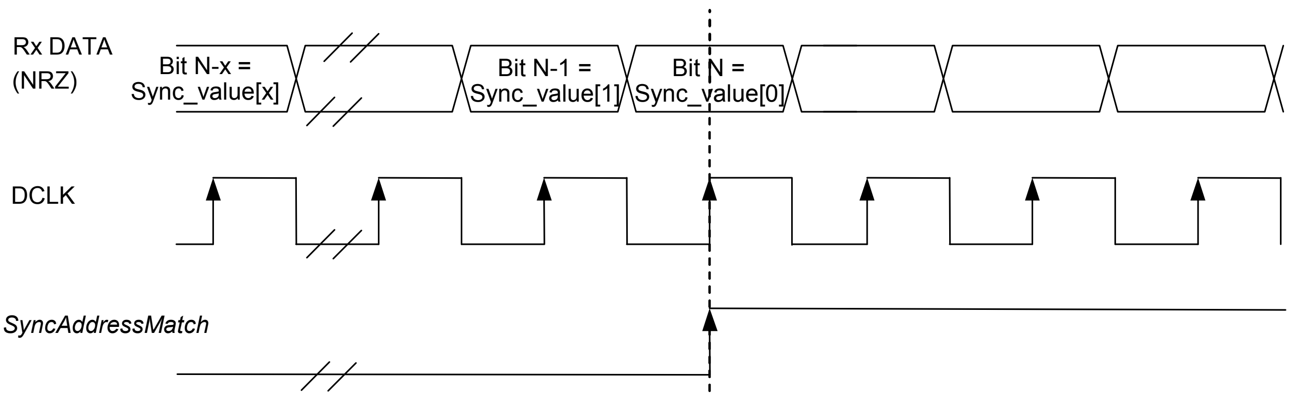


Figure 31. Sync Word Recognition

During the comparison of the demodulated data, the first bit received is compared with bit 7 (MSB) of *RegSyncValue1* and the last bit received is compared with bit 0 (LSB) of the last byte whose address is determined by the length of the Sync word.

When the programmed Sync word is detected the user can assume that this incoming packet is for the node and can be processed accordingly.

SyncAddressMatch is cleared when leaving Rx or FIFO is emptied.

5.2.3.2. Configuration

- Size: Sync word size can be set from 1 to 8 bytes (i.e. 8 to 64 bits) via *SyncSize* in *RegSyncConfig*. In Packet mode this field is also used for Sync word generation in Tx mode.
- Value: The Sync word value is configured in *SyncValue(63:0)*. In Packet mode this field is also used for Sync word generation in Tx mode.

Note SyncValue choices containing 0x00 bytes are not allowed

5.2.4. Packet Handler

The packet handler is the block used in Packet mode. Its functionality is fully described in section 5.5.

5.2.5. Control

The control block configures and controls the full chip's behavior according to the settings programmed in the configuration registers.

5.3. Digital IO Pins Mapping

Six general purpose IO pins are available on the SX1235, and their configuration in Continuous or Packet mode is controlled through *RegDioMapping1* and *RegDioMapping2*.

Table 29 DIO Mapping, Continuous Mode

<table>
<tr><th></th><th>DIOx Mapping</th><th>Sleep</th><th>Standby</th><th>FSRx/Tx</th><th>Rx</th><th>Tx</th></tr>
<tr><td rowspan="4">DIO0</td><td>00</td><td colspan="3">-</td><td>SyncAddress</td><td>TxReady</td></tr>
<tr><td>01</td><td colspan="3">-</td><td>Rssi / PreambleDetect</td><td>-</td></tr>
<tr><td>10</td><td colspan="3">-</td><td>RxReady</td><td>TxReady</td></tr>
<tr><td>11</td><td colspan="5">-</td></tr>
<tr><td rowspan="4">DIO1</td><td>00</td><td colspan="3">-</td><td colspan="2">Dclk</td></tr>
<tr><td>01</td><td colspan="3">-</td><td>Rssi / PreambleDetect</td><td>-</td></tr>
<tr><td>10</td><td colspan="5">-</td></tr>
<tr><td>11</td><td colspan="5">-</td></tr>
<tr><td rowspan="4">DIO2</td><td>00</td><td colspan="3">-</td><td colspan="2">Data</td></tr>
<tr><td>01</td><td colspan="3">-</td><td colspan="2">Data</td></tr>
<tr><td>10</td><td colspan="3">-</td><td colspan="2">Data</td></tr>
<tr><td>11</td><td colspan="3">-</td><td colspan="2">Data</td></tr>
<tr><td rowspan="4">DIO3</td><td>00</td><td colspan="3">-</td><td>Timeout</td><td>-</td></tr>
<tr><td>01</td><td colspan="3">-</td><td>Rssi / PreambleDetect</td><td>-</td></tr>
<tr><td>10</td><td colspan="5">-</td></tr>
<tr><td>11</td><td>-</td><td colspan="2">TempChange / LowBat</td><td colspan="2">TempChange / LowBat</td></tr>
<tr><td rowspan="4">DIO4</td><td>00</td><td colspan="2">-</td><td colspan="3">TempChange / LowBat</td></tr>
<tr><td>01</td><td colspan="2">-</td><td colspan="3">PllLock</td></tr>
<tr><td>10</td><td colspan="3">-</td><td>TimeOut</td><td>-</td></tr>
<tr><td>11</td><td>-</td><td colspan="2">ModeReady</td><td colspan="2">ModeReady</td></tr>
<tr><td rowspan="4">DIO5</td><td>00</td><td>ClkOut if RC</td><td colspan="2">ClkOut</td><td colspan="2">ClkOut</td></tr>
<tr><td>01</td><td colspan="2">-</td><td colspan="3">PllLock</td></tr>
<tr><td>10</td><td colspan="3">-</td><td>Rssi / PreambleDetect</td><td>-</td></tr>
<tr><td>11</td><td>-</td><td colspan="2">ModeReady</td><td colspan="2">ModeReady</td></tr>
</table>

Table 30 DIO Mapping, Packet Mode

<table>
<tr><th></th><th>DIOx Mapping</th><th>Sleep</th><th>Standby</th><th>FSRx/Tx</th><th>Rx</th><th>Tx</th></tr>
<tr><td rowspan="4">DIO0</td><td>00</td><td colspan="3">-</td><td>PayloadReady</td><td>PacketSent</td></tr>
<tr><td>01</td><td colspan="3">-</td><td>CrcOk</td><td>-</td></tr>
<tr><td>10</td><td colspan="5">-</td></tr>
<tr><td>11</td><td>-</td><td colspan="2">TempChange / LowBat</td><td colspan="2">TempChange / LowBat</td></tr>
<tr><td rowspan="4">DIO1</td><td>00</td><td colspan="2">FifoLevel</td><td>FifoLevel</td><td colspan="2">FifoLevel</td></tr>
<tr><td>01</td><td colspan="2">FifoEmpty</td><td>FifoEmpty</td><td colspan="2">FifoEmpty</td></tr>
<tr><td>10</td><td colspan="2">FifoFull</td><td>FifoFull</td><td colspan="2">FifoFull</td></tr>
<tr><td>11</td><td colspan="5">-</td></tr>
<tr><td rowspan="4">DIO2</td><td>00</td><td colspan="2">FifoFull</td><td>FifoFull</td><td colspan="2">FifoFull</td></tr>
<tr><td>01</td><td colspan="3">-</td><td>RxReady</td><td>-</td></tr>
<tr><td>10</td><td colspan="3">FifoFull</td><td>TimeOut</td><td>FifoFull</td></tr>
<tr><td>11</td><td colspan="3">FifoFull</td><td>SyncAddress</td><td>FifoFull</td></tr>
<tr><td rowspan="4">DIO3</td><td>00</td><td colspan="2">FifoEmpty</td><td>FifoEmpty</td><td colspan="2">FifoEmpty</td></tr>
<tr><td>01</td><td colspan="4">-</td><td>TxReady</td></tr>
<tr><td>10</td><td colspan="2">FifoEmpty</td><td>FifoEmpty</td><td colspan="2">FifoEmpty</td></tr>
<tr><td>11</td><td colspan="2">FifoEmpty</td><td>FifoEmpty</td><td colspan="2">FifoEmpty</td></tr>
<tr><td rowspan="4">DIO4</td><td>00</td><td>-</td><td colspan="2">TempChange / LowBat</td><td colspan="2">TempChange / LowBat</td></tr>
<tr><td>01</td><td colspan="2">-</td><td colspan="3">PllLock</td></tr>
<tr><td>10</td><td colspan="3">-</td><td>TimeOut</td><td>-</td></tr>
<tr><td>11</td><td colspan="3">-</td><td>Rssi / PreambleDetect</td><td>-</td></tr>
<tr><td rowspan="4">DIO5</td><td>00</td><td>ClkOut if RC</td><td colspan="2">ClkOut</td><td colspan="2">ClkOut</td></tr>
<tr><td>01</td><td colspan="2">-</td><td colspan="3">PllLock</td></tr>
<tr><td>10</td><td colspan="3">-</td><td colspan="2">Data</td></tr>
<tr><td>11</td><td>-</td><td colspan="2">ModeReady</td><td colspan="2">ModeReady</td></tr>
</table>

5.4. Continuous Mode

5.4.1. General Description

As illustrated in Figure 32, in Continuous mode the NRZ data to (from) the (de)modulator is directly accessed by the uC on the bidirectional DIO2/DATA pin. The FIFO and packet handler are thus inactive.

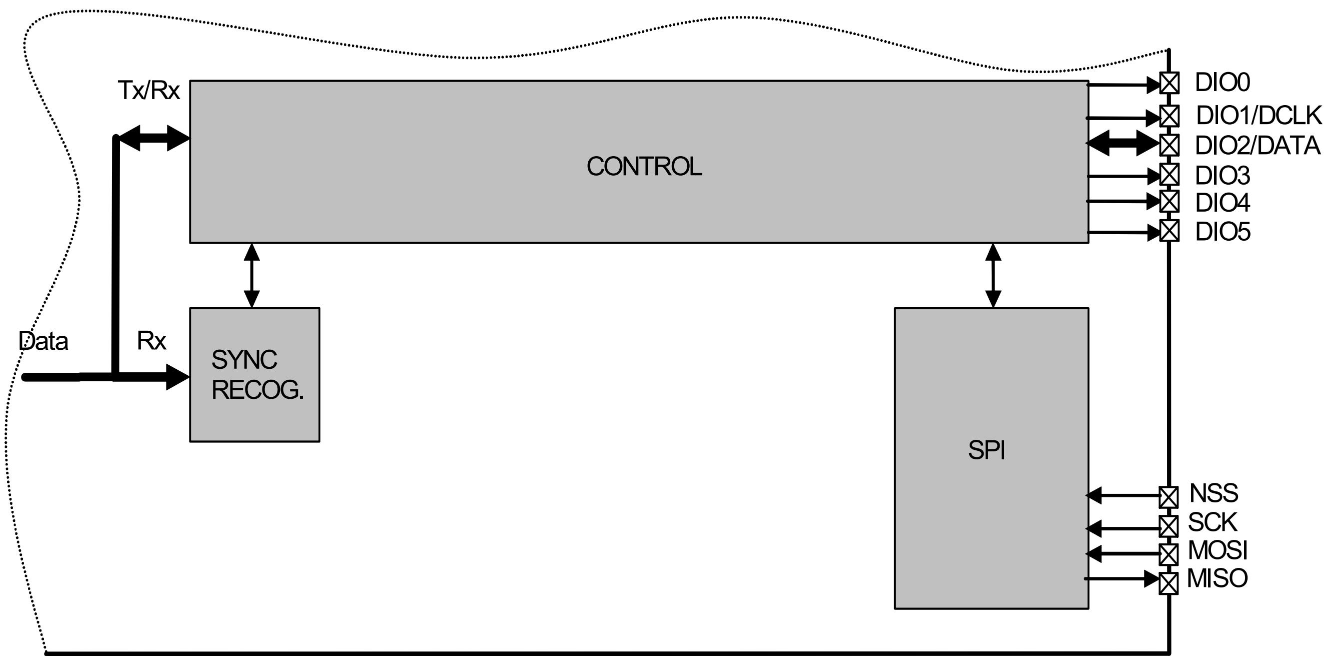


Figure 32. Continuous Mode Conceptual View

5.4.2. Tx Processing

In Tx mode, a synchronous data clock for an external uC is provided on DIO1/DCLK pin. Clock timing with respect to the data is illustrated in Figure 33. DATA is internally sampled on the rising edge of DCLK so the uC can change logic state anytime outside the grayed out setup/hold zone.

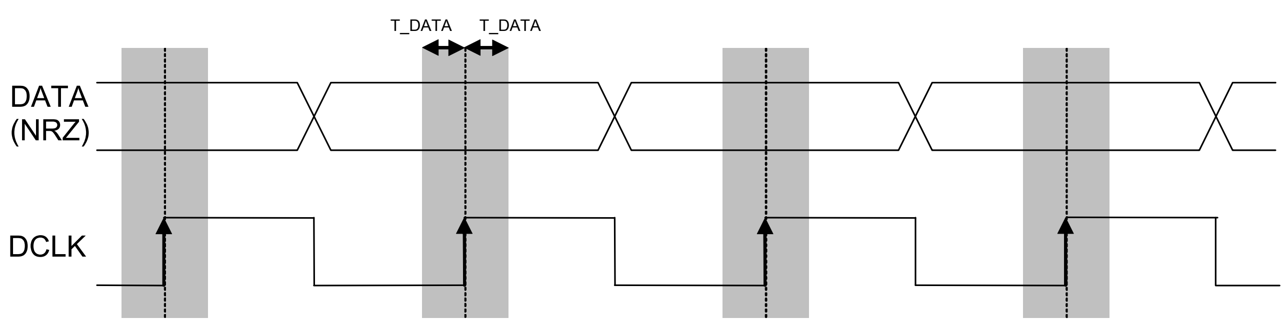


Figure 33. Tx Processing in Continuous Mode

Note the use of DCLK is required when the modulation shaping is enabled (see section 3.4.5).

5.4.3. Rx Processing

If the bit synchronizer is disabled, the raw demodulator output is made directly available on DATA pin and no DCLK signal is provided.

Conversely, if the bit synchronizer is enabled, synchronous cleaned data and clock are made available respectively on DIO2/DATA and DIO1/DCLK pins. DATA is sampled on the rising edge of DCLK and updated on the falling edge as illustrated below.

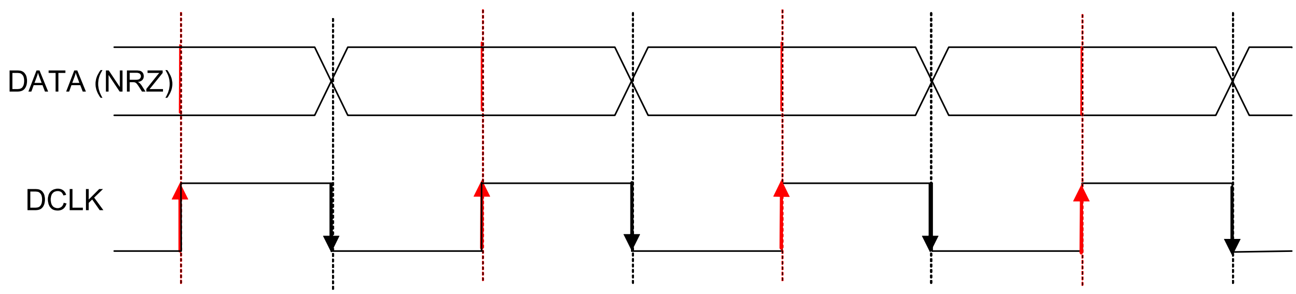


Figure 34. Rx Processing in Continuous Mode

Note in Continuous mode it is always recommended to enable the bit synchronizer to clean the DATA signal even if the DCLK signal is not used by the uC (bit synchronizer is automatically enabled in Packet mode).

5.5. Packet Mode

5.5.1. General Description

In Packet mode the NRZ data to (from) the (de)modulator is not directly accessed by the uC but stored in the FIFO and accessed via the SPI interface.

In addition, the SX1235 packet handler performs several packet oriented tasks such as Preamble and Sync word generation, CRC calculation/check, whitening/dewhitening of data, Manchester encoding/decoding, address filtering, etc. This simplifies software and reduces uC overhead by performing these repetitive tasks within the RF chip itself.

Another important feature is ability to fill and empty the FIFO in Sleep/Stdby mode, ensuring optimum power consumption and adding more flexibility for the software.

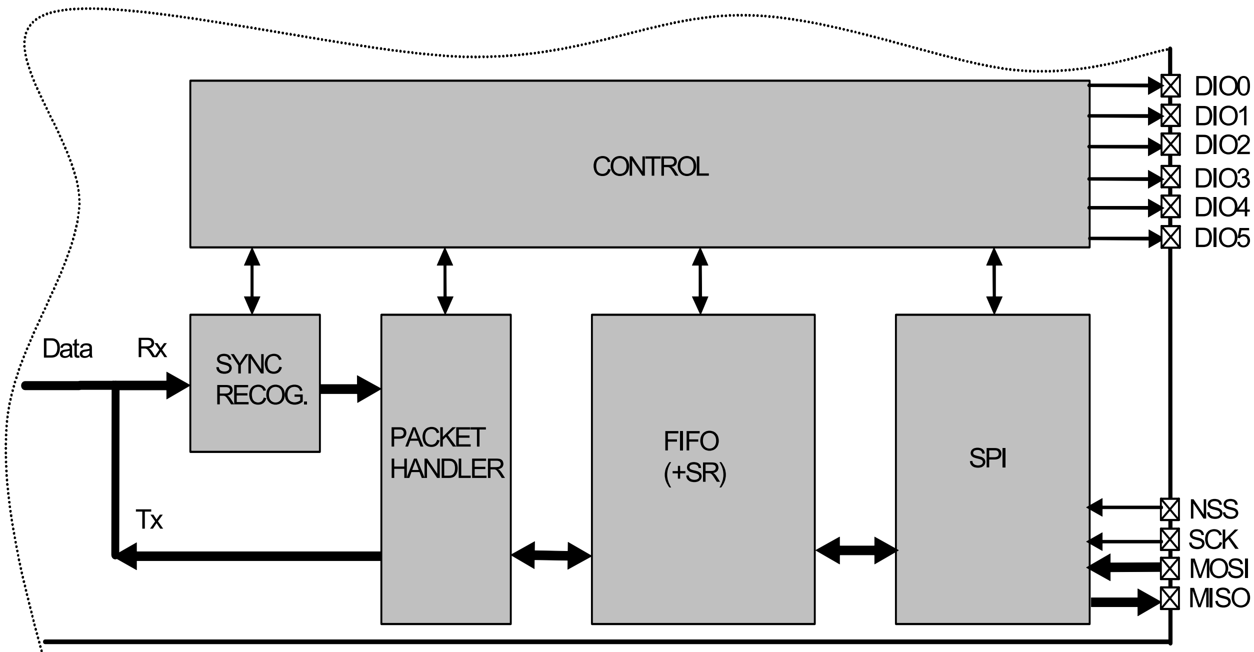


Figure 35. Packet Mode Conceptual View

Note The Bit Synchronizer is automatically enabled in Packet mode.

5.5.2. Packet Format

5.5.2.1. Fixed Length Packet Format

Fixed length packet format is selected when bit *PacketFormat* is set to 0 and *PayloadLength* is set to any value greater than 0.

In applications where the packet length is fixed in advance, this mode of operation may be of interest to minimize RF overhead (no length byte field is required). All nodes, whether Tx only, Rx only, or Tx/Rx should be programmed with the same packet length value.

The length of the payload is limited to 2047 bytes.

The length programmed in *PayloadLength* relates only to the payload which includes the message and the optional address byte. In this mode, the payload must contain at least one byte, i.e. address or message byte.

An illustration of a fixed length packet is shown below. It contains the following fields:

- Preamble (1010...)
- Sync word (Network ID)
- Optional Address byte (Node ID)
- Message data
- Optional 2-bytes CRC checksum

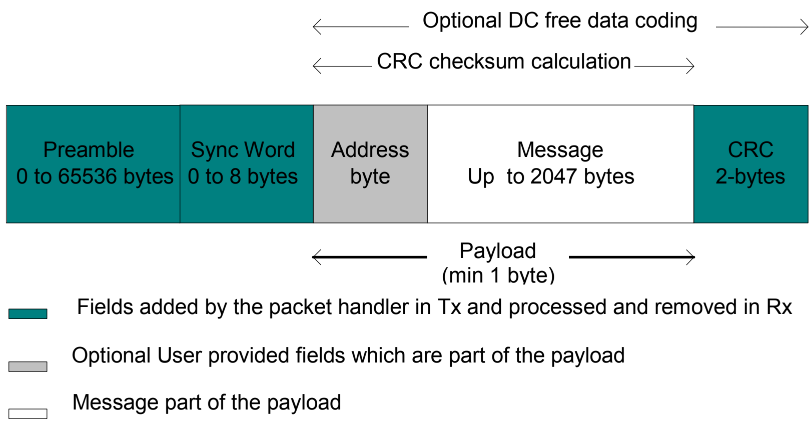


Figure 36. Fixed Length Packet Format

5.5.2.2. Variable Length Packet Format

Variable length packet format is selected when bit *PacketFormat* is set to 1.

This mode is useful in applications where the length of the packet is not known in advance and can vary over time. It is then necessary for the transmitter to send the length information together with each packet in order for the receiver to operate properly.

In this mode the length of the payload, indicated by the length byte, is given by the first byte of the FIFO and is limited to 255 bytes. Note that the length byte itself is not included in its calculation. In this mode, the payload must contain at least 2 bytes, i.e. length + address or message byte.

An illustration of a variable length packet is shown below. It contains the following fields:

- Preamble (1010...)
- Sync word (Network ID)
- Length byte
- Optional Address byte (Node ID)
- Message data

- Optional 2-bytes CRC checksum

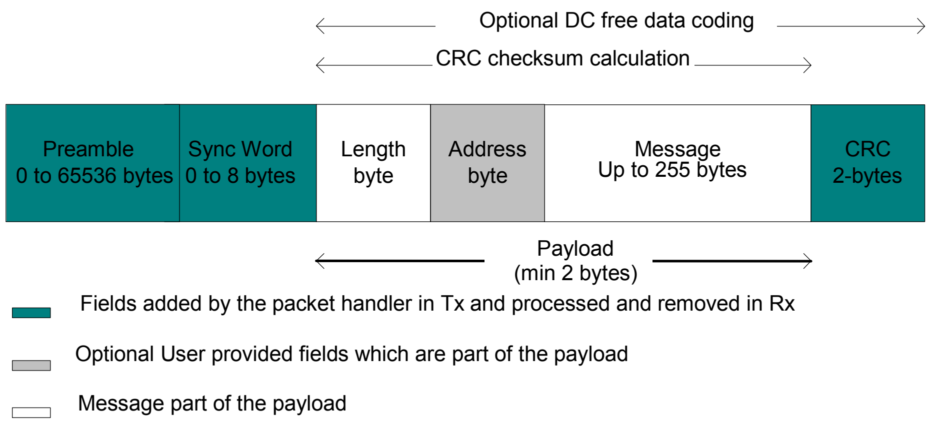


Figure 37. Variable Length Packet Format

5.5.2.3. Unlimited Length Packet Format

Unlimited length packet format is selected when bit *PacketFormat* is set to 0 and *PayloadLength* is set to 0.

The user can then transmit and receive packet of arbitrary length and *PayloadLength* register is not used in Tx/Rx modes for counting the length of the bytes transmitted/received.

In Tx the data is transmitted depending on the *TxStartCondition* bit. On the Rx side the data processing features like Address filtering, Manchester encoding and data whitening are not available if the sync pattern length is set to zero (*SyncOn = 0*). The filling of the FIFO in this case can be controlled by the bit *FifoFillCondition*. The CRC detection in Rx is also not supported in this mode of the packet handler, however CRC generation in Tx is operational. The interrupts like *CrcOk* & *PayloadReady* are not available either.

An unlimited length packet is made up of the following fields:

- Preamble (1010...).
- Sync word (Network ID).
- Optional Address byte (Node ID).
- Message data
- Optional 2-bytes CRC checksum (Tx only)

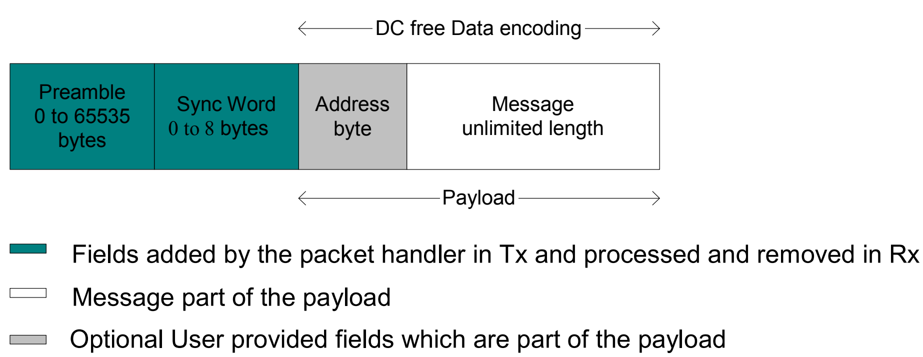


Figure 38. Unlimited Length Packet Format

5.5.3. Tx Processing

In Tx mode the packet handler dynamically builds the packet by performing the following operations on the payload available in the FIFO:

- Add a programmable number of preamble bytes
- Add a programmable Sync word
- Optionally calculating CRC over complete payload field (optional length byte + optional address byte + message) and appending the 2 bytes checksum.
- Optional DC-free encoding of the data (Manchester or whitening)

Only the payload (including optional address and length fields) is required to be provided by the user in the FIFO.

The transmission of packet data is initiated by the Packet Handler only if the chip is in Tx mode and the transmission condition defined by *TxStartCondition* is fulfilled. If transmission condition is not fulfilled then the packet handler transmits a preamble sequence until the condition is met. This happens only if the preamble length /= 0, otherwise it transmits a zero or one until the condition is met to transmit the packet data.

The transmission condition itself is defined as:

- if *TxStartCondition* = 1, the packet handler waits until the first byte is written into the FIFO, then it starts sending the preamble followed by the sync word and user payload
- If *TxStartCondition* = 0, the packet handler waits until the number of bytes written in the FIFO is equal to the number defined in *RegFifoThresh* + 1
- If the condition for transmission was already fulfilled i.e. the FIFO was filled in Sleep/Stdby then the transmission of packet starts immediately on enabling Tx

5.5.4. Rx Processing

In Rx mode the packet handler extracts the user payload to the FIFO by performing the following operations:

- Receiving the preamble and stripping it off
- Detecting the Sync word and stripping it off
- Optional DC-free decoding of data
- Optionally checking the address byte
- Optionally checking CRC and reflecting the result on *CrcOk.*

Only the payload (including optional address and length fields) is made available in the FIFO.

When the Rx mode is enabled the demodulator receives the preamble followed by the detection of sync word. If fixed length packet format is enabled then the number of bytes received as the payload is given by the *PayloadLength* parameter.

In variable length mode the first byte received after the sync word is interpreted as the length of the received packet. The internal length counter is initialized to this received length. The *PayloadLength* register is set to a value which is greater than the maximum expected length of the received packet. If the received length is greater than the maximum length stored in *PayloadLength* register the packet is discarded otherwise the complete packet is received.

If the address check is enabled then the second byte received in case of variable length and first byte in case of fixed length is the address byte. If the address matches to the one in the *NodeAddress* field, reception of the data continues otherwise it's stopped. The CRC check is performed if *CrcOn* = 1 and the result is available in *CrcOk* indicating that the CRC was successful. An interrupt (*PayloadReady*) is also generated on DIO0 as soon as the payload is available in the FIFO. The payload available in the FIFO can also be read in Sleep/Standby mode.

If the CRC fails the *PayloadReady* interrupt is not generated and the FIFO is cleared. This function can be overridden by setting *CrcAutoClearOff* = 1, forcing the availability of *PayloadReady* interrupt and the payload in the FIFO even if the CRC fails.

5.5.5. Handling Large Packets

When *PayloadLength* exceeds FIFO size (64 bytes) whether in fixed, variable or unlimited length packet format, in addition to *PacketSent* in Tx and *PayloadReady* or *CrcOk* in Rx, the FIFO interrupts/flags can be used as described below:

- For Tx:

FIFO can be prefilled in Sleep/Standby but must be refilled "on-the-fly" during Tx with the rest of the payload.

1) Prefill FIFO (in Sleep/Standby first or directly in Tx mode) until *FifoThreshold* or *FifoFull* is set

2) In Tx, wait for *FifoThreshold* or *FifoEmpty* to be set (i.e. FIFO is nearly empty)

3) Write bytes into the FIFO until *FifoThreshold* or *FifoFull* is set.

4) Continue to step 2 until the entire message has been written to the FIFO (*PacketSent* will fire when the last bit of the packet has been sent).

- For Rx:

FIFO must be unfilled "on-the-fly" during Rx to prevent FIFO overrun.

1) Start reading bytes from the FIFO when *FifoEmpty* is cleared or *FifoThreshold* becomes set.

2) Suspend reading from the FIFO if *FifoEmpty* fires before all bytes of the message have been read

3) Continue to step 1 until *PayloadReady* or *CrcOk* fires

4) Read all remaining bytes from the FIFO either in Rx or Sleep/Standby mode

5.5.6. Packet Filtering

The SX1235 packet handler offers several mechanisms for packet filtering, ensuring that only useful packets are made available to the uC, reducing significantly system power consumption and software complexity.

5.5.6.1. Sync Word Based

Sync word filtering/recognition is used for identifying the start of the payload and also for network identification. As previously described, the Sync word recognition block is configured (size, value) in *RegSyncConfig* and *RegSyncValue(i)* registers. This information is used, both for appending Sync word in Tx, and filtering packets in Rx.

Every received packet which does not start with this locally configured Sync word is automatically discarded and no interrupt is generated.

When the Sync word is detected, payload reception automatically starts and *SyncAddressMatch* is asserted.

Note Sync Word values containing 0x00 byte(s) are forbidden

5.5.6.2. Address Based

Address filtering can be enabled via the *AddressFiltering* bits. It adds another level of filtering, above Sync word (i.e. Sync must match first), typically useful in a multi-node networks where a network ID is shared between all nodes (Sync word) and each node has its own ID (address).

Two address based filtering options are available:

- *AddressFiltering = 01*: Received address field is compared with internal register *NodeAddress*. If they match then the packet is accepted and processed, otherwise it is discarded.
- *AddressFiltering = 10*: Received address field is compared with internal registers *NodeAddress* and *BroadcastAddress*. If either is a match, the received packet is accepted and processed, otherwise it is discarded. This additional check with a constant is useful for implementing broadcast in a multi-node networks

Please note that the received address byte, as part of the payload, is not stripped off the packet and is made available in the FIFO. In addition, *NodeAddress* and *AddressFiltering* only apply to Rx. On Tx side, if address filtering is expected, the address byte should simply be put into the FIFO like any other byte of the payload.

As address filtering requires a Sync word match, both features share the same interrupt flag *SyncAddressMatch*.

5.5.6.3. Length Based

In variable length Packet mode, *PayloadLength* must be programmed with the maximum payload length permitted. If received length byte is smaller than this maximum then the packet is accepted and processed, otherwise it is discarded.

Please note that the received length byte, as part of the payload, is not stripped off the packet and is made available in the FIFO.

To disable this function the user should set the value of the *PayloadLength* to 2047.

5.5.6.4. CRC Based

The CRC check is enabled by setting bit *CrcOn* in *RegPacketConfig1*. It is used for checking the integrity of the message.

- On Tx side a two byte CRC checksum is calculated on the payload part of the packet and appended to the end of the message
- On Rx side the checksum is calculated on the received payload and compared with the two checksum bytes received. The result of the comparison is stored in bit *CrcOk.*

By default, if the CRC check fails then the FIFO is automatically cleared and no interrupt is generated. This filtering function can be disabled via *CrcAutoClearOff* bit and in this case, even if CRC fails, the FIFO is not cleared and only *PayloadReady* interrupt goes high. Please note that in both cases, the two CRC checksum bytes are stripped off by the packet handler and only the payload is made available in the FIFO.

Two CRC implementations are selected with bit *CrcWhiteningType*.

Table 31 CRC Description

Crc Type	*CrcWhiteningType*	Polynomial	Seed Value	Complemented
CCITT	0 (default)	$X^{16} + X^{12} + X^5 + 1$	0x1D0F	Yes
IBM	1	$X^{16} + X^{15} + X^2 + 1$	0xFFFF	No

A C code implementation of each CRC type is proposed in Application Section 7.

5.5.7. DC-Free Data Mechanisms

The payload to be transmitted may contain long sequences of 1's and 0's, which introduces a DC bias in the transmitted signal. The radio signal thus produced has a non uniform power distribution over the occupied channel bandwidth. It also introduces data dependencies in the normal operation of the demodulator. Thus it is useful if the transmitted data is random and DC free.

For such purposes, two techniques are made available in the packet handler: Manchester encoding and data whitening.

Note Only one of the two methods can be enabled at a time.

5.5.7.1. Manchester Encoding

Manchester encoding/decoding is enabled if *DcFree = 01* and can only be used in Packet mode.

The NRZ data is converted to Manchester code by coding '1' as "10" and '0' as "01".

In this case, the maximum chip rate is the maximum bit rate given in the specifications section and the actual bit rate is half the chip rate.

Manchester encoding and decoding is only applied to the payload and CRC checksum while preamble and Sync word are kept NRZ. However, the chip rate from preamble to CRC is the same and defined by *BitRate* in *RegBitRate* (Chip Rate = Bit Rate NRZ = 2 x Bit Rate Manchester).

Manchester encoding/decoding is thus made transparent for the user, who still provides/retrieves NRZ data to/from the FIFO.

			1/BR ...Sync								1/BR Payload...								
RF chips @ BR	**...**	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**...**
User/NRZ bits Manchester OFF	...	1	1	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	...
User/NRZ bits Manchester ON	...	1	1	1	0	1	0	0	1		0		0		1		1		...

t

Figure 39. Manchester Encoding/Decoding

5.5.7.2. Data Whitening

Another technique called whitening or scrambling is widely used for randomizing the user data before radio transmission. The data is whitened using a random sequence on the Tx side and de-whitened on the Rx side using the same sequence. Comparing to Manchester technique it has the advantage of keeping NRZ data rate i.e. actual bit rate is not halved.

The whitening/de-whitening process is enabled if *DcFree = 10*. A 9-bit LFSR is used to generate a random sequence. The payload and 2-byte CRC checksum is then XORed with this random sequence as shown below. The data is de-whitened on the receiver side by XORing with the same random sequence.

Payload whitening/de-whitening is thus made transparent for the user, who still provides/retrieves NRZ data to/from the FIFO.

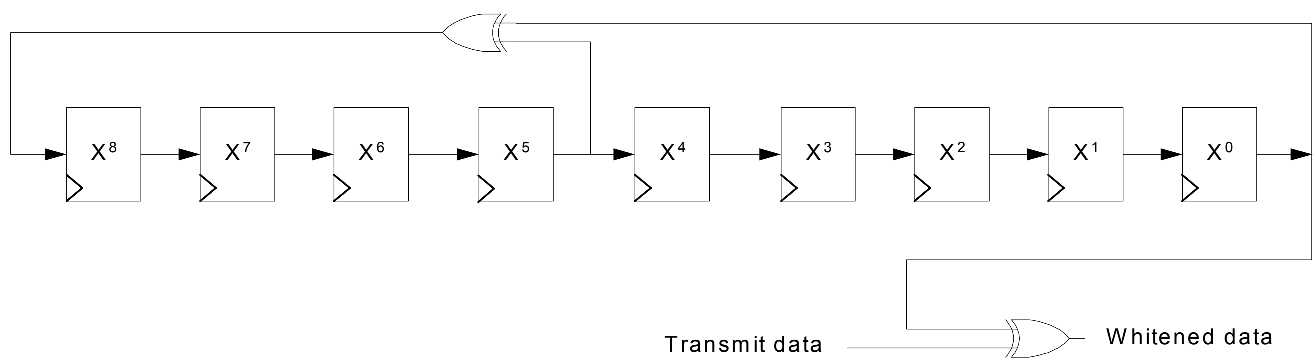


Figure 40. Data Whitening Polynomial

5.5.8. Beacon Tx Mode

In some short range wireless network topologies a repetitive message, also known as beacon, is transmitted periodically by a transmitter. The Beacon Tx mode allows for the re-transmission of the same packet without having to fill the FIFO multiple times with the same data.

When *BeaconOn* in *RegPacketConfig2* is set to 1, the FIFO can be filled only once in Sleep or Stdby mode with the required payload. After a first transmission, *FifoEmpty* will go high as usual, but the FIFO content will be restored when the chip exits Transmit mode. *FifoEmpty*, *FifoFull* and *FifoLevel* flags are also restored.

This feature is only available in Fixed packet format, with the Payload Length smaller than the FIFO size. The control of the chip modes (Tx-Sleep-Tx....) can either be undertaken by the microcontroller, or be automated in the Top Sequencer. See example in section 5.5.8.

The Beacon Tx mode is exited by setting *BeaconOn* to 0, and clearing the FIFO by setting *FifoOverrun* to 1.

5.6. io-homecontrol® Compatibility Mode

The SX1235 features a io-homecontrol® compatibility mode. Please contact your local Semtech representative for details on its implementation.

6. Description of the Registers

6.1. Register Table Summary

Table 32 Registers Summary

Address	Register Name	Reset (built-in)	Default (recommended)	Description
0x00	RegFifo	0x00		FIFO read/write access
0x01	RegOpMode	0x01		Operating modes of the transceiver
0x02	RegBitrateMsb	0x1A		Bit Rate setting, Most Significant Bits
0x03	RegBitrateLsb	0x0B		Bit Rate setting, Least Significant Bits
0x04	RegFdevMsb	0x00		Frequency Deviation setting, Most Significant Bits
0x05	RegFdevLsb	0x52		Frequency Deviation setting, Least Significant Bits
0x06	RegFrfMsb	0xE4		RF Carrier Frequency, Most Significant Bits
0x07	RegFrfMid	0xC0		RF Carrier Frequency, Intermediate Bits
0x08	RegFrfLsb	0x00		RF Carrier Frequency, Least Significant Bits
0x09	RegPaConfig	0x0F		PA selection and Output Power control
0x0A	RegPaRamp	0x19		Control of the PA ramp time in FSK, low phase noise PLL
0x0B	RegOcp	0x2B		Over Current Protection control
0x0C	RegLna	0x20		LNA settings
0x0D	RegRxConfig	0x08	0x0E	Control of the AFC, AGC, Collision detector
0x0E	RegRssiConfig	0x02		RSSI-related settings
0x0F	RegRssiCollision	0x0A		RSSI setting of the Collision detector
0x10	RegRssiThresh	0xFF		RSSI Threshold control
0x11	RegRssiValue	-		RSSI value in dBm
0x12	RegRxBw	0x15		Channel Filter BW Control
0x13	RegAfcBw	0x0B		Channel Filter BW control during the AFC
0x14	RegOokPeak	0x28		OOK demodulator selection and control in peak mode
0x15	RegOokFix	0x0C		Fixed threshold control of the OOK demodulator
0x16	RegOokAvg	0x12		Average threshold control of the OOK demodulator
0x17	Reserved17	0x47		-
0x18	Reserved18	0x32		-
0x19	Reserved19	0x3E		-

Address	Register Name	Reset (built-in)	Default (recommended)	Description
0x1A	RegAfcFei	0x00		AFC and FEI control
0x1B	RegAfcMsb	0x00		MSB of the frequency correction of the AFC
0x1C	RegAfcLsb	0x00		LSB of the frequency correction of the AFC
0x1D	RegFeiMsb	0x00		MSB of the calculated frequency error
0x1E	RegFeiLsb	0x00		LSB of the calculated frequency error
0x1F	RegPreambleDetect	0x40	0xAA	Settings of the Preamble Detector
0x20	RegRxTimeout1	0x00		Timeout duration between Rx request and RSSI detection
0x21	RegRxTimeout2	0x00		Timeout duration between RSSI detection and *PayloadReady*
0x22	RegRxTimeout3	0x00		Timeout duration between RSSI and *SyncAddress*
0x23	RegRxDelay	0x00		Delay between Rx cycles
0x24	RegOsc	0x05	0x07	RC Oscillators Settings, CLKOUT frequency
0x25	RegPreambleMsb	0x00		Preamble length, MSB
0x26	RegPreambleLsb	0x03		Preamble length, LSB
0x27	RegSyncConfig	0x93		Sync Word Recognition control
0x28-0x2F	RegSyncValue1-8	0x55	0x01	Sync Word bytes, 1 through 8
0x30	RegPacketConfig1	0x90		Packet mode settings
0x31	RegPacketConfig2	0x40		Packet mode settings
0x32	RegPayloadLength	0x40		Payload length setting
0x33	RegNodeAdrs	0x00		Node address
0x34	RegBroadcastAdrs	0x00		Broadcast address
0x35	RegFifoThresh	0x0F	0x8F	Fifo threshold, Tx start condition
0x36	RegSeqConfig1	0x00		Top level Sequencer settings
0x37	RegSeqConfig2	0x00		Top level Sequencer settings
0x38	RegTimerResol	0x00		Timer 1 and 2 resolution control
0x39	RegTimer1Coef	0xF5		Timer 1 setting
0x3A	RegTimer2Coef	0x20		Timer 2 setting
0x3B	RegImageCal	0x82	0x02	Image calibration engine control
0x3C	RegTemp	-		Temperature Sensor value
0x3D	RegLowBat	0x02		Low Battery Indicator Settings

Address	Register Name	Reset (built-in)	Default (recommended)	Description
0x3E	RegIrqFlags1	0x80		Status register: PLL Lock state, Timeout, RSSI > Threshold...
0x3F	RegIrqFlags2	0x40		Status register: FIFO handling flags, Low Battery detection...
0x40	RegDioMapping1	0x00		Mapping of pins DIO0 to DIO3
0x41	RegDioMapping2	0x00		Mapping of pins DIO4 and DIO5, ClkOut frequency
0x42	RegVersion	0x21		Semtech ID relating the silicon revision
0x43	RegAgcRef	0x13		Adjustment of the AGC thresholds
0x44	RegAgcThresh1	0x0E		
0x45	RegAgcThresh2	0x5B		
0x46	RegAgcThresh3	0xDB		
0x4B	RegPllHop	0x2E		Control the fast frequency hopping mode
0x58	RegTcxo	0x09		TCXO or XTAL input setting
0x5A	RegPaDac	0x84		Higher power settings of the PA
0x5C	RegPll	0xD0		Control of the PLL bandwidth
0x5E	RegPllLowPn	0xD0		Control of the Low Phase Noise PLL bandwidth
0x5F	RegPllGopt	0x32	0x37	Integrator loop gain control (category 1 use only)
0x6C	RegFormerTemp	-		Stored temperature during the former IQ Calibration
0x70	RegBitRateFrac	0x00		Fractional part in the Bit Rate division ratio
0x42 +	RegTest	-		Internal test registers. Do not overwrite

Note - *Reset values are automatically refreshed in the chip at Power On Reset*

- *Default values are the Semtech recommended register values, optimizing the device operation*
- *Registers for which the Default value differs from the Reset value are denoted by a * in the tables of section 6.2*

6.2. Register Map

Convention: r: read, w: write, t:trigger, c: clear

Table 33 Register Map

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegFifo (0x00)	7-0	Fifo	rw	0x00	FIFO data input/output
Resisters for Common settings					
RegOpMode (0x01)	7	unused	r	0x00	unused
	6-5	ModulationType	rw	0x00	Modulation scheme: 00 → FSK 01 → OOK 10 -11 → reserved
	4-3	ModulationShaping	rw	0x00	Data shaping: In FSK: 00 → no shaping 01 → gaussian filter BT = 1.0 10 → gaussian filter BT = 0.5 11 → gaussian filter BT = 0.3 In OOK: 00 → no shaping 01 → filtering with f_{cutoff} = bit_rate 10 → filtering with f_{cutoff} = 2*bit_rate (for bit_rate < 125 kb/s) 11 → reserved
	2-0	Mode	rw	0x01	Transceiver modes 000 → Sleep mode 001 → Stdby mode 010 → FS mode TX (FSTx) 011 → Transmitter mode (Tx) 100 → FS mode RX (FSRx) 101 → Receiver mode (Rx) 110 → reserved 111 → reserved
RegBitrateMsb (0x02)	7-0	BitRate(15:8)	rw	0x1a	MSB of Bit Rate (chip rate if Manchester encoding is enabled)
RegBitrateLsb (0x03)	7-0	BitRate(7:0)	rw	0x0b	LSB of bit rate (chip rate if Manchester encoding is enabled) $BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{BitrateFrac}{16}}$ Default value: 4.8 kb/s
RegFdevMsb (0x04)	7-6	unused	r	0x00	unused
	5-0	Fdev(13:8)	rw	0x00	MSB of the frequency deviation
RegFdevLsb (0x05)	7-0	Fdev(7:0)	rw	0x52	LSB of the frequency deviation $Fdev = Fstep \times Fdev(15,0)$ Default value: 5 kHz

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegFrfMsb (0x06)	7-0	Frf(23:16)	rw	0xe4	MSB of the RF carrier frequency
RegFrfMid (0x07)	7-0	Frf(15:8)	rw	0xc0	MSB of the RF carrier frequency
RegFrfLsb (0x08)	7-0	Frf(7:0)	rw	0x00	LSB of RF carrier frequency $Frf = Fstep \times Frf(23;0)$ Default value: 915.000 MHz The RF frequency is taken into account internally only when: - entering FSRX/FSTX modes - re-starting the receiver
Registers for the Transmitter					
RegPaConfig (0x09)	7	PaSelect	rw	0x00	Selects PA output pin 0 → RFO pin. Maximum power of +13 dBm 1 → PA_BOOST pin. Maximum power of +20 dBm
	6-4	unused	r	0x00	unused
	3-0	OutputPower	rw	0x0f	Output power setting, with 1dB steps Pout = 2 + *OutputPower* [dBm], on PA_BOOST pin Pout = -1 + *OutputPower* [dBm], on RFO pin
RegPaRamp (0x0A)	7-5	unused	r	-	unused
	4	LowPnTxPllOff	rw	0x01	Select a higher power, lower phase noise PLL only when the transmitter is used: 0 → Standard PLL used in Rx mode, Lower PN PLL in Tx 1 → Standard PLL used in both Tx and Rx modes
	3-0	PaRamp	rw	0x09	Rise/Fall time of ramp up/down in FSK 0000 → 3.4 ms 0001 → 2 ms 0010 → 1 ms 0011 → 500 us 0100 → 250 us 0101 → 125 us 0110 → 100 us 0111 → 62 us 1000 → 50 us 1001 → 40 us (d) 1010 → 31 us 1011 → 25 us 1100 → 20 us 1101 → 15 us 1110 → 12 us 1111 → 10 us

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegOcp (0x0B)	7-6	unused	r	0x00	unused
	5	OcpOn	rw	0x01	Enables overload current protection (OCP) for the PA: 0 → OCP disabled 1 → OCP enabled
	4-0	OcpTrim	rw	0x0b	Trimming of OCP current: I_{max} = 45+5*OcpTrim [mA] if OcpTrim <= 15 (120 mA) / I_{max} = -30+10*OcpTrim [mA] if 15 < OcpTrim <= 27 (130 to 240 mA) I_{max} = 240mA for higher settings Default I_{max} = 100mA
Registers for the Receiver					
RegLna (0x0C)	7-5	LnaGain	rw	0x01	LNA gain setting: 000 → reserved 001 → G1 = highest gain 010 → G2 = highest gain – 6 dB 011 → G3 = highest gain – 12 dB 100 → G4 = highest gain – 24 dB 101 → G5 = highest gain – 36 dB 110 → G6 = highest gain – 48 dB 111 → reserved Note: Reading this address always returns the current LNA gain (which may be different from what had been previously selected if AGC is enabled.
	4-2	-	r	0x00	unused
	1-0	LnaBoost	rw	0x00	Improves the system Noise Figure at the expense of Rx current consumption: 00 → Default setting, meeting the specification 11 → Improved sensitivity
RegRxConfig (0x0d)	7	RestartRxOnCollision	rw	0x00	Turns on the mechanism restarting the receiver automatically if it gets saturated or a packet collision is detected 0 → No automatic Restart 1 → Automatic restart On
	6	RestartRxWithoutPllLock	wt	0x00	Triggers a manual Restart of the Receiver chain when set to 1. Use this bit when there is no frequency change, RestartRxWithPllLock otherwise.
	5	RestartRxWithPllLock	wt	0x00	Triggers a manual Restart of the Receiver chain when set to 1. Use this bit when there is a frequency change, requiring some time for the PLL to re-lock.
	4	AfcAutoOn	rw	0x00	0 → No AFC performed at receiver startup 1 → AFC is performed at each receiver startup
	3	AgcAutoOn	rw	0x01	0 → LNA gain forced by the LnaGain Setting 1 → LNA gain is controlled by the AGC
	2-0	RxTrigger	rw	0x06 *	Selects the event triggering AGC and/or AFC at receiver startup. See Table 24 for a description.

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegRssiConfig (0x0e)	7-3	RssiOffset	rw	0x00	Signed RSSI offset, to compensate for the possible losses/ gains in the front-end (LNA, SAW filter...) 1dB / LSB, 2's complement format
	2-0	RssiSmoothing	rw	0x02	Defines the number of samples taken to average the RSSI result: 000 → 2 samples used 001 → 4 samples used 010 → 8 samples used 011 → 16 samples used 100 → 32 samples used 101 → 64 samples used 110 → 128 samples used 111 → 256 samples used
RegRssiCollision (0x0f)	7-0	RssiCollisionThreshold	rw	0x0a	Sets the threshold used to consider that an interferer is detected, witnessing a packet collision. 1dB/LSB (only RSSI increase) Default: 10dB
RegRssiThresh (0x10)	7-0	RssiThreshold	rw	0xff	RSSI trigger level for the Rssi interrupt: - RssiThreshold / 2 [dBm]
RegRssiValue (0x11)	7-0	RssiValue	r	-	Absolute value of the RSSI in dBm, 0.5dB steps. RSSI = - RssiValue/2 [dBm]
RegRxBw (0x12)	7	unused	r	-	unused
	6-5	reserved	rw	0x00	reserved
	4-3	RxBwMant	rw	0x02	Channel filter bandwidth control: 00 → RxBwMant = 16 10 → RxBwMant = 24 01 → RxBwMant = 20 11 → reserved
	2-0	RxBwExp	rw	0x05	Channel filter bandwidth control: FSK Mode: $RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp + 2}}$
RegAfcBw (0x13)	7-5	reserved	rw	0x00	reserved
	4-3	RxBwMantAfc	rw	0x01	RxBwMant parameter used during the AFC
	2-0	RxBwExpAfc	rw	0x03	RxBwExp parameter used during the AFC

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegOokPeak (0x14)	7-6	reserved	rw	0x00	reserved
	5	BitSyncOn	rw	0x01	Enables the Bit Synchronizer. 0 → Bit Sync disabled (not possible in Packet mode) 1 → Bit Sync enabled
	4-3	OokThreshType	rw	0x01	Selects the type of threshold in the OOK data slicer: 00 → fixed threshold 10 → average mode 01 → peak mode (default) 11 → reserved
	2-0	OokPeakTheshStep	rw	0x00	Size of each decrement of the RSSI threshold in the OOK demodulator: 000 → 0.5 dB 001 → 1.0 dB 010 → 1.5 dB 011 → 2.0 dB 100 → 3.0 dB 101 → 4.0 dB 110 → 5.0 dB 111 → 6.0 dB
RegOokFix (0x15)	7-0	OokFixedThreshold	rw	0x0C	Fixed threshold for the Data Slicer in OOK mode Floor threshold for the Data Slicer in OOK when Peak mode is used
RegOokAvg (0x16)	7-5	OokPeakThreshDec	rw	0x00	Period of decrement of the RSSI threshold in the OOK demodulator: 000 → once per chip 001 → once every 2 chips 010 → once every 4 chips 011 → once every 8 chips 100 → twice in each chip 101 → 4 times in each chip 110 → 8 times in each chip 111 → 16 times in each chip
	4	reserved	rw	0x01	reserved
	3-2	OokAverageOffset	rw	0x00	Static offset added to the threshold in average mode in order to reduce glitching activity (OOK only): 00 → 0.0 dB 10 → 4.0 dB 01 → 2.0 dB 11 → 6.0 dB
	1-0	OokAverageThreshFilt	rw	0x02	Filter coefficients in average mode of the OOK demodulator: 00 → f_C ≈ chip rate / 32.π 01 → f_C ≈ chip rate / 8.π 10 → f_C ≈ chip rate / 4.π 11 → f_C ≈ chip rate / 2.π
RegRes17 to RegRes19	7-0	reserved	rw	0x47 0x32 0x3E	reserved. Keep the Reset values.
RegAfcFei (0x1a)	7-5	unused	r	-	unused
	4	AgcStart	wt	0x00	Triggers an AGC sequence when set to 1.
	3	reserved	rw	0x00	reserved
	2	unused	-	-	unused
	1	AfcClear	wc	0x00	Clear AFC register set in Rx mode. Always reads 0.
	0	AfcAutoClearOn	rw	0x00	Only valid if AfcAutoOn is set 0 → AFC register is not cleared at the beginning of the automatic AFC phase 1 → AFC register is cleared at the beginning of the automatic AFC phase

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegAfcMsb (0x1b)	7-0	AfcValue(15:8)	rw	0x00	MSB of the AfcValue, 2's complement format. Can be used to overwrite the current AFC value
RegAfcLsb (0x1c)	7-0	AfcValue(7:0)	rw	0x00	LSB of the AfcValue, 2's complement format. Can be used to overwrite the current AFC value
RegFeiMsb (0x1d)	7-0	FeiValue(15:8)	rw	-	MSB of the measured frequency offset, 2's complement. Must be read before RegFeiLsb.
RegFeiLsb (0x1e)	7-0	FeiValue(7:0)	rw	-	LSB of the measured frequency offset, 2's complement *Frequency error* = FeiValue x Fstep
RegPreambleDetect (0x1f)	7	PreambleDetectorOn	rw	0x01 *	Enables Preamble detector when set to 1. The AGC settings supersede this bit during the startup / AGC phase. 0 → Turned off 1 → Turned on
	6-5	PreambleDetectorSize	rw	0x01 *	Number of Preamble bytes to detect to trigger an interrupt 00 → 1 byte 01 → 2 bytes 10 → 3 bytes 11 → Reserved
	4-0	PreambleDetectorTol	rw	0x0A *	Number or chip errors tolerated over PreambleDetectorSize. 4 chips per bit.
RegRxTimeout1 (0x20)	7-0	TimeoutRxRssi	rw	0x00	*Timeout* interrupt is generated *TimeoutRxRssi**16*T_{bit} after switching to Rx mode if *Rssi* interrupt doesn't occur (i.e. *RssiValue > RssiThreshold)* 0x00: *TimeoutRxRssi* is disabled
RegRxTimeout2 (0x21)	7-0	TimeoutRxPreamble	rw	0x00	*Timeout* interrupt is generated *TimeoutRxPreamble**16*T_{bit} after switching to Rx mode if *Preamble* interrupt doesn't occur 0x00: *TimeoutRxPreamble* is disabled
RegRxTimeout3 (0x22)	7-0	TimeoutSignalSync	rw	0x00	*Timeout* interrupt is generated *TimeoutSignalSync**16*T_{bit} after the Rx mode is programmed, if *SyncAddress* doesn't occur 0x00: *TimeoutSignalSync* is disabled
RegRxDelay (0x23)	7-0	InterPacketRxDelay	rw	0x00	Additional delay befopre an automatic receiver restart is launched: Delay = InterPacketRxDelay*4*Tbit
		RC Oscillator registers			
RegOsc (0x24)	7-4	unused	r	-	unused
	3	RcCalStart	wt	0x00	Triggers the calibration of the RC oscillator when set. Always reads 0. RC calibration must be triggered in Standby mode.
	2-0	ClkOut	rw	0x07 *	Selects CLKOUT frequency: 000 → FXOSC 001 → FXOSC / 2 010 → FXOSC / 4 011 → FXOSC / 8 100 → FXOSC / 16 101 → FXOSC / 32 110 → RC (automatically enabled) 111 → OFF

Name (Address)	Bits	Variable Name	Mode	Default value	Description
Packet Handling registers					
RegPreambleMsb (0x25)	7-0	PreambleSize(15:8)	rw	0x00	Size of the preamble to be sent (from *TxStartCondition* fulfilled). (MSB byte)
RegPreambleLsb (0x26)	7-0	PreambleSize(7:0)	rw	0x03	Size of the preamble to be sent (from *TxStartCondition* fulfilled). (LSB byte)
RegSyncConfig (0x27)	7-6	AutoRestartRxMode	rw	0x02	Controls the automatic restart of the receiver after the reception of a valid packet (PayloadReady or CrcOk): 00 → Off 01 → On, without waiting for the PLL to re-lock 10 → On, wait for the PLL to lock (frequency changed) 11 → reserved
	5	PreamblePolarity	rw	0x00	Sets the polarity of the Preamble 0 → 0xAA (default) 1 → 0x55
	4	SyncOn	rw	0x01	Enables the Sync word generation and detection: 0 → Off 1 → On
	3	FifoFillCondition	rw	0x00	FIFO filling condition: 0 → if *SyncAddress* interrupt occurs 1 → as long as *FifoFillCondition* is set
	2-0	SyncSize	rw	0x03	Size of the Sync word: (*SyncSize* + 1) bytes, (*SyncSize*) bytes if *ioHomeOn*=1
RegSyncValue1 (0x28)	7-0	SyncValue(63:56)	rw	0x01 *	1st byte of Sync word. (MSB byte) Used if *SyncOn* is set.
RegSyncValue2 (0x29)	7-0	SyncValue(55:48)	rw	0x01 *	2nd byte of Sync word Used if *SyncOn* is set and *(SyncSize +1)* >= 2.
RegSyncValue3 (0x2a)	7-0	SyncValue(47:40)	rw	0x01 *	3rd byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 3.
RegSyncValue4 (0x2b)	7-0	SyncValue(39:32)	rw	0x01 *	4th byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 4.
RegSyncValue5 (0x2c)	7-0	SyncValue(31:24)	rw	0x01 *	5th byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 5.
RegSyncValue6 (0x2d)	7-0	SyncValue(23:16)	rw	0x01 *	6th byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 6.
RegSyncValue7 (0x2e)	7-0	SyncValue(15:8)	rw	0x01 *	7th byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 7.
RegSyncValue8 (0x2f)	7-0	SyncValue(7:0)	rw	0x01 *	8th byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* = 8.

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegPacketConfig1 (0x30)	7	PacketFormat	rw	0x01	Defines the packet format used: 0 → Fixed length 1 → Variable length
	6-5	DcFree	rw	0x00	Defines DC-free encoding/decoding performed: 00 → None (Off) 01 → Manchester 10 → Whitening 11 → reserved
	4	CrcOn	rw	0x01	Enables CRC calculation/check (Tx/Rx): 0 → Off 1 → On
	3	CrcAutoClearOff	rw	0x00	Defines the behavior of the packet handler when CRC check fails: 0 → Clear FIFO and restart new packet reception. No *PayloadReady* interrupt issued. 1 → Do not clear FIFO. *PayloadReady* interrupt issued.
	2-1	AddressFiltering	rw	0x00	Defines address based filtering in Rx: 00 → None (Off) 01 → Address field must match *NodeAddress* 10 → Address field must match *NodeAddress* or *BroadcastAddress* 11 → reserved
	0	CrcWhiteningType	rw	0x00	Selects the CRC and whitening algorithms: 0 → CCITT CRC implementation with standard whitening 1 → IBM CRC implementation with alternate whitening
RegPacketConfig2 (0x31)	7	unused	r	-	unused
	6	DataMode	rw	0x01	Data processing mode: 0 → Continuous mode 1 → Packet mode
	5	IoHomeOn	rw	0x00	Enables the io-homecontrol® compatibility mode 0 → Disabled 1 → Enabled
	4	IoHomePowerFrame	rw	0x00	reserved - Linked to io-homecontrol® compatibility mode
	3	BeaconOn	rw	0x00	Enables the Beacon mode in Fixed packet format
	2-0	PayloadLength(10:8)	rw	0x00	Packet Length Most significant bits
RegPayloadLength (0x32)	7-0	PayloadLength(7:0)	rw	0x40	If PacketFormat = 0 (fixed), payload length. If PacketFormat = 1 (variable), max length in Rx, not used in Tx.
RegNodeAdrs (0x33)	7-0	NodeAddress	rw	0x00	Node address used in address filtering.
RegBroadcastAdrs (0x34)	7-0	BroadcastAddress	rw	0x00	Broadcast address used in address filtering.

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegFifoThresh (0x35)	7	TxStartCondition	rw	0x01 *	Defines the condition to start packet transmission: 0 → *FifoLevel* (i.e. the number of bytes in the FIFO exceeds *FifoThreshold)* 1 → *FifoEmpty goes low*(i.e. at least one byte in the FIFO)
	6	unused	r	-	unused
	5-0	FifoThreshold	rw	0x0f	Used to trigger *FifoLevel* interrupt, when: number of bytes in FIFO >= FifoThreshold + 1
Sequencer registers					
RegSeqConfig1 (0x36)	7	SequencerStart	wt	0x00	Controls the top level Sequencer When set to ‘1’, executes the “Start” transition. The sequencer can only be enabled when the chip is in Sleep or Standby mode.
	6	SequencerStop	wt	0x00	Forces the Sequencer Off. Always reads ‘0’
	5	IdleMode	rw	0x00	Selects chip mode during the state: 0: Standby mode 1: Sleep mode
	4-3	FromStart	rw	0x00	Controls the Sequencer transition when *SequencerStart* is set to 1 in Sleep or Standby mode: 00: to LowPowerSelection 01: to Receive state 10: to Transmit state 11: to Transmit state on a *FifoLevel* interrupt
	2	LowPowerSelection	rw	0x00	Selects the Sequencer LowPower state after a *to LowPowerSelection* transition: 0: SequencerOff state with chip on Initial mode 1: Idle state with chip on *Standby* or *Sleep* mode depending on *IdleMode* *Note: Initial mode is the chip LowPower mode at Sequencer Start.*
	1	FromIdle	rw	0x00	Controls the Sequencer transition from the Idle state on a T1 interrupt: 0: to Transmit state 1: to Receive state
	0	FromTransmit	rw	0x00	Controls the Sequencer transition from the Transmit state: 0: to LowPowerSelection on a *PacketSent* interrupt 1: to Receive state on a *PacketSent* interrupt

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegSeqConfig2 (0x37)	7-5	FromReceive	rw	0x00	Controls the Sequencer transition from the Receive state 000 and 111: unused 001: to PacketReceived state on a *PayloadReady* interrupt 010: to LowPowerSelection on a *PayloadReady* interrupt 011: to PacketReceived state on a *CrcOk* interrupt (1) 100: to SequencerOff state on a *Rssi* interrupt 101: to SequencerOff state on a *SyncAddress* interrupt 110: to SequencerOff state on a *PreambleDetect* interrupt Irrespective of this setting, transition to LowPowerSelection on a T2 interrupt (1) If the CRC is wrong (corrupted packet, with CRC on but *CrcAutoClearOn*=0), the *PayloadReady* interrupt will drive the sequencer to RxTimeout state.
	4-3	FromRxTimeout	rw	0x00	Controls the state-machine transition from the Receive state on a *RxTimeout* interrupt (and on *PayloadReady* if FromReceive = 011): 00: to Receive State, via ReceiveRestart 01: to Transmit state 10: to LowPowerSelection 11: to SequencerOff state *Note: RxTimeout interrupt is a TimeoutRxRssi, TimeoutRxPreamble or TimeoutSignalSync interrupt*
	2-0	FromPacketReceived	rw	0x00	Controls the state-machine transition from the PacketReceived state: 000: to SequencerOff state 001: to Transmit state on a *FifoEmpty* interrupt 010: to LowPowerSelection 011: to Receive via FS mode, if frequency was changed 100: to Receive state (no frequency change)
RegTimerResol (0x38)	7-4	unused	r	-	unused
	3-2	Timer1Resolution	rw	0x00	Resolution of Timer 1 00: Timer1 disabled 01: 64 us 10: 4.1 ms 11: 262 ms
	1-0	Timer2Resolution	rw	0x00	Resolution of Timer 2 00: Timer2 disabled 01: 64 us 10: 4.1 ms 11: 262 ms
RegTimer1Coef (0x39)	7-0	Timer1Coefficient	rw	0xf5	Multiplying coefficient for Timer 1
RegTimer2Coef (0x3a)	7-0	Timer2Coefficient	rw	0x20	Multiplying coefficient for Timer 2

Name (Address)	Bits	Variable Name	Mode	Default value	Description
Services registers					
RegImageCal (0x3b)	7	AutoImageCalOn	rw	0x00 *	Controls the Image calibration mechanism 0 → Calibration of the receiver depending on the temperature is disabled 1 → Calibration of the receiver depending on the temperature enabled.
	6	ImageCalStart	wt	-	Triggers the IQ and RSSI calibration when set in Standby mode.
	5	ImageCalRunning	r	0x00	Set to 1 while the Image and RSSI calibration are running. Toggles back to 0 when the process is completed
	4	unused	r	-	unused
	3	TempChange	r	0x00	IRQ flag witnessing a temperature change exceeding TempThreshold since the last Image and RSSI calibration: 0 → Temperature change lower than TempThreshold 1 → Temperature change greater than TempThreshold
	2-1	TempThreshold	rw	0x01	Temperature change threshold to trigger a new I/Q calibration 00 → 5 °C 01 → 10 °C 10 → 15 °C 11 → 20 °C
	0	TempMonitorOff	rw	0x00	Controls the temperature monitor operation: 0 → Temperature monitoring done in all modes except Sleep and Standby 1 → Temperature monitoring stopped.
RegTemp (0x3c)	7-0	TempValue	r	-	Measured temperature -1°C per Lsb Needs calibration for absolute accuracy
RegLowBat (0x3d)	7-4	unused	r	-	unused
	3	LowBatOn	rw	0x00	Low Battery detector enable signal 0 → LowBat detector disabled 1 → LowBat detector enabled
	2-0	LowBatTrim	rw	0x02	Trimming of the LowBat threshold: 000 → 1.695 V 001 → 1.764 V 010 → 1.835 V (d) 011 → 1.905 V 100 → 1.976 V 101 → 2.045 V 110 → 2.116 V 111 → 2.185 V
Status registers					

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegIrqFlags1 (0x3e)	7	ModeReady	r	-	Set when the operation mode requested in *Mode*, is ready - Sleep: Entering Sleep mode - Standby: XO is running - FS: PLL is locked - Rx: RSSI sampling starts - Tx: PA ramp-up completed Cleared when changing the operating mode.
	6	RxReady	r	-	Set in Rx mode, after RSSI, AGC and AFC. Cleared when leaving Rx.
	5	TxReady	r	-	Set in Tx mode, after PA ramp-up. Cleared when leaving Tx.
	4	PllLock	r	-	Set (in FS, Rx or Tx) when the PLL is locked. Cleared when it is not.
	3	Rssi	rwc	-	Set in Rx when the *RssiValue* exceeds *RssiThreshold.* Cleared when leaving Rx or setting this bit to 1.
	2	Timeout	r	-	Set when a timeout occurs Cleared when leaving Rx or FIFO is emptied.
	1	PreambleDetect	rwc	-	Set when the Preamble Detector has found valid Preamble. bit clear when set to 1
	0	SyncAddressMatch	rwc	-	Set when Sync and Address (if enabled) are detected. Cleared when leaving Rx or FIFO is emptied. This bit is read only in Packet mode, rwc in Continuous mode
RegIrqFlags2 (0x3f)	7	FifoFull	r	-	Set when FIFO is full (i.e. contains 66 bytes), else cleared.
	6	FifoEmpty	r	-	Set when FIFO is empty, and cleared when there is at least 1 byte in the FIFO.
	5	FifoLevel	r	-	Set when the number of bytes in the FIFO strictly exceeds *FifoThreshold*, else cleared.
	4	FifoOverrun	rwc	-	Set when FIFO overrun occurs. (except in Sleep mode) Flag(s) and FIFO are cleared when this bit is set. The FIFO then becomes immediately available for the next transmission / reception.
	3	PacketSent	r	-	Set in Tx when the complete packet has been sent. Cleared when exiting Tx
	2	PayloadReady	r	-	Set in Rx when the payload is ready (i.e. last byte received and CRC, if enabled and *CrcAutoClearOff* is cleared, is Ok). Cleared when FIFO is empty.
	1	CrcOk	r	-	Set in Rx when the CRC of the payload is Ok. Cleared when FIFO is empty.
	0	LowBat	rwc	-	Set when the battery voltage drops below the Low Battery threshold. Cleared only when set to 1 by the user.
IO control registers					

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegDioMapping1 (0x40)	7-6	Dio0Mapping	rw	0x00	Mapping of pins DIO0 to DIO5 See Table 29 for mapping in Continuous mode See Table 30 for mapping in Packet mode
	5-4	Dio1Mapping	rw	0x00	
	3-2	Dio2Mapping	rw	0x00	
	1-0	Dio3Mapping	rw	0x00	
RegDioMapping2 (0x41)	7-6	Dio4Mapping	rw	0x00	
	5-4	Dio5Mapping	rw	0x00	
	3-1	reserved	rw	0x00	reserved. Retain default value
	0	MapPreambleDetect	rw	0x00	Allows the mapping of either *Rssi* Or *PreambleDetect* to the DIO pins, as summarized on Table 29 and Table 30 0 → *Rssi* interrupt 1 → *PreambleDetect* interrupt
Version register					
RegVersion (0x42)	7-0	Version	r	0x21	Version code of the chip. Bits 7-4 give the full revision number; bits 3-0 give the metal mask revision number.
Additional registers					
RegAgcRef (0x43)	7-6	unused	r	-	unused
	5-0	AgcReferenceLevel	rw	0x13	Sets the floor reference for all AGC thresholds: AGC Reference[dBm]= -174dBm+10*log(2*$RxBw$)+SNR+*AgcReferenceLevel* SNR = 8dB, fixed value
RegAgcThresh1 (0x44)	7-5	unused	r	-	unused
	4-0	AgcStep1	rw	0x0e	Defines the 1st AGC Threshold
RegAgcThresh2 (0x45)	7-4	AgcStep2	rw	0x05	Defines the 2nd AGC Threshold:
	3-0	AgcStep3	rw	0x0b	Defines the 3rd AGC Threshold:
RegAgcThresh3 (0x46)	7-4	AgcStep4	rw	0x0d	Defines the 4th AGC Threshold:
	3-0	AgcStep5	rw	0x0b	Defines the 5th AGC Threshold:
RegPllHop (0x4b)	7	FastHopOn	rw	0x00	Bypasses the main state machine for a quick frequency hop. Writing RegFrfLsb will trigger the frequency change. 0 → Frf is validated when FSTx or FSRx is requested 1 → Frf is validated triggered when RegFrfLsb is written
	6-0	reserved	rw	0x2e	reserved
RegTcxo (0x58)	7-5	reserved	rw	0x00	reserved. Retain default value
	4	TcxoInputOn	rw	0x00	Controls the crystal oscillator 0 → Crystal Oscillator with external Crystal 1 → External clipped sine TCXO AC-connected to XTA pin
	3-0	reserved	rw	0x09	Reserved. Retain default value.
RegPaDac (0x5a)	7-3	reserved	rw	0x10	reserved. Retain default value
	2-0	PaDac	rw	0x04	Enables the +20dBm option on PA_BOOST pin 0x04 → Default value 0x07 → +20dBm on PA_BOOST when OutputPower=1111

Name (Address)	Bits	Variable Name	Mode	Default value	Description
RegPll (0x5c)	7-6	PllBandwidth	rw	0x03	Controls the PLL bandwidth: 00 → 75 kHz 10 → 225 kHz 01 → 150 kHz 11 → 300 kHz
	5-0	reserved	rw	0x10	reserved. Retain default value
RegPllLowPn (0x5e)	7-6	PllBandwidth	rw	0x03	Controls the Low Phase Noise PLL bandwidth: 00 → 75 kHz 10 → 225 kHz 01 → 150 kHz 11 → 300 kHz
	5-0	reserved	rw	0x10	reserved. Retain default value
RegPllGopt	7-0	LoopGain	rw	0x32	Controls the PLL loop gain and other settings 0x37 → Category 1 phase noise optimization 0x32 → All other applications
RegFormerTemp (0x6c)	7-0	FormerTemp	rw	-	Temperature saved during the latest IQ (RSSI and Image) calibrated. Same format as *TempValue* in *RegTemp*.
RegBitrateFrac (0x70)	7-4	unused	r	0x00	unused
	3-0	BitRateFrac	rw	0x00	Fractional part of the bit rate divider (Only valid for FSK) If *BitRateFrac*> 0 then: $BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{BitrateFrac}{16}}$

7. Application Information

7.1. Crystal Resonator Specification

Table 34 shows the crystal resonator specification for the crystal reference oscillator circuit of the SX1235. This specification covers the full range of operation of the SX1235 and is employed in the reference design.

Table 34 Crystal Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FXOSC	XTAL Frequency		-	32	-	MHz
RS	XTAL Serial Resistance		-	30	140	ohms
C0	XTAL Shunt Capacitance		-	2.8	7	pF
CFOOT	External Foot Capacitance	On each pin XTA and XTB	8	15	22	pF
CLOAD	Crystal Load Capacitance		6	-	12	pF

Notes - the initial frequency tolerance, temperature stability and ageing performance should be chosen in accordance with the target operating temperature range and the receiver bandwidth selected.

- the loading capacitance should be applied externally, and adapted to the actual Cload specification of the XTAL.

7.2. Reset of the Chip

A power-on reset of the SX1235 is triggered at power up. Additionally, a manual reset can be issued by controlling pin 6.

7.2.1. POR

If the application requires the disconnection of VDD from the SX1235, despite of the extremely low Sleep Mode current, the user should wait for 10 ms from of the end of the POR cycle before commencing communications over the SPI bus. Pin 6 (Reset) should be left floating during the POR sequence.

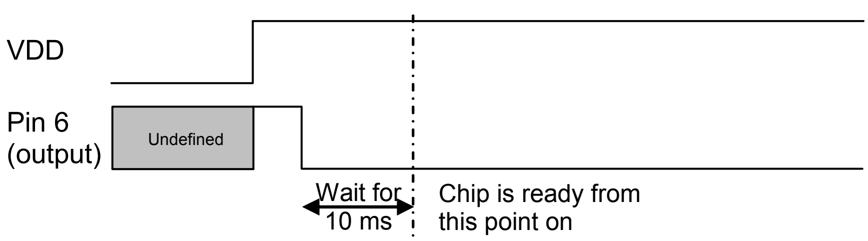


Figure 41. POR Timing Diagram

Please note that any CLKOUT activity can also be used to detect that the chip is ready.

7.2.2. Manual Reset

A manual reset of the SX1235 is possible even for applications in which VDD cannot be physically disconnected. Pin 6 should be pulled high for a hundred microseconds, and then released. The user should then wait for 5 ms before using the chip.

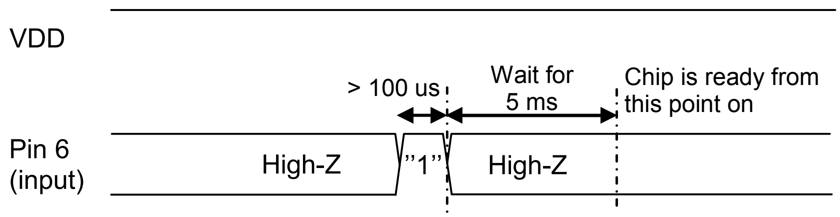


Figure 42. Manual Reset Timing Diagram

Note whilst pin 6 is driven high, an over current consumption of up to ten milliamps can be seen on VDD.

7.3. Reference Designs

Please contact your Semtech representative for evaluation tools, reference designs and design assistance. Note that all schematics shown in this section are full schematics, listing ALL required components, including decoupling capacitors.

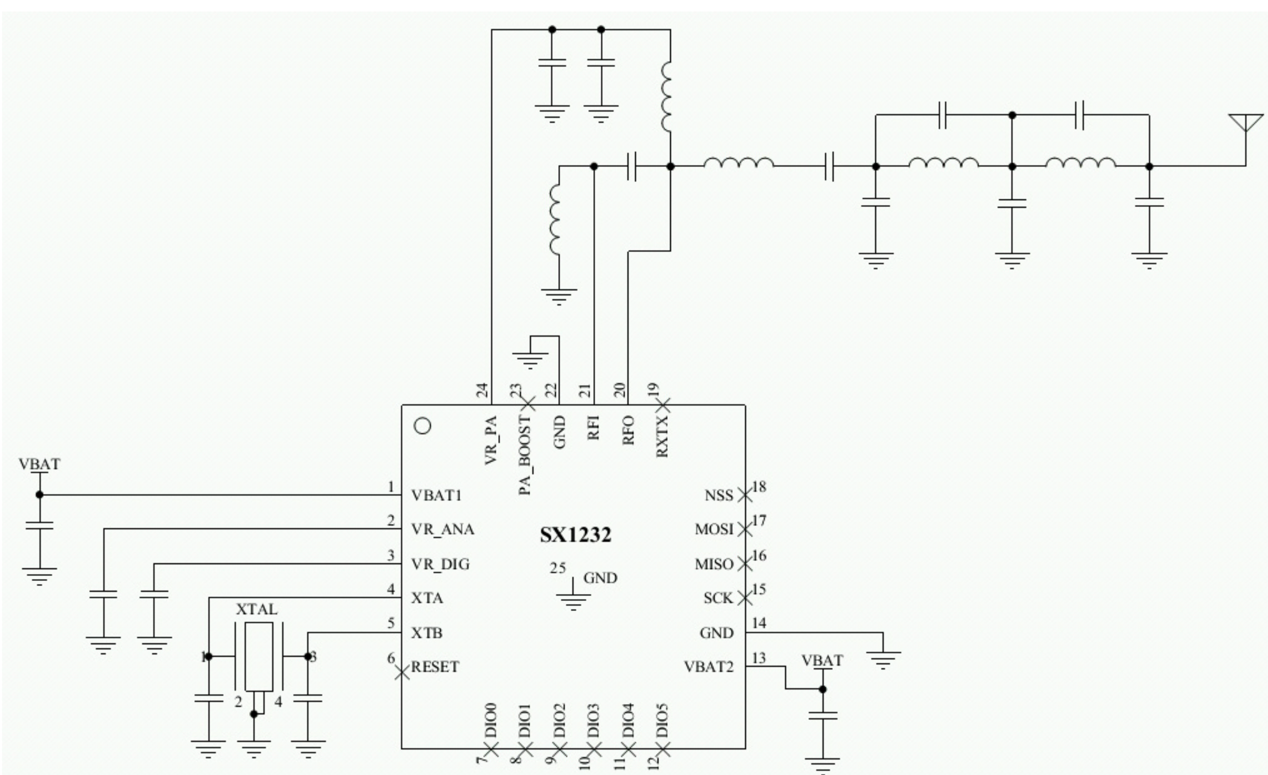


Figure 43. Reference Design - Single RF Input/Output, High Efficiency PA

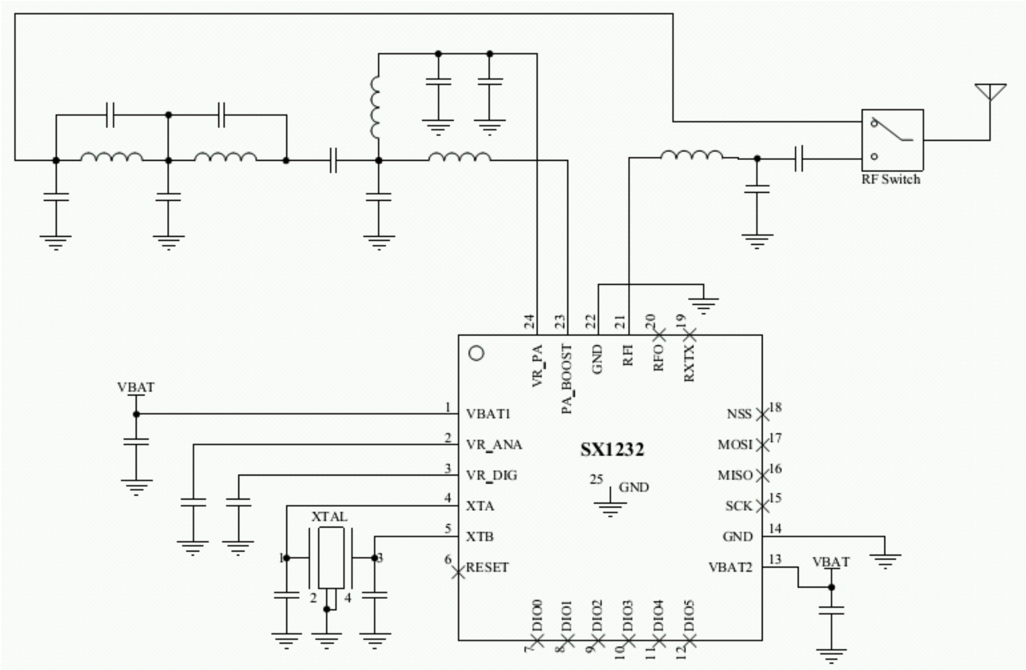


Figure 44. Reference Design - with Antenna Switch up to +20dBm

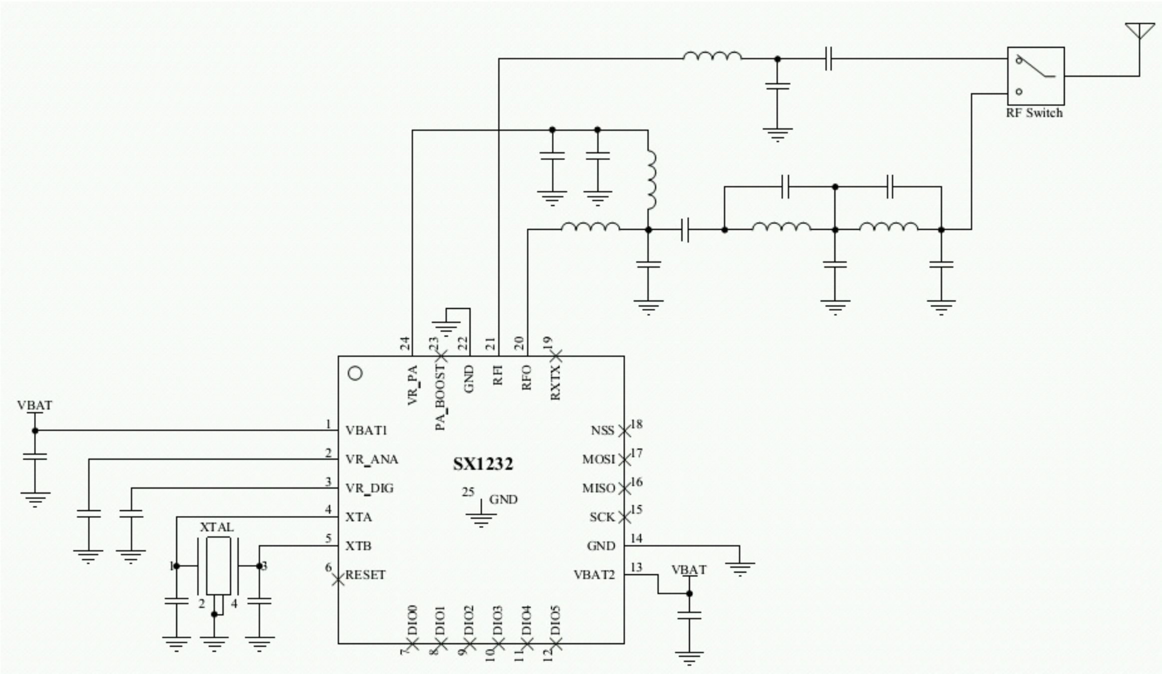


Figure 45. Reference Design - with Antenna Switch and High Efficiency PA

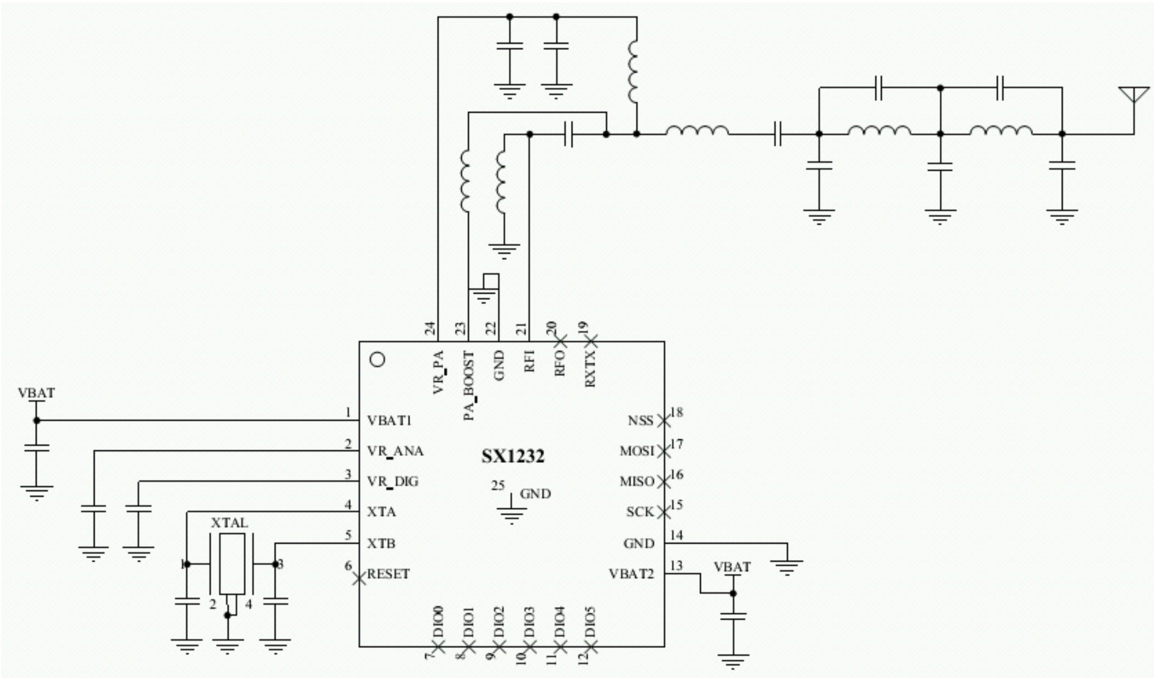


Figure 46. Reference Design - Single RF Input/Output, High Stability PA

Note The implementation of Figure 46 is limited to +14dBm Operation

For detailed Bills of Materials, please consult the Reference Design section on the SX1235 web page, or contact your local Semtech representative.

7.4. Top Sequencer: Listen Mode Examples

In this scenario, the circuit spends most of the time in Idle mode, during which only the RC oscillator is on. Periodically the receiver wakes up and looks for incoming signal. If a wanted signal is detected, the receiver is kept on and data are analyzed. Otherwise, if there was no wanted signal for a defined period of time, the receiver is switched off until the next receive period.

During Listen mode, the Radio stays most of the time in a Low Power mode, resulting in very low average power consumption. The general timing diagram of this scenario is given in Figure 47.

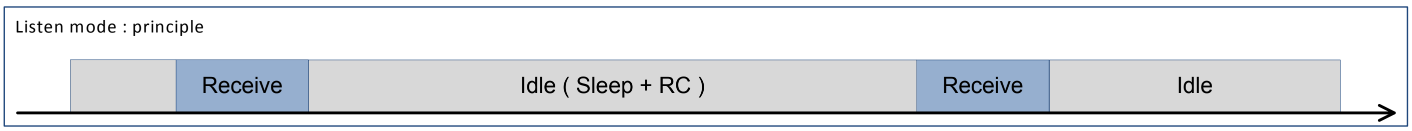


Figure 47. Listen Mode: Principle

An interrupt request is generated on a packet reception. The user can then take appropriate action.

Depending on the application and environment, there are several ways to implement Listen mode:

- Wake on a *PreambleDetect* interrupt
- Wake on *a SyncAddress* interrupt
- Wake on *a PayloadReady* interrupt

7.4.1. Wake on Preamble Interrupt

In one possible scenario, the sequencer polls for a Preamble detection. If a preamble signal is detected, the sequencer is switched off and the circuit stays in Receive mode until the user switches modes. Otherwise, the receiver is switched off until the next Rx period.

7.4.1.1. Timing Diagram

When no signal is received, the circuit wakes every Timer1 + Timer2 and switches to Receive mode for a time defined by Timer2, as shown on the following diagram. If no Preamble is detected, it then switches back to Idle mode, i.e. Sleep mode with RC oscillator on.

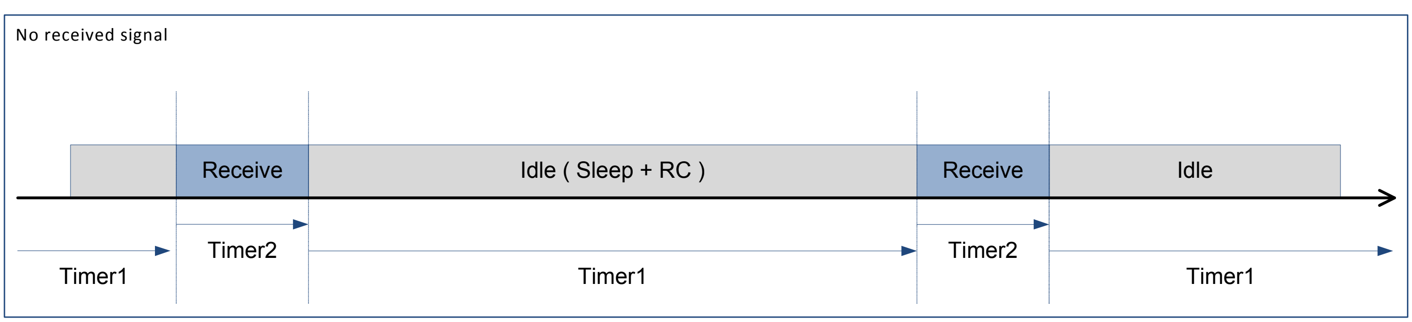


Figure 48. Listen Mode with No Preamble Received

If a Preamble signal is detected, the Sequencer is switched off. The *PreambleDetect* signal can be mapped to DIO4, in order to request the user's attention. The user can then take appropriate action.

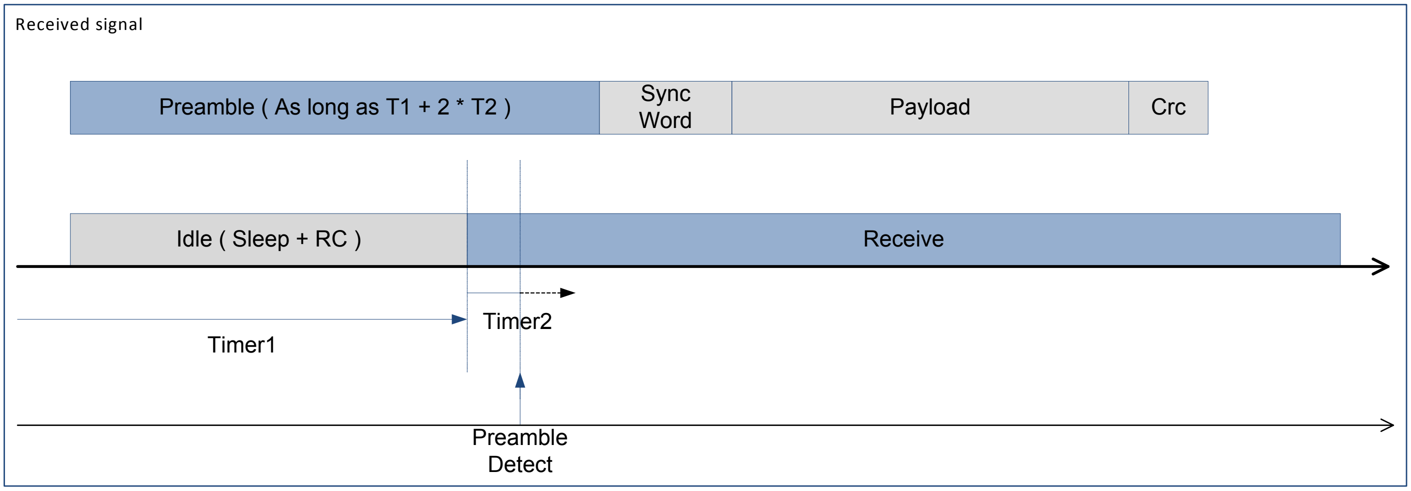


Figure 49. Listen Mode with Preamble Received

7.4.1.2. Sequencer Configuration

The following graph shows Listen mode - Wake on *PreambleDetect* state machine:

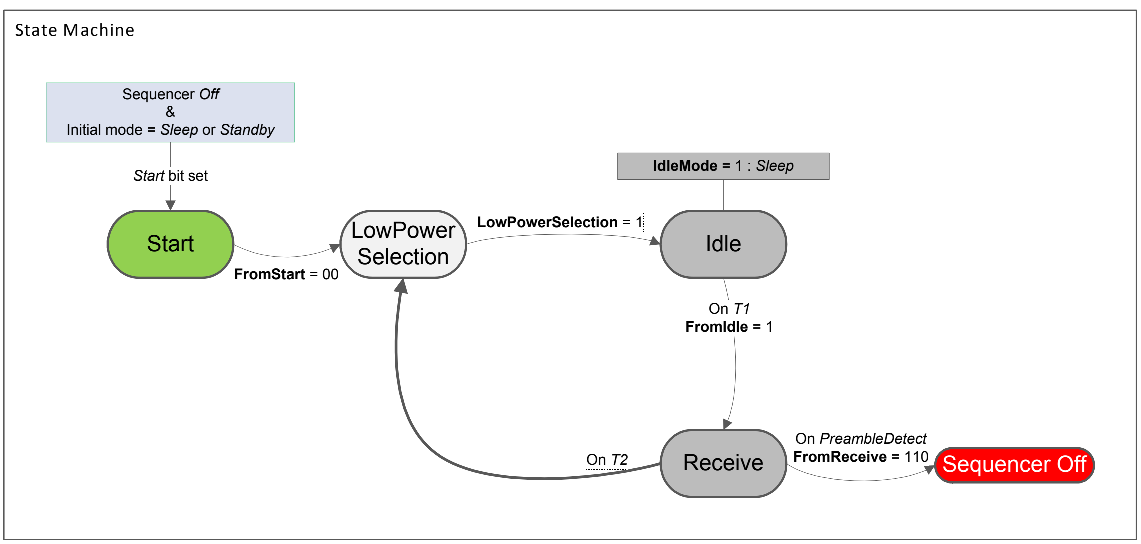


Figure 50. Wake On PreambleDetect State Machine

This example configuration is achieved as follows:

Table 35 Listen Mode with PreambleDetect Condition Settings

Variable	Effect
IdleMode	1 : **Sleep** mode
FromStart	00 : To **LowPowerSelection**
LowPowerSelection	1 : To **Idle** state
FromIdle	1 : To **Receive** state on *T1* interrupt
FromReceive	110 : To **Sequencer Off** on *PreambleDetect* interrupt

T_{Timer2} defines the maximum duration the chip stays in Receive mode as long as no Preamble is detected. In order to optimize power consumption, Timer2 must be set just long enough for Preamble detection.

$T_{Timer1} + T_{Timer2}$ defines the cycling period, i.e. time between two Preamble polling starts. In order to optimize average power consumption, Timer1 should be relatively long. However, increasing Timer1 also extends packet reception duration.

In order to insure packet detection and optimize the receiver's power consumption, the received packet Preamble should be as long as $T_{Timer1} + 2 \times T_{Timer2}$.

An example of DIO configuration for this mode is described in the following table:

Table 36 Listen Mode with PreambleDetect Condition Recommended DIO Mapping

DIO	Value	Description
0	01	CrcOk
1	00	FifoLevel
3	00	FifoEmpty
4	11	PreambleDetect – Note: *MapPreambleDetect* bit should be set.

7.4.2. Wake on SyncAddress Interrupt

In another possible scenario, the sequencer polls for a Preamble detection and then for a valid *SyncAddress* interrupt. If events occur, the sequencer is switched off and the circuit stays in Receive mode until the user switches modes. Otherwise, the receiver is switched off until the next Rx period.

7.4.2.1. Timing Diagram

Most of the sequencer running time is spent while no wanted signal is received. As shown by the timing diagram in Figure 51, the circuit wakes periodically for a short time, defined by RxTimeout. The circuit is in a Low Power mode for the rest of Timer1 + Timer2 (i.e. Timer1 + Timer2 - TrxTimeout)

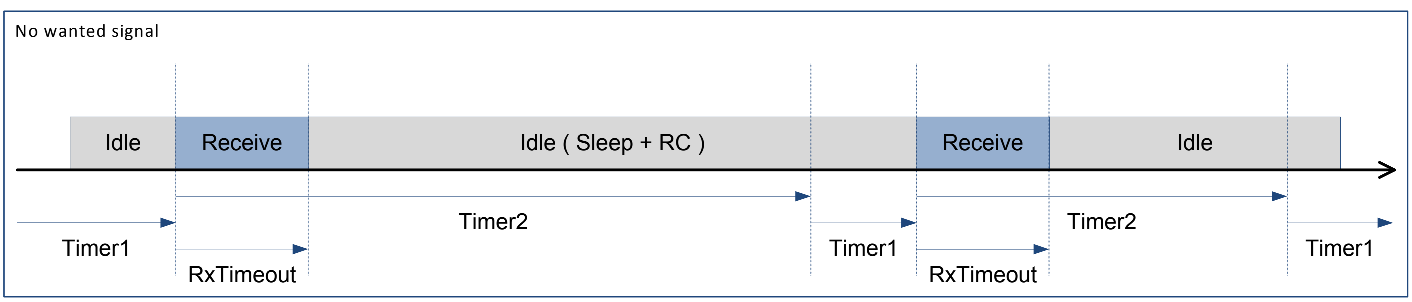


Figure 51. Listen Mode with no SyncAddress Detected

If a preamble is detected before *RxTimeout* timer ends, the circuit stays in Receive mode and waits for a valid *SyncAddress* detection. If none is detected by the end of Timer2, Receive mode is deactivated and the polling cycle resumes, without any user intervention.

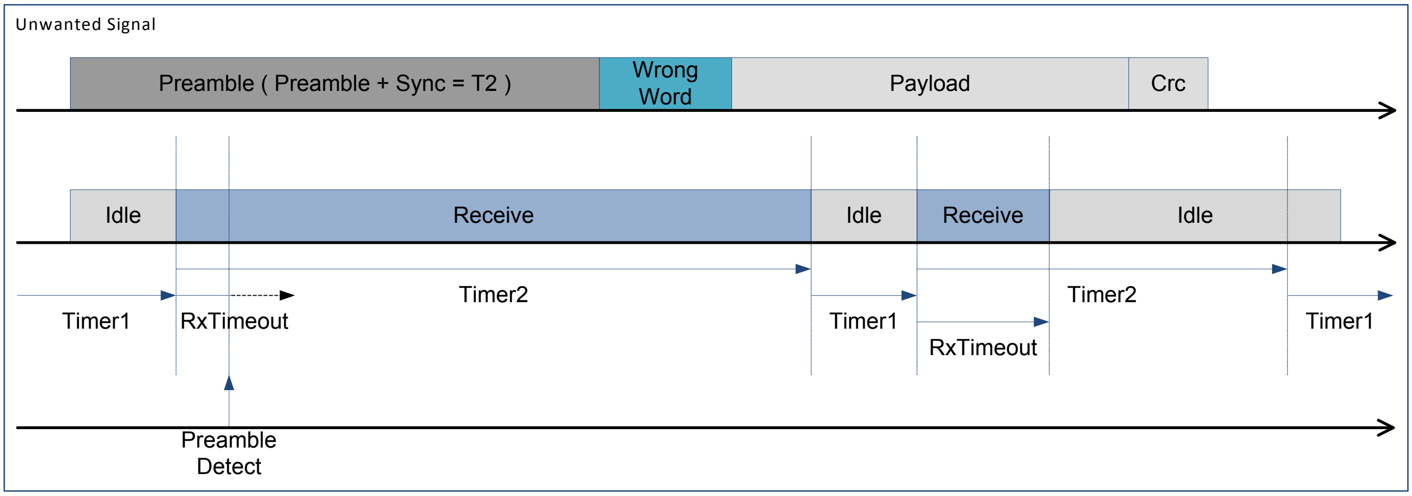


Figure 52. Listen Mode with Preamble Received and no SyncAddress

But if a valid Sync Word is detected, a *SyncAddress* interrupt is fired, the Sequencer is switched off and the circuit stays in Receive mode as long as the user doesn't switch modes.

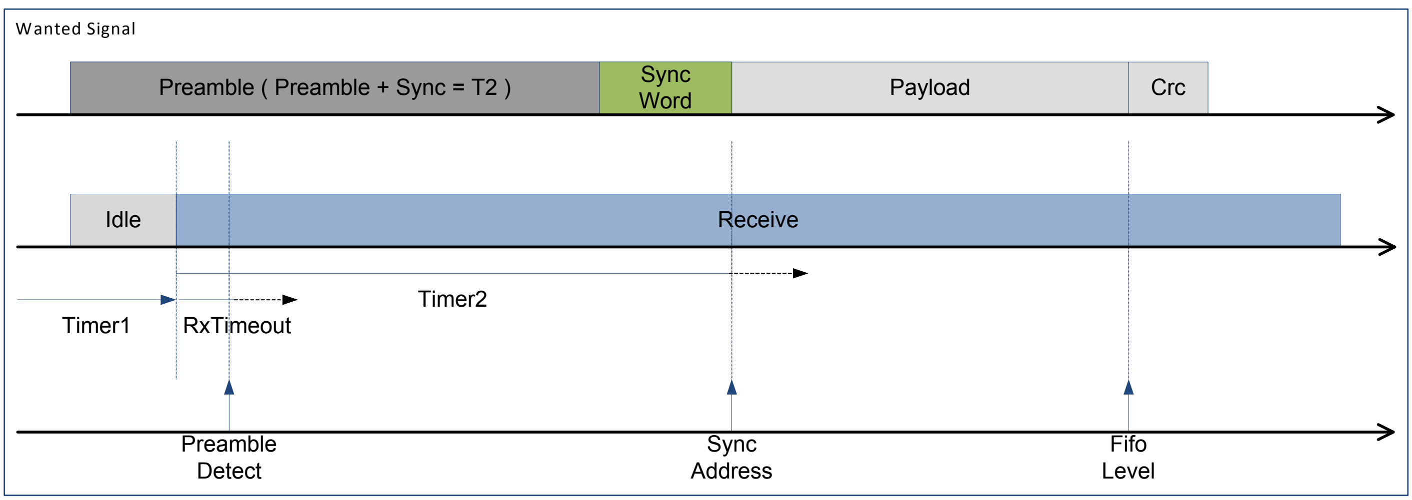


Figure 53. Listen Mode with Preamble Received & Valid SyncAddress

7.4.2.2. Sequencer Configuration

The following graph shows Listen mode - Wake on SyncAddress state machine:

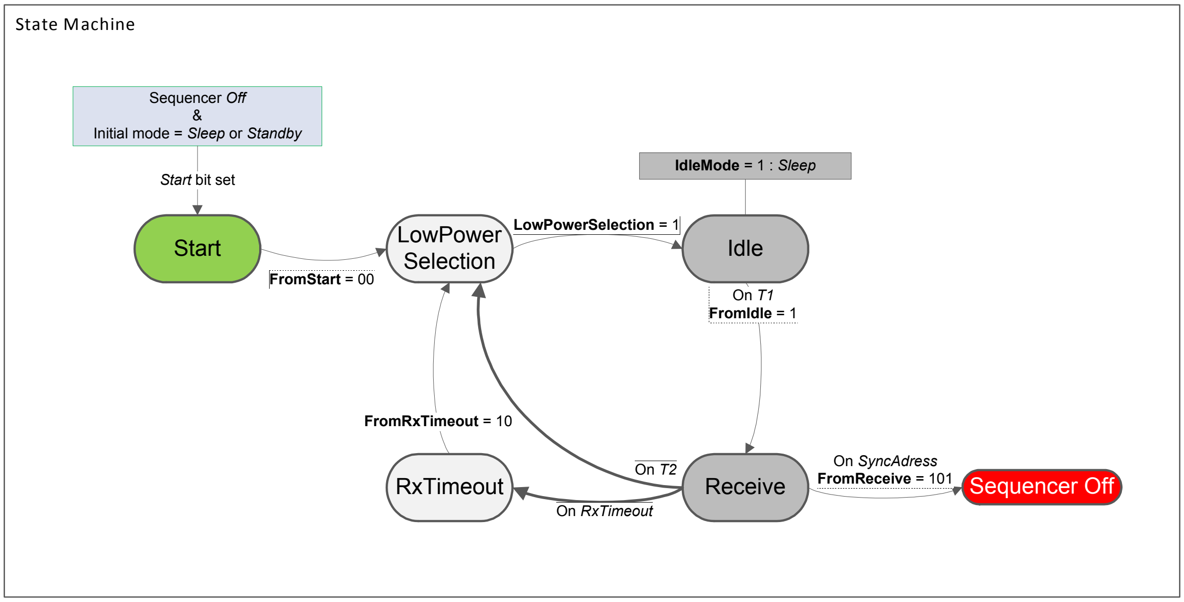


Figure 54. Wake On SyncAddress State Machine

This example configuration is achieved as follows:

Table 37 Listen Mode with SyncAddress Condition Settings

Variable	Effect
IdleMode	1 : **Sleep** mode
FromStart	00 : To **LowPowerSelection**
LowPowerSelection	1 : To **Idle** state
FromIdle	1 : To **Receive** state on *T1* interrupt
FromReceive	101 : To **Sequencer off** on *SyncAddress* interrupt
FromRxTimeout	10 : To **LowPowerSelection**

$T_{TimeoutRxPreamble}$ should be set to just long enough to catch a preamble (depends on *PreambleDetectSize* and *BitRate*).

T_{Timer1} should be set to 64 µs (shortest possible duration).

T_{Timer2} is set so that $T_{Timer1} + T_{Timer2}$ defines the time between two start of reception.

In order to insure packet detection and optimize the receiver power consumption, the received packet Preamble should be defined so that $T_{Preamble} = T_{Timer2} - T_{SyncAddress}$, with $T_{SyncAddress} = (SyncSize + 1)*8/BitRate$.

An example of DIO configuration for this mode is described in the following table:

Table 38 Listen Mode with PreambleDetect Condition Recommended DIO Mapping

DIO	Value	Description
0	01	CrcOk
1	00	FifoLevel
2	11	SyncAddress
3	00	FifoEmpty
4	11	PreambleDetect – Note: *MapPreambleDetect* bit should be set.

7.5. Top Sequencer: Beacon Mode

In this mode, a repetitive message is transmitted periodically. If the Payload being sent is always identical, and *PayloadLength* is smaller than the FIFO size, the use of the *BeaconOn* bit in *RegPacketConfig2* together with the Sequencer permit to achieve periodic beacon without any user intervention.

7.5.1. Timing diagram

In this mode, the Radio is switched to Transmit mode every T_{Timer1} + T_{Timer2} and back to Idle mode after *PacketSent*, as shown in the diagram below. The Sequencer insures minimal time is spent in Transmit mode, and therefore power consumption is optimized.

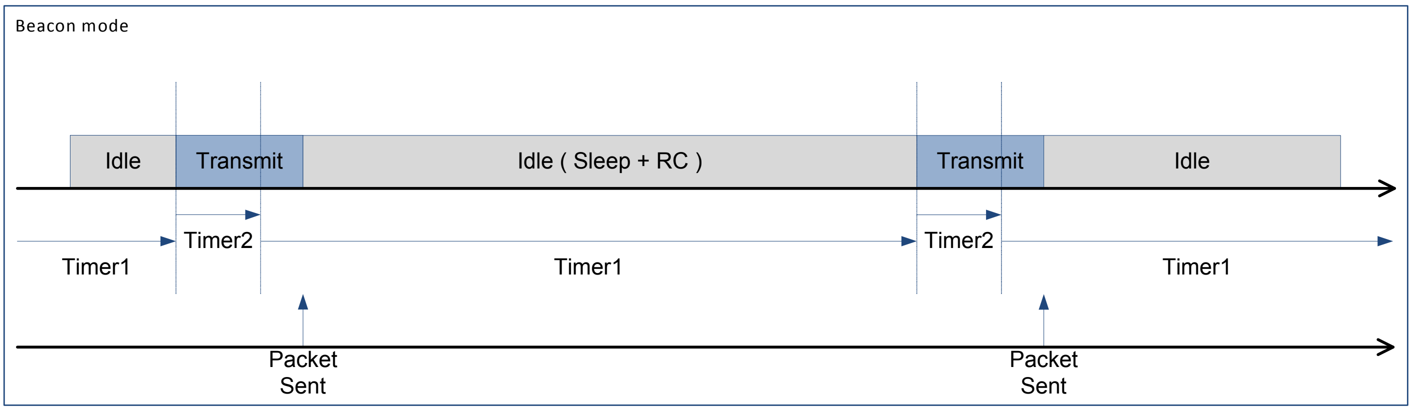


Figure 55. Beacon Mode Timing Diagram

7.5.2. Sequencer Configuration

The Beacon mode state machine is presented in the following graph. It is noticeable that the sequencer enters an infinite loop and can only be stopped by setting *SequencerStop* bit in *RegSeqConfig1*.

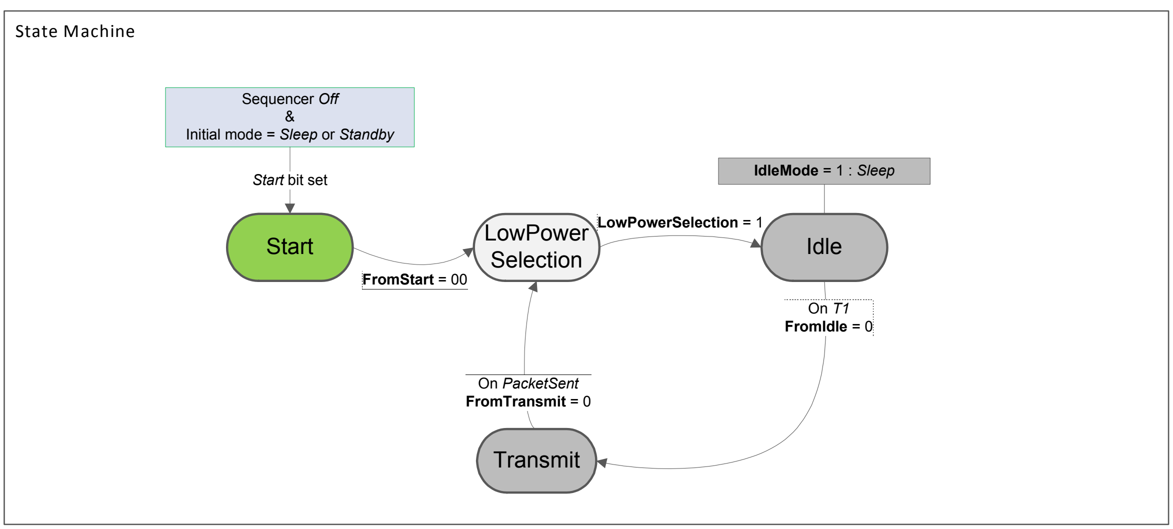


Figure 56. Beacon Mode State Machine

This example is achieved by programming the Sequencer as follows:

Table 39 Beacon Mode Settings

Variable	Effect
IdleMode	1 : **Sleep** mode
FromStart	00 : To **LowPowerSelection**
LowPowerSelection	1 : To **Idle** state
FromIdle	0 : To **Transmit** state on *T1* interrupt
FromTransmit	0 : To **LowPowerSelection** on *PacketSent* interrupt

$T_{Timer1} + T_{Timer2}$ define the time between the start of two transmissions.

7.6. Example CRC Calculation

The following routine(s) may be implemented to mimic the CRC calculation of the SX1235:

```
// CRC types
#define CRC_TYPE_CCITT                0
#define CRC_TYPE_IBM                  1

// Polynomial = X^16 + X^12 + X^5 + 1
#define POLYNOMIAL_CCITT              0x1021
// Polynomial = X^16 + X^15 + X^2 + 1
#define POLYNOMIAL_IBM                0x8005

// Seeds
#define CRC_IBM_SEED                  0xFFFF
#define CRC_CCITT_SEED                0x1D0F

/*
 * CRC algorithm implementation
 *
 * \param[IN] crc Previous CRC value
 * \param[IN] data New data to be added to the CRC
 * \param[IN] polynomial CRC polynomial selection [CRC_TYPE_CCITT, CRC_TYPE_IBM]
 *
 * \retval crc New computed CRC
 */
U16 ComputeCrc( U16 crc, U8 data, U16 polynomial )
{
    U8 i;
    for( i = 0; i < 8; i++ )
    {
        if( ( ( ( crc & 0x8000 ) >> 8 ) ^ ( data & 0x80 ) ) != 0 )
        {
            crc <<= 1;              // shift left once
            crc ^= polynomial;      // XOR with polynomial
        }
        else
        {
            crc <<= 1;              // shift left once
        }
        data <<= 1;                 // Next data bit
    }
    return crc;
}

/*
 * CRC algorithm implementation
 *
 * \param[IN] buffer Array containing the data
 * \param[IN] bufferLength Buffer length
 * \param[IN] crcType Selects the CRC polynomial[CRC_TYPE_CCITT, CRC_TYPE_IBM]
 *
 * \retval crc Buffer computed CRC
 */
U16 RadioPacketComputeCrc( U8 *buffer, U8 bufferLength, U8 crcType )
{
    U8 i;
    U16 crc;
    U16 polynomial;

    polynomial = ( crcType == CRC_TYPE_IBM ) ? POLYNOMIAL_IBM : POLYNOMIAL_CCITT;
    crc = ( crcType == CRC_TYPE_IBM ) ? CRC_IBM_SEED : CRC_CCITT_SEED;

    for( i = 0; i < bufferLength; i++ )
    {
        crc = ComputeCrc( crc, buffer[i], polynomial );
    }

    if( crcType == CRC_TYPE_IBM )
    {
        return crc;
    }
    else
    {
        return ( U16 )( ~crc );
    }
}
```

Figure 57. Example CRC Code

7.7. Example Temperature Reading

The following routine(s) may be implemented to read the temperature and calibrate the sensor:

Temperature.c

```c

/*!
 * Reads the raw temperature
 * \retval temperature New raw temperature reading in 2's complement format
 */
S8 RadioGetRawTemp( void )
{
    S8 temp = 0;
    U8 regValue = 0;
    
    regValue = RadioRead( 0x3C );

    // 2's complements conversion
    temp = regValue & 0x7F;
    if( ( regValue & 0x80 ) == 0x80 )
    {
        temp *= -1;
    }
    return temp;
}

/*!
 * Computes the temperature compensation factor
 * \param [IN] actualTemp Actual temperature measured by an external device
 * \retval compensationFactor Computed compensation factor
 */
S8 RadioCalibrateTemp( S8 actualTemp )
{
    return actualTemp - RadioGetRawTemp( );
}

/*!
 * Gets the actual compensated temperature
 * \param [IN] compensationFactor Return value of the calibration function
 * \retval New compensated temperature value
 */
S8 RadioGetTemp( S8 compensationFactor )
{
    return RadioGetRawTemp( ) + compensationFactor;
}

/*!
 * Usage example
 */
void main( void )
{
    S8 temp;
    S8 actualTemp = 0;
    S8 compensationFactor = 0;
    
    // Ask user for the temperature during calibration
    actualTemp = AskUserTemperature( );
    compensationFactor = RadioCalibrateTemp( actualTemp );

    while( True )
    {
        temp = RadioGetTemp( compensationFactor );
    }
}
```

Figure 58.   Example Temperature Reading

7.8. ETSI Category 1 Quick Start

To correctly configure the SX1235 for ETSI category 1 operation, it is necessary to enable some specific functionality within the receiver. The following description highlights the settings required to enable and realize the category 1 performances of the SX1235.

7.8.1. PLL Settings

The SX1235 features a single PLL for use in reception. Correctly configured, the PLL becomes the component of the receiver system that has the greatest contribution to the adjacent channel performances of the receiver. By minimizing the phase noise, the rejection afforded in the adjacent channels is increased.

The default PLL bandwidth setting provides the lowest phase noise in the 12.5 kHz and 25 kHz frequency offsets. However, by modification of the loop gain setting it is possible to further improve the phase noise in this frequency range. The RegPllGopt (address 0x5F) should be written to value 0x37. With this setting the resultant phase noise is shown in the figure below.

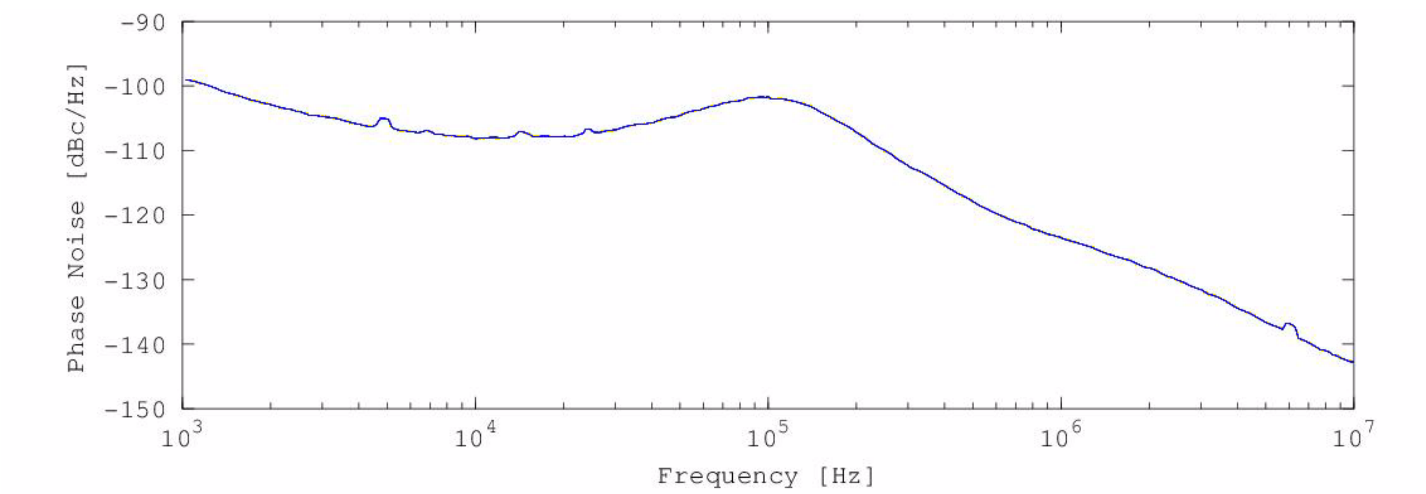


Figure 59. SX1235 Optimised Phase Noise at 12.5 kHz and 25 kHz

7.8.2. Channel Filter Settings

The dominance of the phase noise on the adjacent channel rejection performance of the SX1235 assumes that the receiver channel filtration is correctly configured. Two receiver channel filter bandwidths are accessible during the reception of data: The first, the AFC bandwidth is the bandwidth used during reception of preamble and alignment of the receiver. The second, the communication (Rx) bandwidth is that used for the ensuing communication phase. These must be suitably wide that the total crystal error and modulation bandwidth of the signal can be accommodated by the receiver during the AFC phase. The narrower communication bandwidth must then be at least as wide as the received signal's modulation bandwidth. To ensure the highest link quality the -20 dB bandwidth of the receiver filter is declared.

The figure below illustrates the difference between these three filter settings and the conventions used in the use of either double or single side band used.

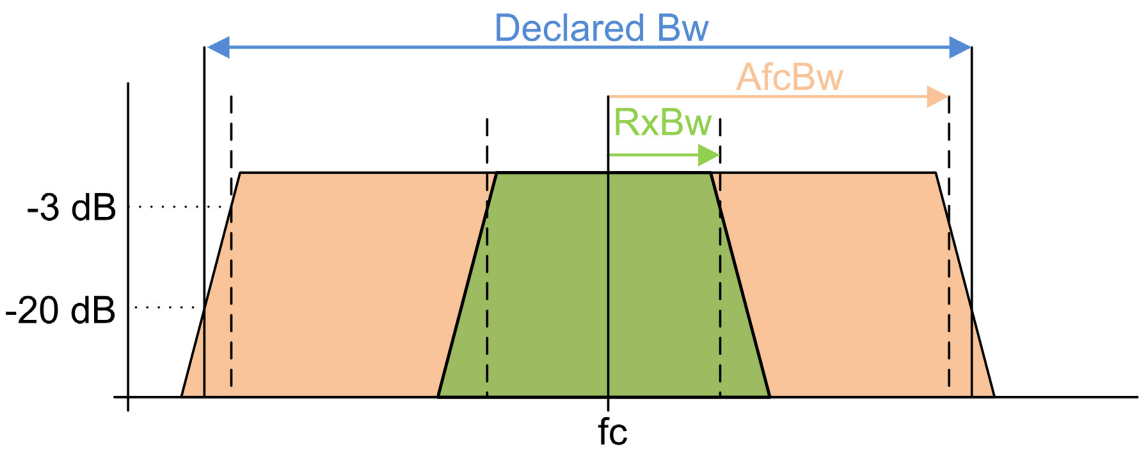


Figure 60. SX1235 Filter Definitions and Conventions

To aid with the selection of the appropriate bandwidth settings the programmable filter steps relevant to narrow band category 1 applications are shown below

Table 40 Category 1 Narrowband Filter Settings for SX1235

RxBwMant (binary/value)	RxBwExp (decimal)	Bw (kHz) Afc or Rx	Declared Bw$_{-20\,dB}$ (kHz)	Intermediate Frequency (kHz)
10b / 24	7	2.6	6.2	166.66
01b / 20	7	3.1	7.4	200
00b / 16	7	3.9	9.4	250
10b / 24	6	5.2	12.5	166.66
01b / 20	6	6.3	15.1	200
00b / 16	6	7.8	18.7	250
10b / 24	5	10.4	24.9	166.66
01b / 20	5	12.5	-	200
00b / 16	5	15.6	-	250
10b / 24	4	20.8	-	166.66
01b / 20	4	25.0	-	200

7.8.3. Image Frequency

Also shown in the preceding table is the intermediate frequency (IF) used depending upon which receiver bandwidth is used. Because the SX1235 features a low IF based upon a local oscillator lower in frequency than the RF centre frequency the resulting image frequency, at which there is a spurious response, is as shown below:

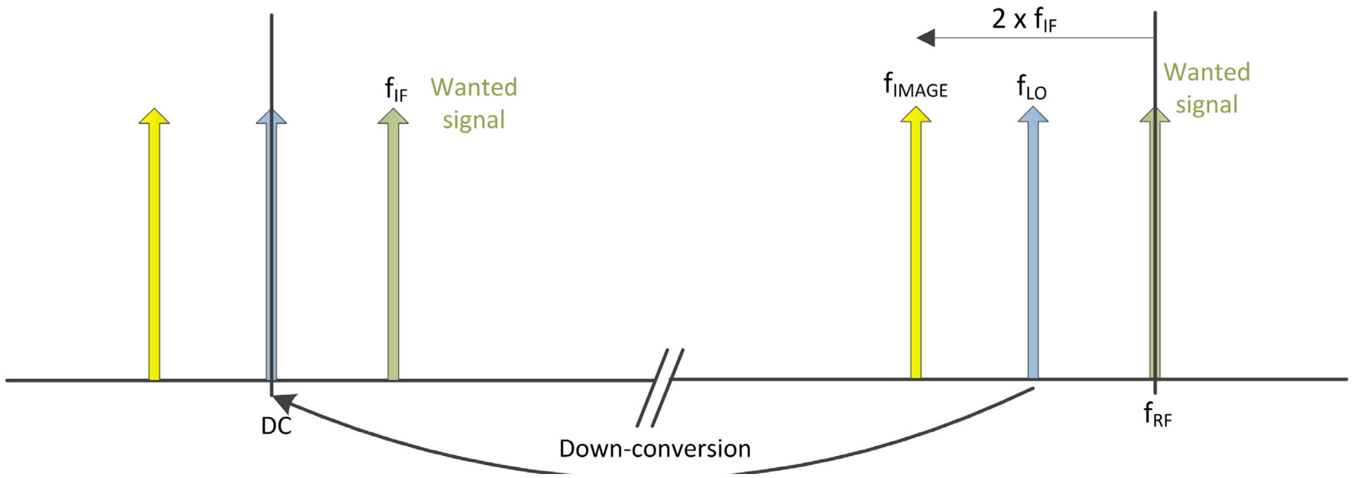


Figure 61. SX1235 Spurious Image Response Frequency

This spurious image response frequency is hence located at twice the intermediate frequency below the wanted signal frequency.

Table 41 SX1235 Image and Intermediate Frequency Values.

RxBwMant (binary)	IF (kHz)	Image Frequency
00b	250	f_{RF} - 500 kHz
01b	200	f_{RF} - 400 kHz
10b	166.6	f_{RF} - 333 kHz

The SX1235 features an image rejection filter which, when calibrated, is capable of providing over 45 dB of image rejection. To ensure the highest quality calibration, and so the best image rejection, calibration procedure outlined below should be performed following reset of the circuit or after a significant temperature change (see *TempChange* flag).

Step 1. Register address 0x0E should be written to 0x07 to increase the RSSI smoothing value to 256.
Step 2. Trigger the image calibration by writing to register address 0x3B with the contents 0x22.
Step 3. Wait 8 ms
Step 4. Register address 0x0E should be written to 0x02 to return the RSSI smoothing value to default.

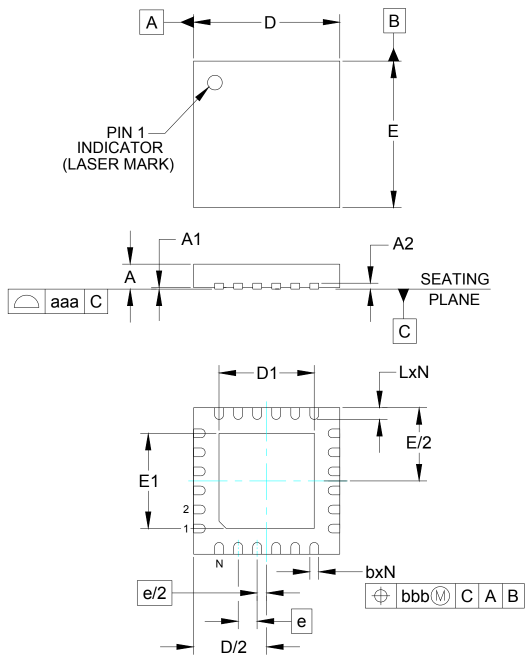
7.8.4. TCXO Settings

The use of narrow band channels in the Category 1 regulations means that a TCXO is typically required. Use of the TCXO is enabled by setting bit *TcxoInputOn* of register *RegTcxo*. For connection of the TCXO see Figure 9.

8. Packaging Information

8.1. Package Outline Drawing

The SX1235 is available in a 24-lead QFN package as shown in Figure 62.



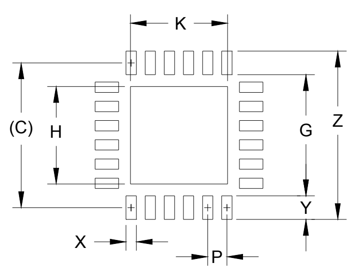
DIM	DIMENSIONS MILLIMETERS MIN	NOM	MAX
A	0.80	-	1.00
A1	0.00	-	0.05
A2	-	(0.20)	-
b	0.25	0.30	0.35
D	4.90	5.00	5.10
D1	3.20	3.25	3.30
E	4.90	5.00	5.10
E1	3.20	3.25	3.30
e		0.65 BSC	
L	0.35	0.40	0.45
N		24	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 62. Package Outline Drawing

8.2. Recommended Land Pattern



DIM	DIMENSIONS MILLIMETERS
C	(4.90)
G	4.10
H	3.30
K	3.30
P	0.65
X	0.35
Y	0.80
Z	5.70

NOTES:

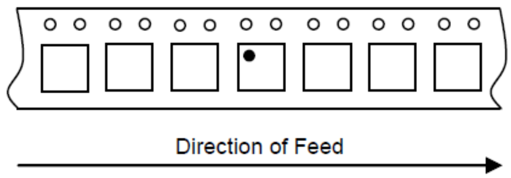
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

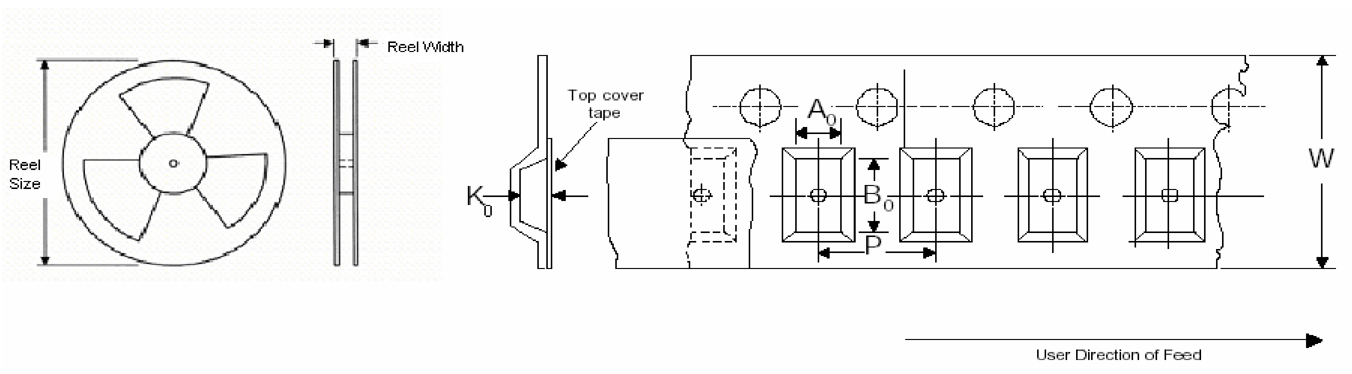
Figure 63. Recommended Land Pattern

8.3. Thermal Impedance

The thermal impedance of this package is: **Theta ja = 23.8° C/W typ.**, calculated from a package in still air, on a 4-layer FR4 PCB, as per the Jedec standard.

8.4. Tape & Reel Specification





Carrier Tape				Reel					
Tape Width (W)	Pocket Pitch (P)	Ao / Bo	Ko	Reel Size	Reel Width	Min. Trailer Length	Min. Leader Length	QTY per	Unit
12 +/-0.30	8 +/-0.10	5.25 +/-0.20	1.10 +/-0.10	330.2	12.4	400	400	3000	mm

Figure 64. Tape & Reel Specification

Note Single sprocket holes

9. Revision History

Table 42 Revision History

Revision	Date	Comment
1	December 2012	First release

Contact information

Semtech Corporation

Wireless & Sensing Products Division

200 Flynn Road, Camarillo, CA 93012

Phone: (805) 498-2111 Fax: (805) 498-3804

E-mail: sales@semtech.com

support_rf@semtech.com

Internet: http://www.semtech.com