SC1116
Linear FET Controller For DDR Supplies

Description

The SC1116 is a low cost controller for low power linear DDR power supplies.

The SC1116 comes in a space saving SOT-23 6 pin package.

The SC1116 provides a dual gate drive for the top serial and bottom parallel MOSFETs with internal shoot through protection.

The wide range of input voltages (3V to 15V) allows the chip to work in many various applications.

The variable output voltage is programmable from the outside with an input divider or an external reference.

Wide range of V_{DDQ}, down to 0.5V

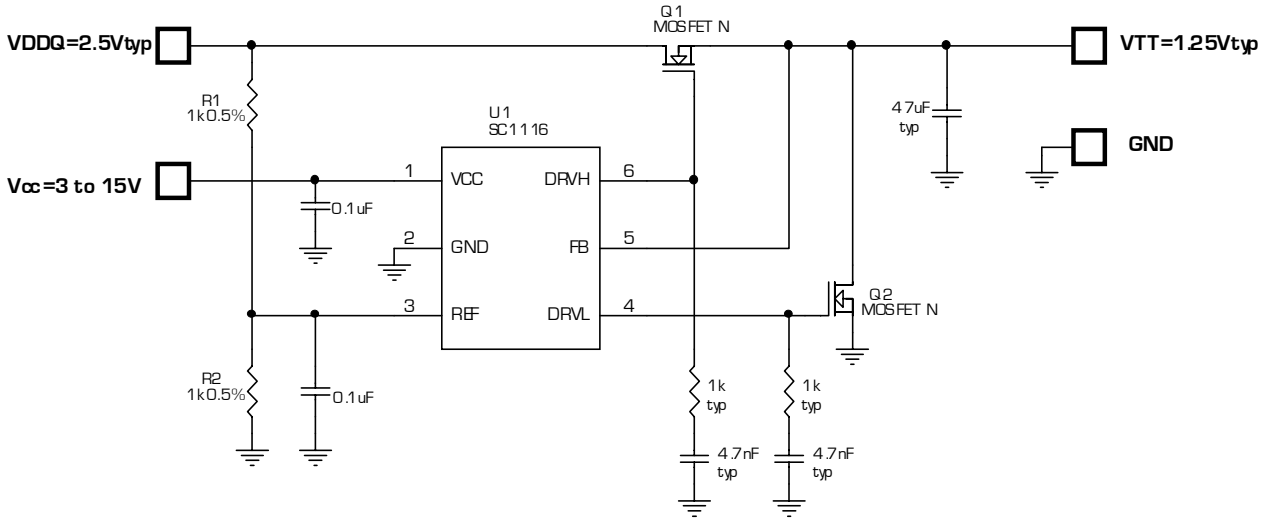
Features

- User can select FETs to optimize system current rating/dropout/cost
- Low V_{DDQ}, 0.5V to 2.5V
- -40°C to +85°C operating temperature
- External compensation capable for low ESR loads
- Minimum external components
- 0.6 mA Quiescent current
- Guaranteed no shoot through
- SOT-23 6L small package. Fully WEEE and RoHS compliant

Applications

- DDR supplies
- SCSI
- Line termination
- Source / Sink LDOs

Typical Application Circuit



Notes:
(1) Values used for optional compensation are 1K and 4.7nF typical.
(2) When using 3V as Vcc, use of low threshold FETs is a must.

Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V_{CC}	-0.3 to +16.5	V
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Thermal Impedance Junction to Ambient	θ_{JA}	95.7	°C/W
Thermal Impedance Junction to Case	θ_{JC}	61.7	°C/W
Power Dissipation at T_A = 25°C	P_D	250	mW
Lead Temperature (Soldering) 10 seconds	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

Electricial Characteristics

Unless otherwise specified, V_{CC} = 5V, 0.5V ≤ V_{DDQ} ≤ 2.5V, R1 = R2 = 1kΩ +/- 0.1%.

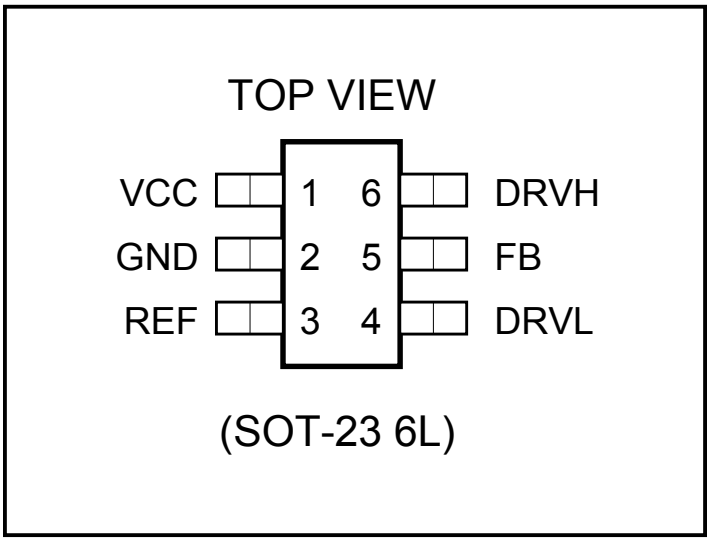
Specifications with standard typeface are for T_J = 25°C, and limits in **boldface** type apply over the full operating temperature range (T_A = -40°C to +85°C).

Parameter	Test Conditions	Min	Typ	Max	Units
Supply Voltage		3		15	V
Load Regulation (1)	IL: 0 + 3A IL: 0 - 3A		-1 +1		%
Quiescent Current/Standby Current	V_{CC} = 15V, no load = 0A		600	**800**	µA
FB & REF Input Current	V_{CC} = 15V			100	nA
Gate Drive					
Output Low	I_{SINK} = 2.5mA		0.15	**0.25**	V
Output High	I_{SOURCE} = 2.5mA	**Vcc -0.25**	Vcc -0.15		V

Note:

(1) For Load Regulation testing use a low duty cycle current pulse, when measuring VTT.

Pin Configuration



Ordering Information

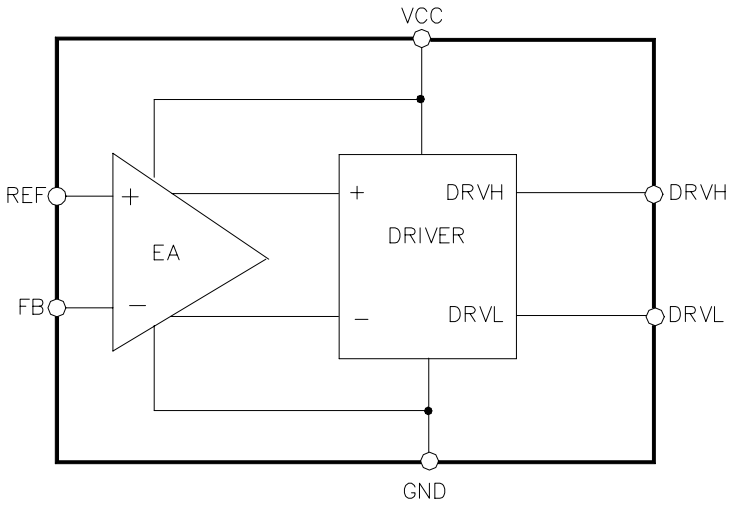
Part Number	Top Mark	Package
SC1116ISKTR (1)	AH00	SOT-23 6L
SC1116ISKTRT (1)(2)		

Notes:
(1) Only available in tape and reel packaging. A reel contains 3000 devices.
(2) Lead free option. Fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	VCC	Supply pin, connect a 3V to 15V supply and decouple to ground with a 0.1µF ceramic capacitor.
2	GND	Power and signal ground.
3	REF	Reference input. Output voltage will be regulated to this voltage.
4	DRVL	Low side FET drive output.
5	FB	Feedback pin.
6	DRVH	High side FET drive output.

Block Diagram



Application Information

Overview

The SC1116 linear controller is designed to meet the JEDEC specifications for termination of DDR-SDRAM. Double Data Rate (DDR) memory is clocked at the same speed as older SDRAM (synchronous dynamic random access memory), yet handles twice the amount of data by using the rising and falling edge of the clock signal for data transfers. Another difference is that DDR memory requires 2.5V instead of 3.3V used by standard SDRAM. The other feature that separates DDR memory from a conventional type is employment of the V_{TT} – termination voltage. Main requirements for the V_{TT} are that it must track variations of V_{DDQ} and be able to supply (source) current, and absorb (sink) current.

The SC1116 controller offers a low cost solution for DDR termination voltage regulation by using external pass elements (MOSFETs). Having the flexibility of choosing the MOSFETs allows for optimization on the basis of cost/size/performance of the specific application.

Test Circuit & Waveforms

The test circuit is shown below in Figure 1.
Note that V_{REF} voltage is supplied externally to eliminate inaccuracy caused by resistor divider.

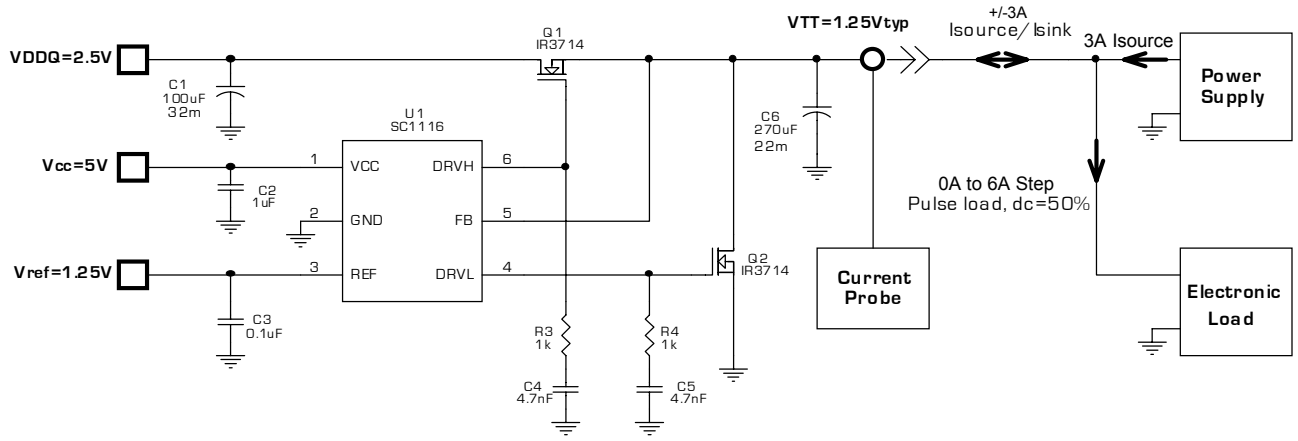
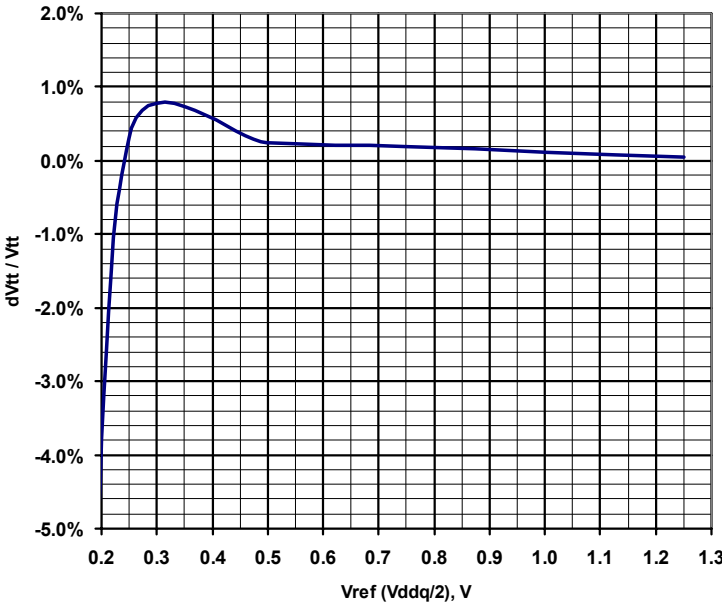


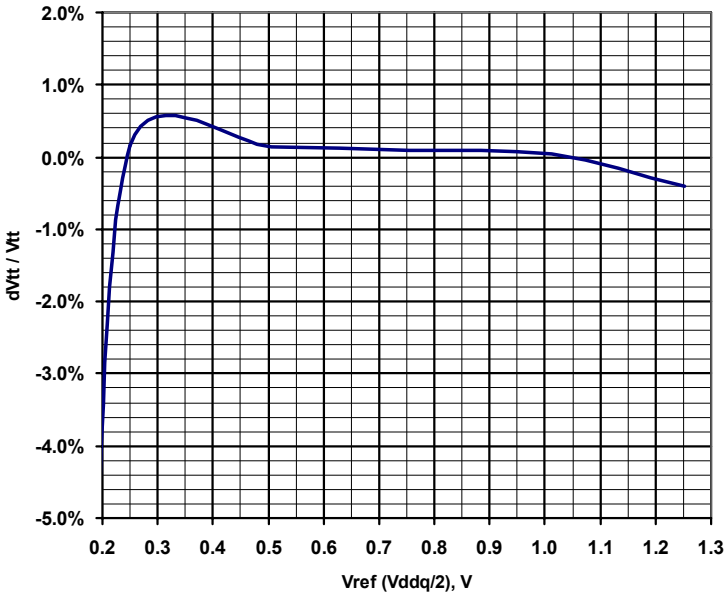
Figure 1.

Typical Characteristics

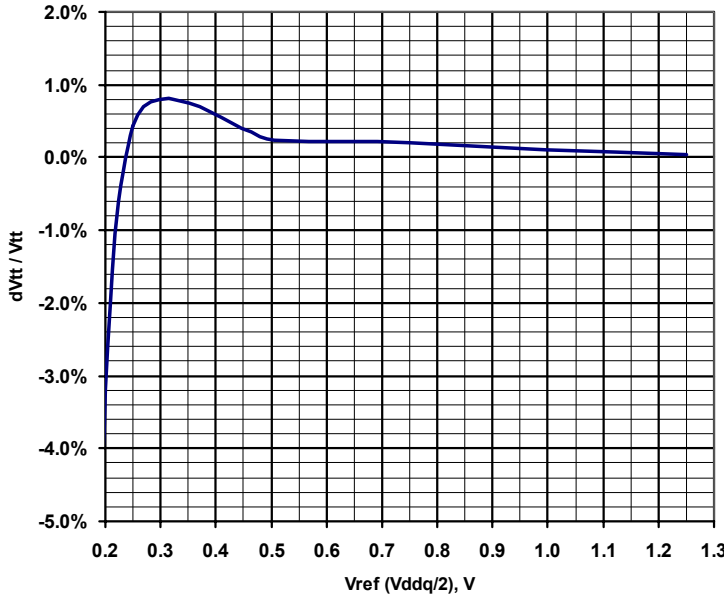
Regulation Vtt vs. Vref @ Is/s=1A; Vcc=5V



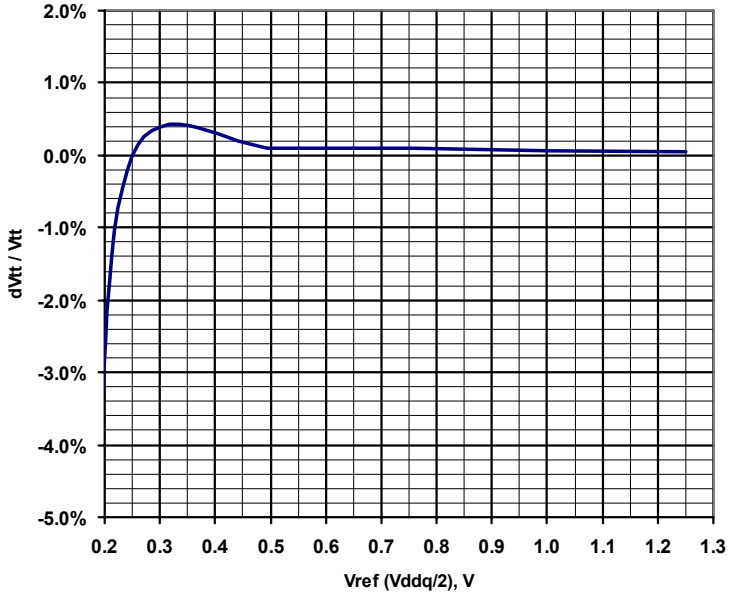
Regulation Vtt vs. Vref @ Is/s=5A; Vcc=5V



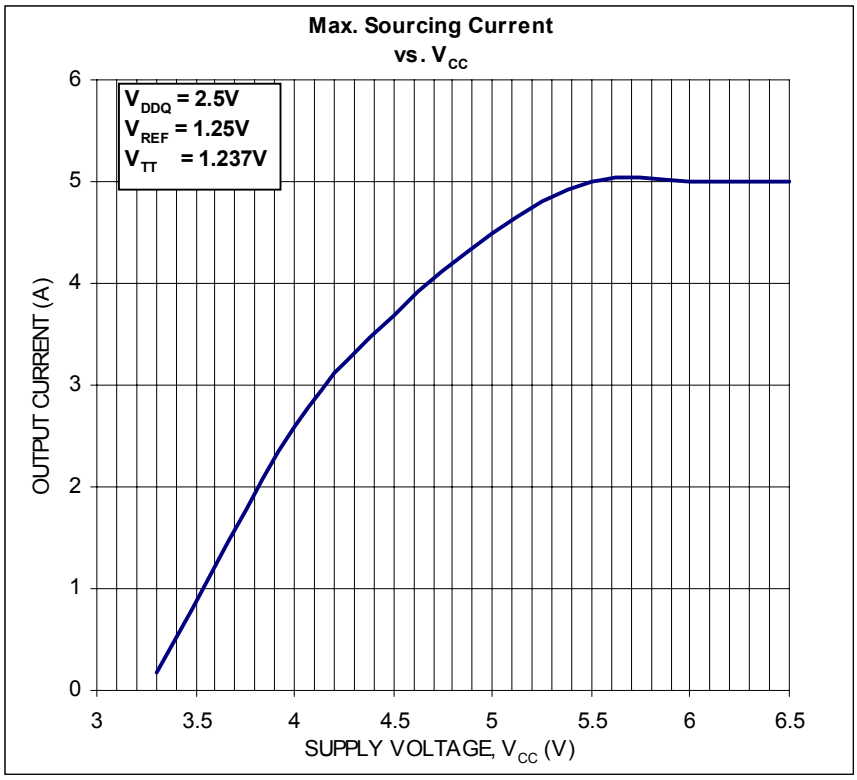
Regulation Vtt vs. Vref @ Is/s=1A; Vcc=12V

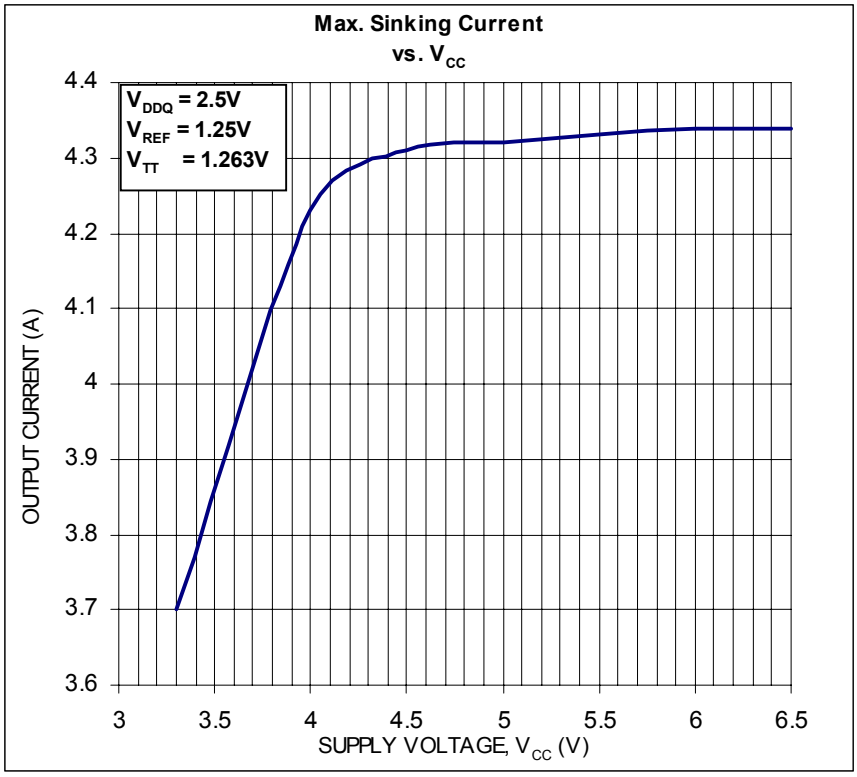


Regulation Vtt vs. Vref @ Is/s=5A; Vcc=12V

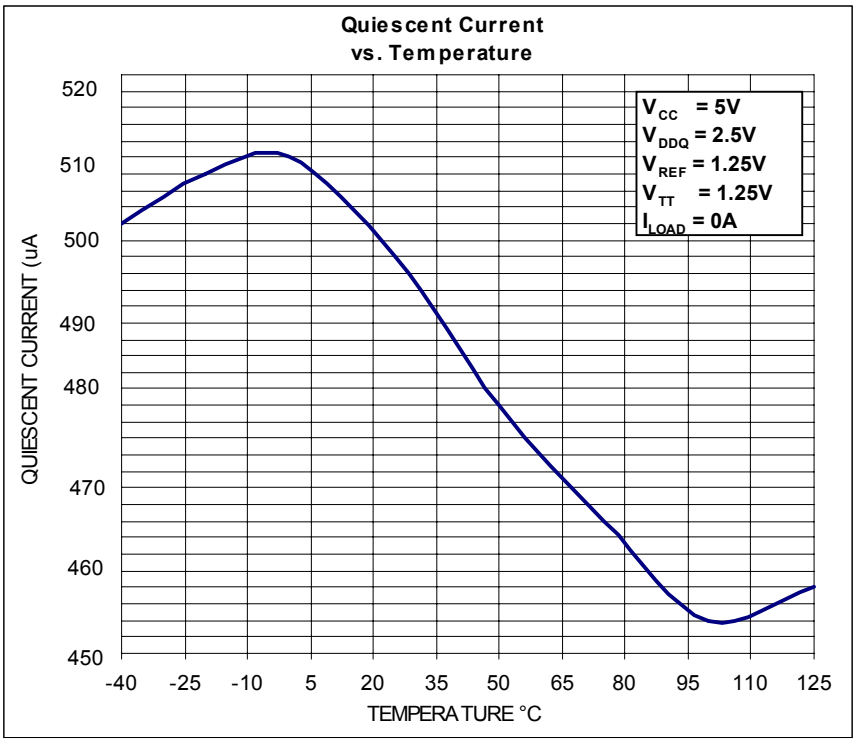


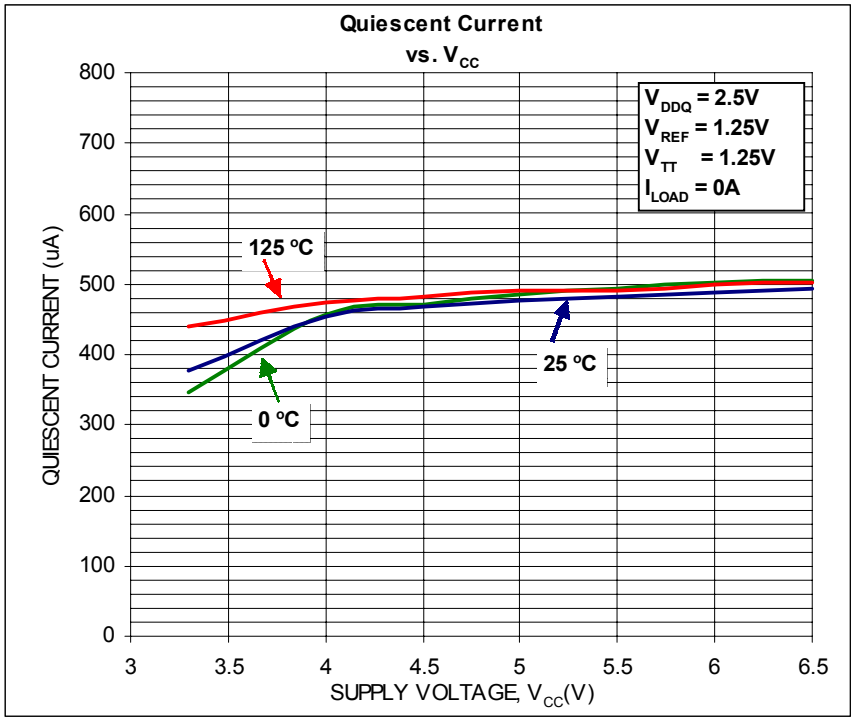
Typical Characteristics (Cont.)





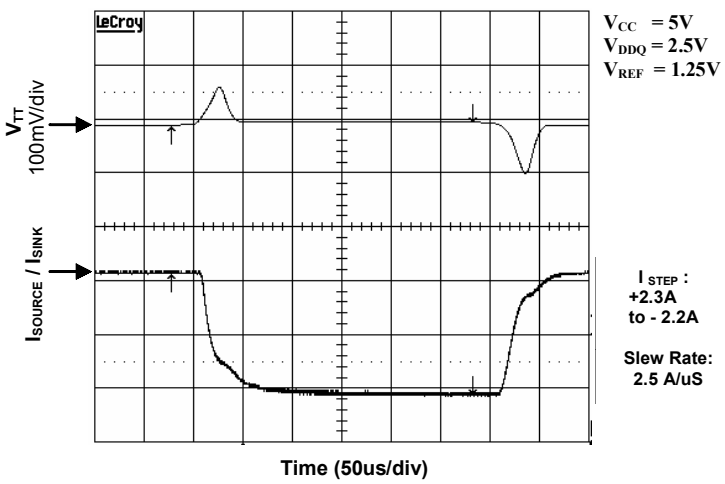
Typical Characteristics (Cont.)

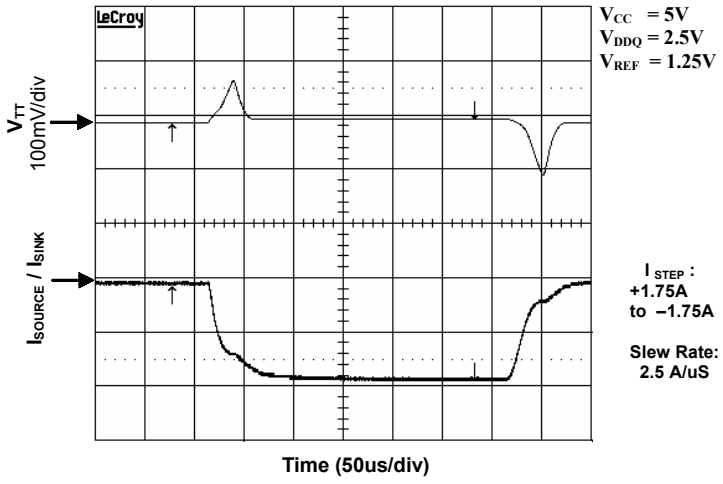


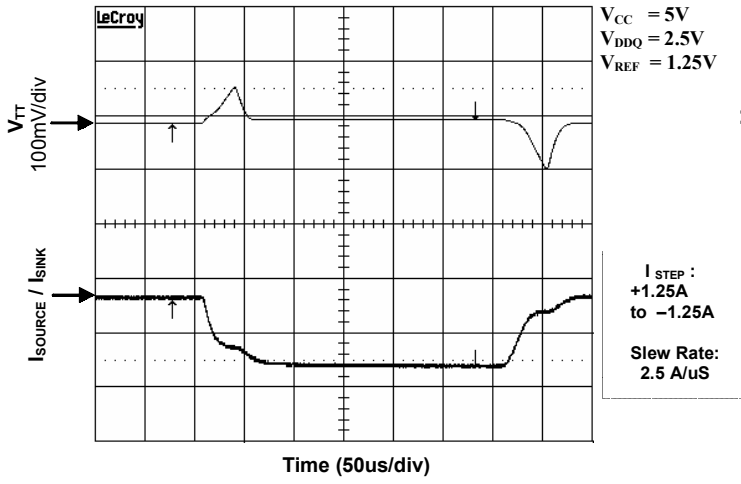


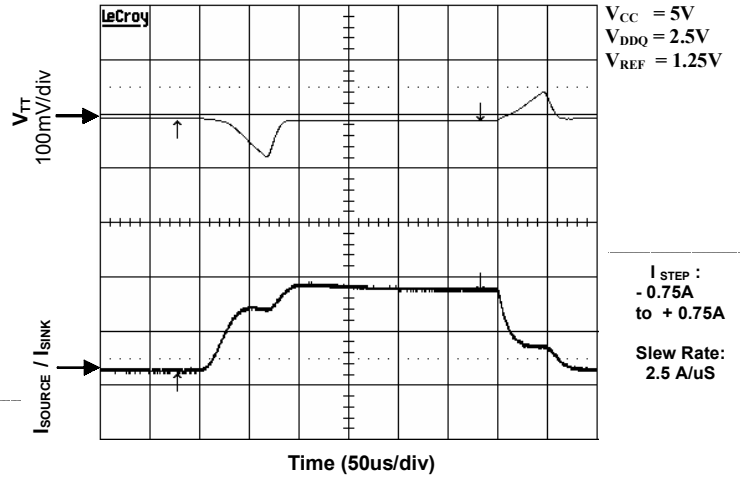
Test Waveforms

V_{TT} Transient Response



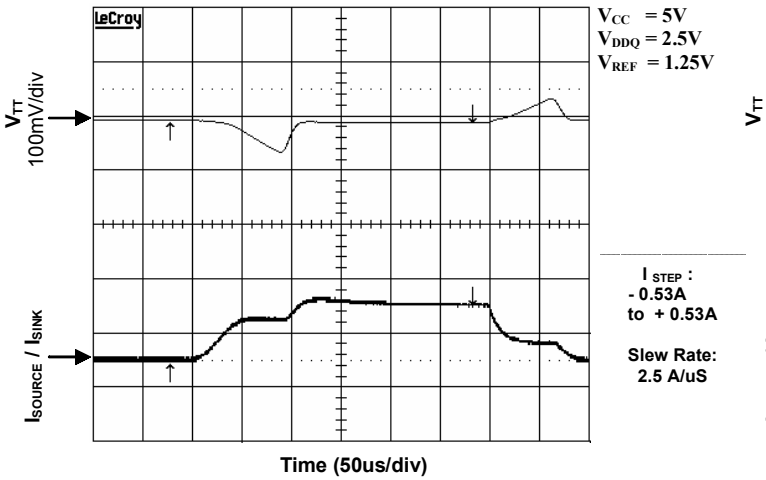


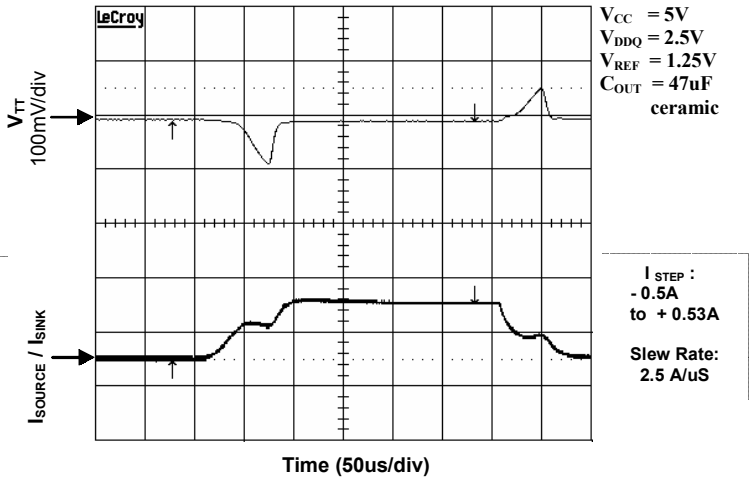


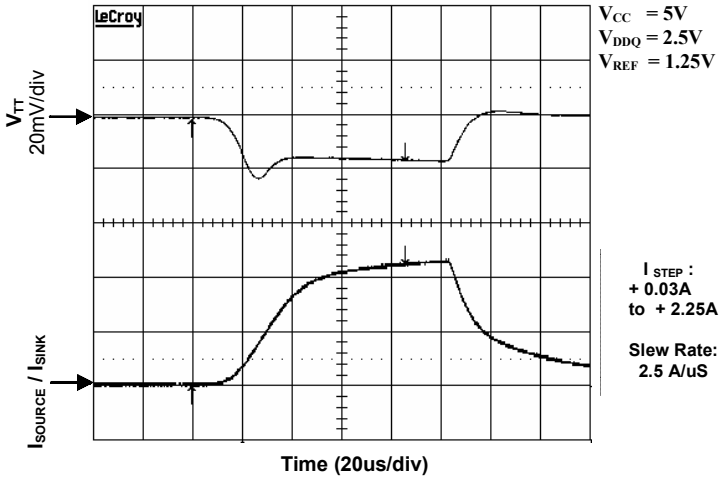


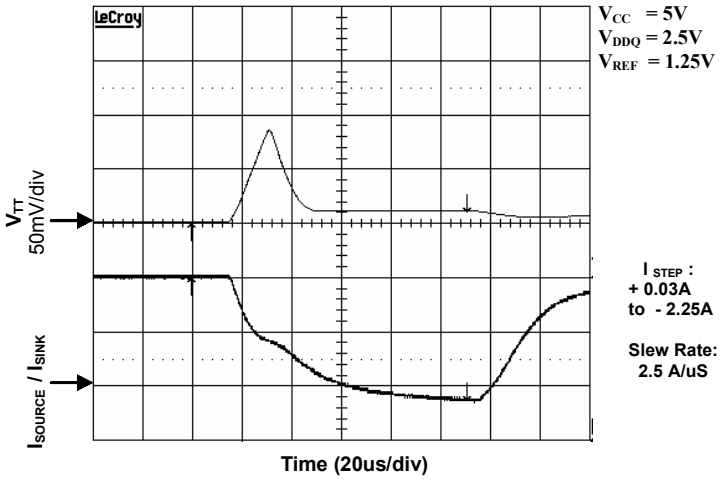
Test Waveforms (Cont.)

V_{TT} Transient Response



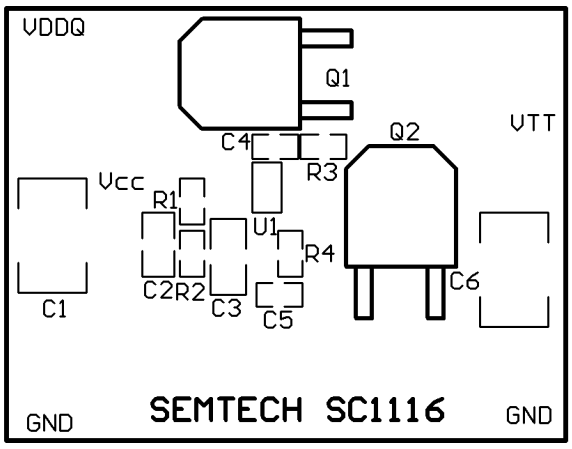




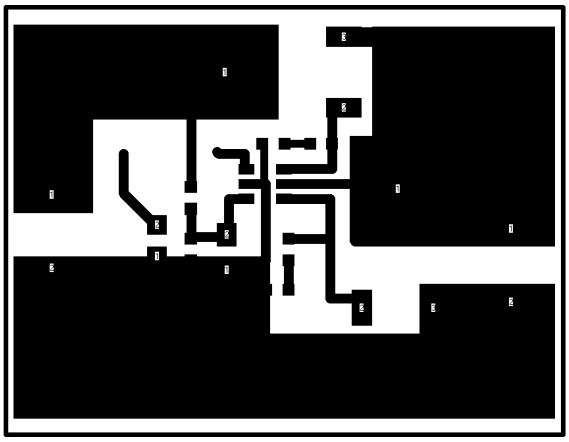


Evaluation Board

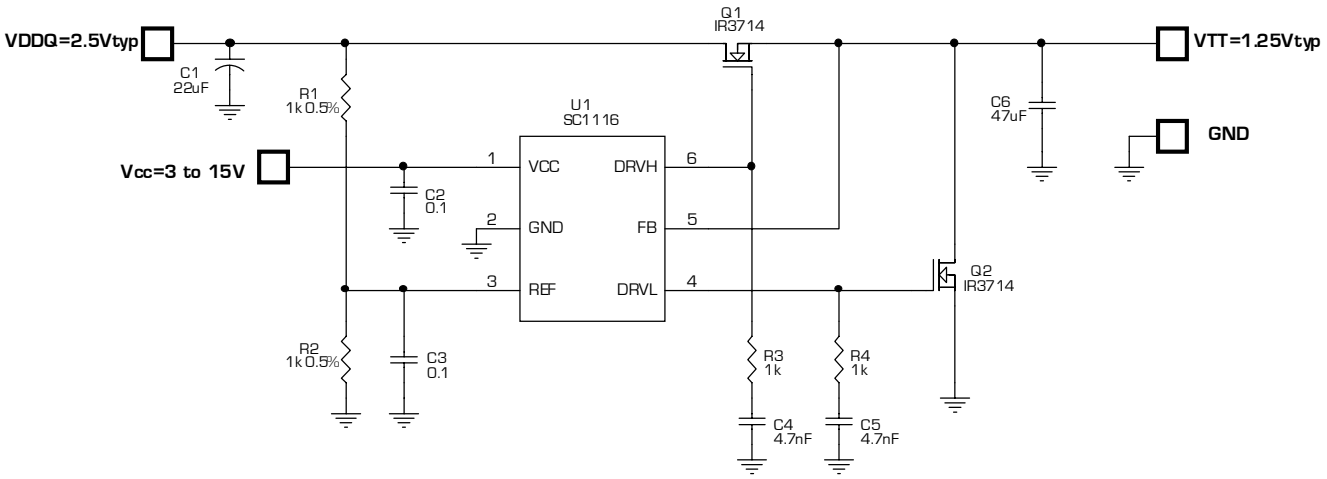
Top View



Top Layer

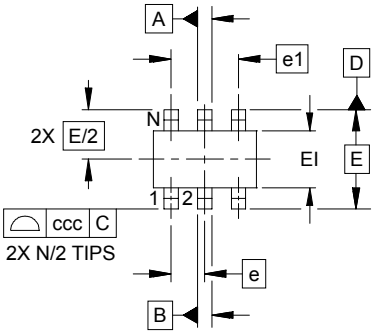


Evaluation Board Schematic

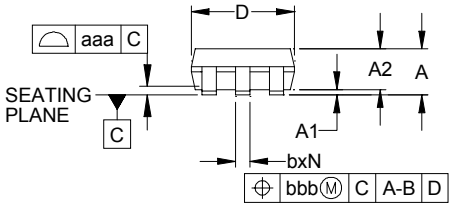


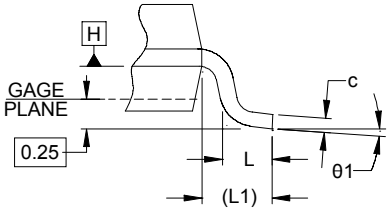
Notes:
(1) Values used for optional compensation are 1K and 4.7nF typical.
(2) When using 3V as Vcc, use of low threshold FETs is a must.

Outline Drawing - SOT-23-6

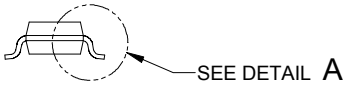


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.035	-	.057	0.90	-	1.45
A1	.000	-	.006	0.00	-	0.15
A2	.035	.045	.051	.90	1.15	1.30
b	.010	-	.020	0.25	-	0.50
c	.003	-	.009	0.08	-	0.22
D	.110	.114	.122	2.80	2.90	3.10
E1	.060	.063	.069	1.50	1.60	1.75
E	.110 BSC			2.80 BSC		
e	.037 BSC			0.95 BSC		
e1	.075 BSC			1.90 BSC		
L	.012	.018	.024	0.30	0.45	0.60
L1	(.024)			(0.60)		
N	6			6		
θ1	0°	-	10°	0°	-	10°
aaa	.004			0.10		
bbb	.008			0.20		
ccc	.008			0.20		





DETAIL A

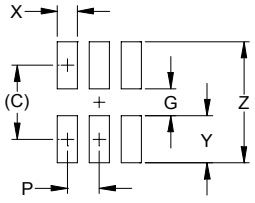


SIDE VIEW

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Minimum Land Pattern - SOT-23-6



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.098)	(2.50)
G	.055	1.40
P	.037	0.95
X	.024	0.60
Y	.043	1.10
Z	.141	3.60

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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