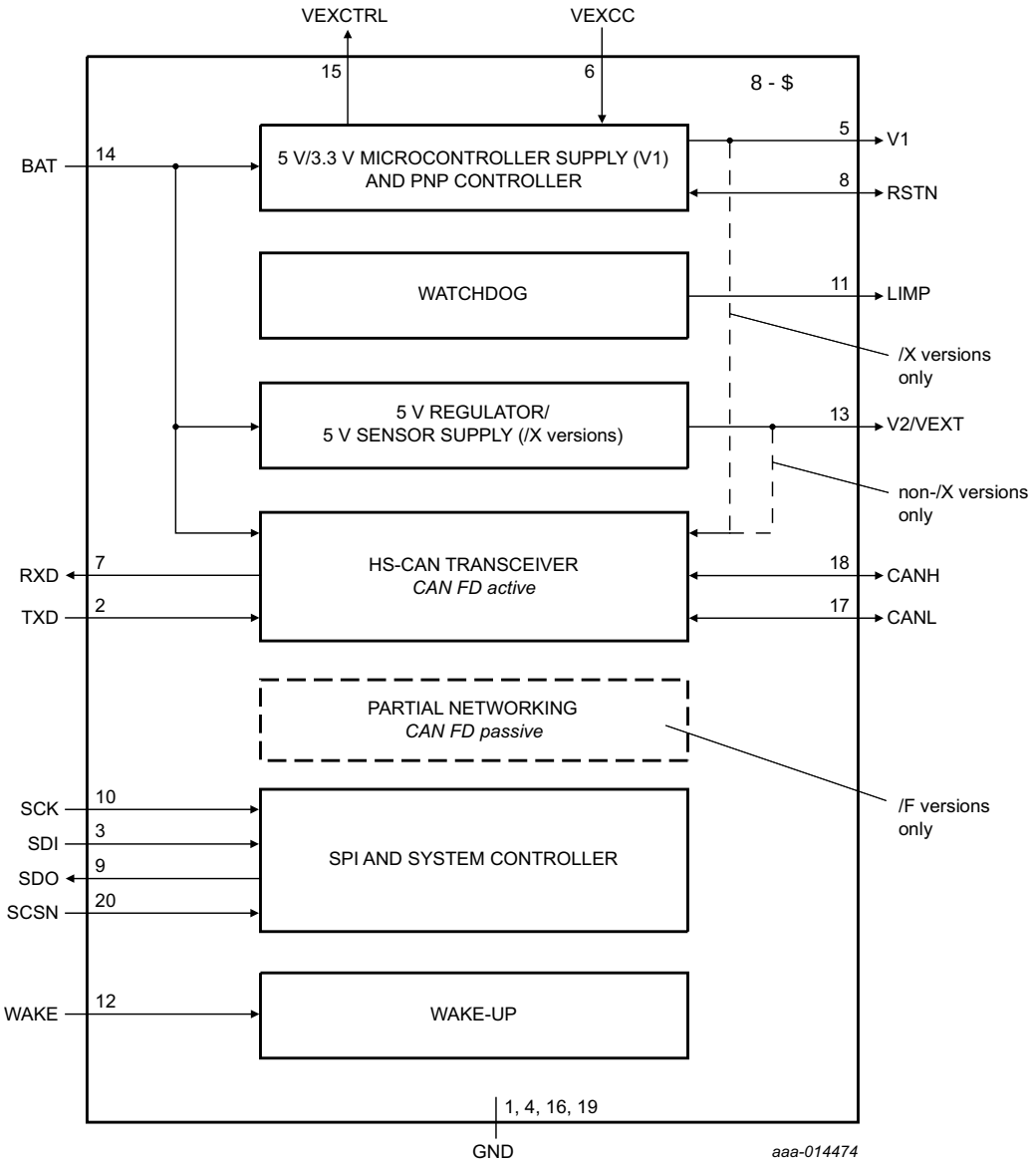
1. General description

The UJA1169 is a mini high-speed CAN System Basis Chip (SBC) containing an ISO 11898-2:201x (upcoming merged ISO 11898-2/5/6) compliant HS-CAN transceiver and an integrated 5 V or 3.3 V 250 mA scalable supply (V1) for a microcontroller and/or

5. Block diagram



The internal CAN transceiver is supplied from V1 in the UJA1169TK/X and UJA1169TK/X/F and from V2 in the other variants.

Fig 1. Block diagram of UJA1169

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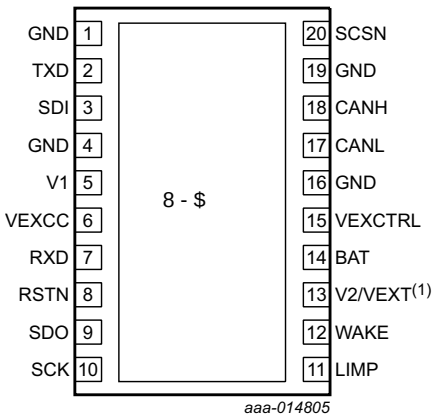
6. Pinning information

6.1 Pinning



(1) V2 in the UJA1169TK, UJA1169TK/3, UJA1169TK/F and UJA1169TK/F/3; VEXT in the UJA1169TK/X and UJA1169TK/X/F

Fig 2. Pin configuration diagram

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1[1]	ground
TXD	2	transmit data input
SDI	3	SPI data input
GND	4[1]	ground
V1	5	5 V/3.3 V microcontroller supply voltage
VEXCC	6	current measurement for external PNP transistor; this pin is connected to the collector of the external PNP transistor
RXD	7	receive data output; reflects data on bus lines and wake-up conditions
RSTN	8	reset input/output; active-LOW
SDO	9	SPI data output
SCK	10	SPI clock input
LIMP	11	limp home output, open-drain; active-LOW
WAKE	12	local wake-up input
V2	13	5 V CAN supply (UJA1169TK, UJA1169TK/3, UJA1169TK/F and UJA1169TK/F/3 only)
VEXT	13	5 V sensor supply (UJA1169TK/X and UJA1169TK/X/F only)
BAT	14	battery supply voltage
VEXCTRL	15	control pin of the external PNP transistor; this pin is connected to the base of the external PNP transistor
GND	16[1]	ground
CANL	17	LOW-level CAN-bus line

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Table 3. Pin description *…continued*

Symbol	Pin	Description
CANH	18	HIGH-level CAN-bus line
GND	19[1]	ground
SCSN	20	SPI chip select input; active-LOW

[1] The exposed die pad at the bottom of the package allows for better heat dissipation and grounding from the SBC via the printed circuit board. For enhanced thermal and electrical performance, connect the exposed die pad to GND.

7. Functional description

7.1 System controller

The system controller manages register configuration and controls the internal functions of the UJA1169. Detailed device status information is collected and made available to the microcontroller.

7.1.1 Operating modes

The system controller contains a state machine that supports seven operating modes: Normal, Standby, Sleep, Reset, Forced Normal, Overtemp and Off. The state transitions are illustrated in Figure 3.

7.1.1.1 Normal mode

Normal mode is the active operating mode. In this mode, all the hardware on the device is available and can be activated (see Table 4). Voltage regulator V1 is enabled to supply the microcontroller.

The CAN interface can be configured to be active and thus to support normal CAN communication. Depending on the SPI register settings, the watchdog may be running in Window or Timeout mode and the V2/VEXT output may be active.

7.1.1.2 Standby mode

Standby mode is the first-level power-saving mode of the UJA1169, offering reduced current consumption. The transceiver is unable to transmit or receive data in Standby mode. The SPI remains enabled and V1 is still active; the watchdog is active (in Timeout mode) if enabled. The behavior of V2/VEXT is determined by the SPI setting.

If remote CAN wake-up is enabled (CWE = 1; see Table 32), the receiver monitors bus activity for a wake-up request. The bus pins are biased to GND (via $R_{i(cm)}$) when the bus is inactive for $t > t_{to(silence)}$ and at approximately 2.5 V when there is activity on the bus (autonomous biasing). CAN wake-up can occur via a standard wake-up pattern or via a selective wake-up frame (selective wake-up is enabled when CPNC = PNCOK = 1, otherwise standard wake-up is enabled; see Table 15).

Pin RXD is forced LOW when any enabled wake-up event is detected. This event can be either a regular wake-up (via the CAN-bus or pin WAKE) or a diagnostic wake-up such as an overtemperature event (see Section 7.10).

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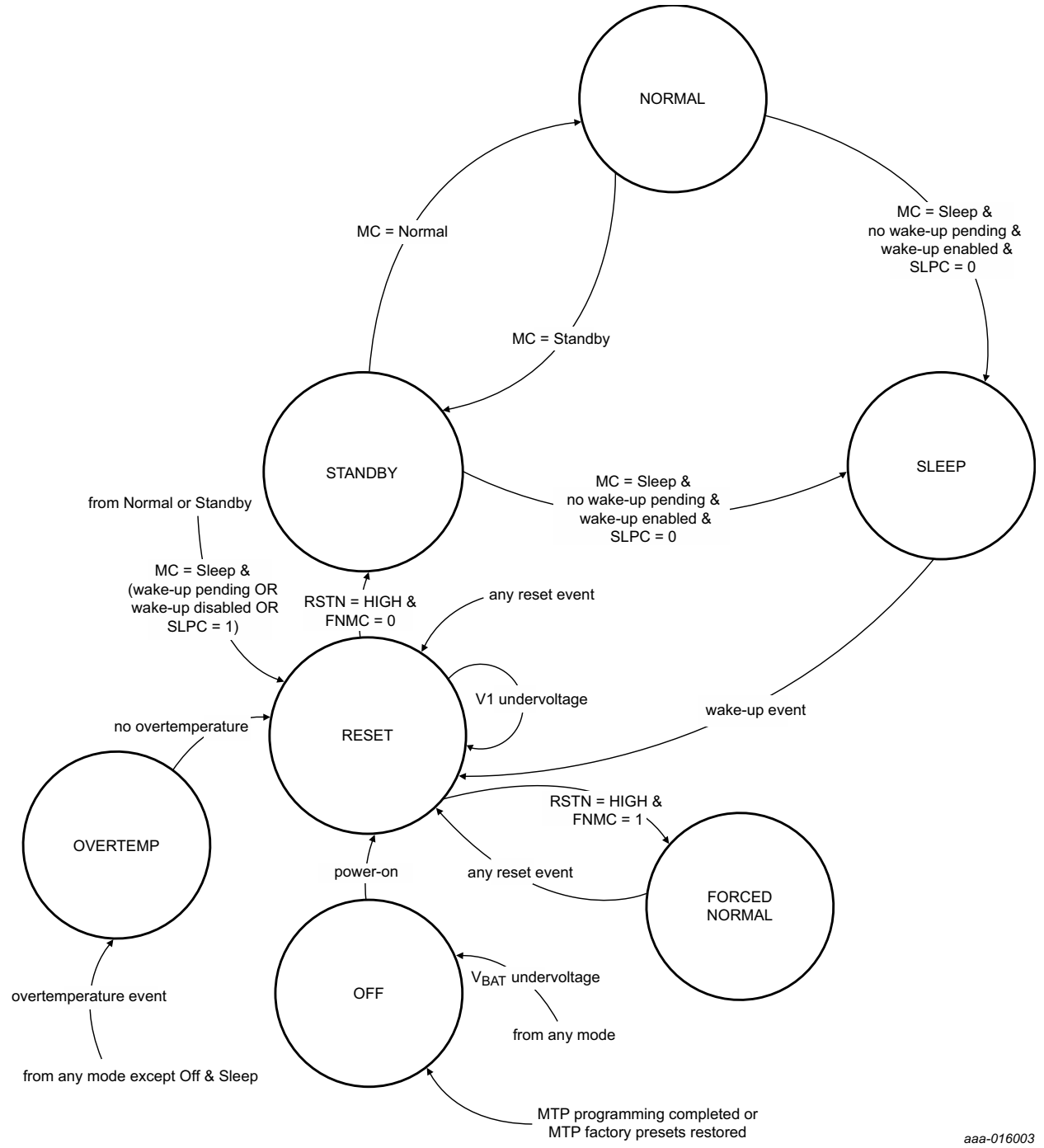

Fig 3. UJA1169 system controller state diagram

7.1.1.3 Sleep mode

Sleep mode is the second-level power-saving mode of the UJA1169. The difference between Sleep and Standby modes is that V1 is off in Sleep mode and temperature protection is inactive.

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Any enabled regular wake-up via CAN or WAKE or any diagnostic wake-up event will cause the UJA1169 to wake up from Sleep mode. The behavior of V2/VEXT is determined by the SPI settings. The SPI and the watchdog are disabled. Autonomous bus biasing is active.

Sleep mode can be permanently disabled in applications where, for safety reasons, the supply voltage to the host controller must never be cut off. Sleep mode is permanently disabled by setting the Sleep control bit (SLPC) in the SBC configuration register (see Table 9) to 1. This register is located in the non-volatile memory area of the device (see Section 7.11). When SLPC = 1, a Sleep mode SPI command (MC = 001) triggers an SPI failure event instead of a transition to Sleep mode.

7.1.1.4 Reset mode

Reset mode is the reset execution state of the SBC. This mode ensures that pin RSTN is pulled down for a defined time to allow the microcontroller to start up in a controlled manner.

The transceiver is unable to transmit or receive data in Reset mode. The behavior of V2/VEXT is determined by the settings of bits V2C/VEXTC and V2SUC/VEXTSUC (see Section 7.5.3). The SPI is inactive; the watchdog is disabled; V1 and overtemperature detection are active.

After the UJA1169 exits Reset mode (positive edge on RSTN), an SPI read/write access must not be attempted for at least $t_{to(SPI)}$. Any earlier access may be ignored (without generating an SPI failure event).

7.1.1.5 Off mode

The UJA1169 switches to Off mode when the battery is first connected or from any mode when $V_{BAT} < V_{th(det)poff}$. Only power-on detection is enabled; all other modules are inactive. The UJA1169 starts to boot up when the battery voltage rises above the power-on detection threshold $V_{th(det)pon}$ (triggering an initializat

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7.1.1.7 Forced Normal mode

Forced Normal mode simplifies SBC testing and is useful for initial prototyping as well as first flashing of the microcontroller. The watchdog is disabled in Forced Normal mode. The low-drop voltage regulator (V1) is active, VEXT/V2 is enabled and the CAN transceiver is active.

Bit FNMC is factory preset to 1, so the UJA1169 initially boots up in Forced Normal mode (see Table 9). This feature allows a newly installed device to be run in Normal mode without a watchdog. So the microcontroller can, optionally, be flashed via the CAN-bus without having to consider the integrated watchdog.

The register containing bit FNMC (address 74h) is stored in non-volatile memory. So once bit FNMC is programmed to 0, the SBC will no longer boot up in Forced Normal mode, allowing the watchdog to be enabled.

Even in Forced Normal mode, a reset event (e.g. an external reset or a V1 undervoltage) will trigger a transition to Reset mode with normal Reset mode behavior (except that the CAN transmitter remains active if there is no V_{CAN} undervoltage). When the UJA1169 exits Reset mode, however, it returns to Forced Normal mode instead of switching to Standby mode.

In Forced Normal mode, only the Main status register, the Watchdog status register, the Identification register and registers stored in non-volatile memory can be read. The non-volatile memory area is fully accessible for writing as long as the UJA1169 is in the factory preset state (for details see Section 7.11).

7.1.1.8 Hardware characterization for the UJA1169 operating modes

Table 4. Hardware characterization by functional block

Block	Operating mode						
	Off	**Forced Normal**	**Standby**	**Normal**	**Sleep**	**Reset**	**Overtemp**
V1	off[1]	on	on	on	off	on	off
VEXT/V2	off	on	[2]	[2]	[2]	[2]	VEXT/V2 off
RSTN	LOW	HIGH	HIGH	HIGH	LOW	LOW	LOW
SPI	disabled	active[3]	active	active	disabled	disabled	disabled
Watchdog	off	off	determined by bits WMC (see Table 8)[4]	determined by bits WMC	determined by bits WMC[4]	off	off
CAN	off	Active	Offline	Active/ Offline/ Listen-only (determined by bits CMC; see Table 15)	Offline	Offline	off
RXD	V1 level	CAN bit stream	V1 level/LOW if wake-up detected	CAN bit stream if CMC = 01/10/11; otherwise same as Standby/Sleep	V1 level/LOW if wake-up detected	V1 level/LOW if wake-up detected	V1 level/LOW if wake-up detected

[1] When the SBC switches from Reset, Standby or Normal mode to Off mode in the 5 V variants, V1 behaves as a current source during power down while V_{BAT} is falling from $V_{th(det)pof}$ down to 2 V (RAM retention feature; see Section 7.5.1).

[2] Determined by bits V2C/VEXTC and V2SUC/VEXTSUC (see Table 12)

[3] Limited register access: Main status register, Watchdog status register, Identification register and non-volatile memory only.

[4] Window mode is only active in Normal mode.

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7.1.2 System control registers

7.1.2.1 Mode control register (0x01)

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 0x01 (see Section 7.15).

Table 5. Mode control register (address 01h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	MC	R/W		mode control:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

7.1.2.2 Main status register (0x03)

The Main status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the UJA1169 has entered Normal mode after initial power-up. It also indicates the source of the most recent reset event.

Table 6. Main status register (address 03h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	
6	OTWS	R		overtemperature warning status:
			0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	UJA1169 has entered Normal mode (after power-up)
			1	UJA1169 has powered up but has not yet switched to Normal mode
4:0	RSS	R		reset source status:
			00000	left Off mode (power-on)
			00001	CAN wake-up in Sleep mode
			00100	wake-up via WAKE pin in Sleep mode
			01100	watchdog overflow in Sleep mode (Timeout mode)
			01101	diagnostic wake-up in Sleep mode
			01110	watchdog triggered too early (Window mode)
			01111	watchdog overflow (Window mode or Timeout mode with WDF = 1)
			10000	illegal watchdog mode control access
			10001	RSTN pulled down externally
			10010	left Overtemp mode
			10011	V1 undervoltage
			10100	illegal Sleep mode command received
			10110	wake-up from Sleep mode due to a frame detect error

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7.2 Watchdog

7.2.1 Watchdog overview

The UJA1169 contains a watchdog that supports three operating modes: Window, Timeout and Autonomous. In Window mode (available only in SBC Normal mode), a watchdog trigger event within a defined watchdog window triggers and resets the watchdog timer. In Timeout mode, the watchdog runs continuously and can be triggered and reset at any time within the watchdog period by a watchdog trigger. Watchdog time-out mode can also be used for cyclic wake-up of the microcontroller. In Autonomous mode, the watchdog can be off or autonomously in Timeout mode, depending on the selected SBC mode (see Section 7.2.5).

The watchdog mode is selected via bits WMC in the Watchdog control register (Table 8). The SBC must be in Standby mode when the watchdog mode is changed. If Window mode is selected (WMC = 100), the watchdog remains in (or switches to) Timeout mode until the SBC enters Normal mode. Any attempt to change the watchdog operating mode (via WMC) while the SBC is in Normal mode causes the UJA1169 to switch to Reset mode and the reset source status bits (RSS) to be set to 10000 (‘illegal watchdog mode control access’; see Table 6).

Eight watchdog periods are supported, from 8 ms to 4096 ms. The watchdog period is programmed via bits NWP. The selected period is valid for both Window and Timeout modes. The default watchdog period is 128 ms.

A watchdog trigger event resets the watchdog timer. A watchdog trigger event is any valid write access to the Watchdog control register. If the watchdog mode or the watchdog period have changed as a result of the write access, the new values are immediately valid.

Table 7. Watchdog configuration

Operating/watchdog mode						
FNMC (Forced Normal mode control)		0	0	0	0	1
SDMC (Software Development mode control)		x	x	0	1	x
WMC (watchdog mode control)		100 (Window)	010 (Timeout)	001 (Autonomous)	001 (Autonomous)	n.a.
SBC Operating Mode	Normal mode	Window	Timeout	Timeout	off	off
	Standby mode (RXD HIGH)[1]	Timeout	Timeout	off	off	off
	Standby mode (RXD LOW)[1]	Timeout	Timeout	Timeout	off	off
	Sleep mode	Timeout	Timeout	off	off	off
	Other modes	off	off	off	off	off

[1] RXD LOW signals a pending wake-up.

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7.2.1.1 Watchdog control register (0x00)

Table 8. Watchdog control register (address 00h)

Bit	Symbol	Access	Value	Description
7:5	WMC	R/W		watchdog mode control:
			001[1]	Autonomous mode
			010[2]	Timeout mode
			100[3]	Window mode
4	reserved	R	-	
3:0	NWP	R/W		nominal watchdog period:
			1000	8 ms
			0001	16 ms
			0010	32 ms
			1011	64 ms
			0100[2]	128 ms
			1101	256 ms
			1110	1024 ms
			0111	4096 ms

[1] Default value if SDMC = 1 (see Section 7.2.2)

[2] Default value.

[3] Selected in Standby mode but only activated when the SBC switches to Normal mode.

The watchdog is a valuable safety mechanism, so it is critical that it is configured correctly. Two features are provided to prevent watchdog parameters being changed by mistake:

- redundant coding of configuration bits WMC and NWP
- reconfiguration protection in Normal mode

Redundant codes associated with control bits WMC and NWP ensure that a single bit error cannot cause the watchdog to be configured incorrectly (at least 2 bits must be changed to reconfigure WMC or NWP). If an attempt is made to write an invalid code to WMC or NWP (e.g. 011 or 1001 respectively), the SPI operation is abandoned and an SPI failure event is captured, if enabled (see Section 7.10).

7.2.1.2 SBC configuration control register (0x74)

Two operating modes have a major impact on the operation of the watchdog: Forced Normal mode and Software Development mode (Software Development mode is provided for test and development purposes only and is not a dedicated SBC operating mode; the UJA1169 can be in any functional operating mode with Software Development mode enabled; see Section 7.2.2). These modes are enabled and disabled via bits FNMC and SDMC respectively in the SBC configuration control register (see Table 9). Note that this register is located in the non-volatile memory area. The watchdog is disabled in Forced Normal mode (FNM). In Software Development mode (SDM), the watchdog can be disabled or activated for test and software debugging purposes.

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Table 9. SBC configuration control register (address 74h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5:4	V1RTSUC	R/W	[1]	V1 undervoltage threshold (defined by bit V1RTC) at start-up:
			00[2]	V1 undervoltage detection at 90 % of nominal value at start-up (V1RTC = 00)
			01	V1 undervoltage detection at 80 % of nominal value at start-up (V1RTC = 01)
			10	V1 undervoltage detection at 70 % of nominal value at start-up (V1RTC = 10)
			11	V1 undervoltage detection at 60 % of nominal value at start-up (V1RTC = 11)
3	FNMC	R/W	[3]	Forced Normal mode control:
			0	Forced Normal mode disabled
			1[2]	Forced Normal mode enabled
2	SDMC	R/W		Software Development mode control:
			0[2]	Software Development mode disabled
			1	Software Development mode enabled
1	reserved	R	-	
0	SLPC	R/W		Sleep control:
			0[2]	Sleep mode commands accepted
			1	Sleep mode commands ignored

[1] The V1 undervoltage threshold is fixed at 90 % in the UJA1169TK/3 and UJA1169TK/F/3, regardless of the setting of bit V1RTSUC.

[2] Factory preset value.

[3] FNMC settings overrule SDMC.

7.2.1.3 Watchdog status register (0x05)

Information on the status of the watchdog is available from the Watchdog status register (Table 10). This register also indicates whether Forced Normal and Software Development modes are active.

Table 10. Watchdog status register (address 05h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	
3	FNMS	R/W		Forced Normal mode status:
			0	SBC is not in Forced Normal mode
			1	SBC is in Forced Normal mode
2	SDMS	R/W		Software Development mode status:
			0	SBC is not in Software Development mode
			1	SBC is in Software Development mode

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Table 10. Watchdog status register (address 05h) *…continued*

Bit	Symbol	Access	Value	Description
1:0	WDS	R		watchdog status:
			00	watchdog is off
			01	watchdog is in first half of the nominal period
			10	watchdog is in second half of the nominal period
			11	reserved

7.2.2 Software Development mode

Software Development mode is provided to simplify the software design process. When Software Development mode is enabled, the watchdog starts up in Autonomous mode (WMC = 001) and is inactive after a system reset, overriding the default value (see Table 8). The watchdog is always off in Autonomous mode if Software Development mode is enabled (SDMC = 1; see Table 7).

However, it is possible to activate and deactivate the watchdog for test purposes by selecting Window or Timeout mode via bits WMC while the SBC is in Standby mode.

7.2.3 Watchdog behavior in Window mode

In Window mode, the watchdog can only be triggered during the second half of the watchdog period. If the watchdog overflows, or is triggered in the first half of the watchdog period (before $t_{trig(wd)1}$), a system reset is performed. After the system reset, the reset source (either 'watchdog triggered too early' or 'watchdog overflow') can be read via the reset source status bits (RSS) in the Main Status register (Table 6). If the watchdog is triggered in the second half of the watchdog period (after $t_{trig(wd)1}$ but before $t_{trig(wd)2}$), the watchdog timer is restarted.

7.2.4 Watchdog behavior in Timeout mode

In Timeout mode, the watchdog timer can be reset at any time by a watchdog trigger. If the watchdog overflows, a watchdog failure event (WDF) is captured. If a WDF is already pending when the watchdog overflows, a system reset is performed. In Timeout mode, the watchdog can be used as a cyclic wake-up source for the microcontroller when the UJA1169 is in Standby or Sleep mode. In Sleep mode, a watchdog overflow generates a wake-up event while setting WDF.

When the SBC is in Sleep mode with watchdog Timeout mode selected, a wake-up event is generated after the nominal watchdog period (NWP), setting WDF. RXD is forced LOW and V1 is turned on. The application software can then clear the WDF bit and trigger the watchdog before it overflows again.

7.2.5 Watchdog behavior in Autonomous mode

In Autonomous mode, the watchdog will not be running when the SBC is in Standby (RXD HIGH) or Sleep mode. If a wake-up event is captured, pin RXD is forced LOW to signal the event and the watchdog is automatically restarted in Timeout mode. If the SBC was in Sleep mode when the wake-up event was captured, it switches to Standby mode.

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7.2.6 Exceptional behavior of the watchdog after writing to the Watchdog register

A successful write operation to the Watchdog control register resets the watchdog timer. Bits WDS are set to 01 and the watchdog restarts at the beginning of the watchdog period (regardless of the selected watchdog mode). However, the watchdog may restart unexpectedly in the second half of the watchdog period or a WDF interrupt may be captured under the following conditions.

Case A: When the watchdog is running in Timeout mode (see Table 7) and a new watchdog period is selected (via bits NWP) that is shorter than the existing watchdog period, one of both of the following events may occur.

Status bits WDS can be set to 10. The timer then restarts at the beginning of the second half of the watchdog period, causing the watchdog to overflow earlier than expected. This can be avoided by writing the new NWP (or NWP + WMC) code twice whenever the watchdog period needs to be changed. The write commands should be sent consecutively. The gap between the commands must be less than half of the new watchdog period.

If the watchdog is in the second half of the watchdog period when the watchdog period is changed, the timer will be reset correctly. The watchdog then restarts at the beginning of the watchdog period and WDS is set 01. However, a WDF event may be captured unexpectedly. To counteract this effect, the WDF event should be cleared by default after the new watchdog period has been selected as described above (two consecutive write commands).

Case B: If the watchdog is triggered in Timeout mode (see Table 7) at exactly the same time that WDS is set to 10, it will start up again in the second half of the watchdog period. As in Case A, this causes the watchdog to overflow earlier than expected. This behavior appears identical to an ignored watchdog trigger event and can be avoided by issuing two consecutive watchdog commands. The second command should be issued before the end of the first half of the watchdog period. Use this trigger scheme if it is possible that the watchdog could be triggered exactly in the middle of the watchdog window.

7.3 System reset

When a system reset occurs, the SBC switches to Reset mode and initiates process that generates a low-level pulse on pin RSTN. The UJA1169 can distinguish up to 13 different reset sources, as detailed in Table 6.

7.3.1 Characteristics of pin RSTN

Pin RSTN is a bidirectional open-drain low side driver with integrated pull-up resistance, as shown in Figure 4. With this configuration, the SBC can detect the pin being pulled down externally, e.g. by the microcontroller. The input reset pulse width must be at least $t_{w(rst)}$ to guarantee that external reset events are detected correctly.

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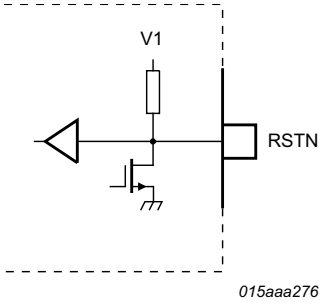

Fig 4. RSTN internal pin configuration

7.3.2 Selecting the output reset pulse width

The duration of the output reset pulse is selected via bits RLC in the Start-up control register (Table 11). The SBC distinguishes between a cold start and a warm start. A cold start is performed if the reset event was combined with a V1 undervoltage event (power-on reset, reset during Sleep mode, over-temperature reset, V1 undervoltage before entering or while in Reset mode). The setting of bits RLC determines the output reset pulse width for a cold start.

A warm start is performed if any other reset event occurs without a V1 undervoltage (external reset, watchdog failure, watchdog change attempt in Normal mode, illegal Sleep mode command). The SBC uses the shortest reset length ($t_{w(rst)}$ as defined when RLC = 11).

7.3.2.1 Start-up control register (0x73)

Table 11. Start-up control register (address 73h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5:4	RLC	R/W		RSTN output reset pulse width:
			00[1]	$t_{w(rst)}$ = 20 ms to 25 ms
			01	$t_{w(rst)}$ = 10 ms to 12.5 ms
			10	$t_{w(rst)}$ = 3.6 ms to 5 ms
			11	$t_{w(rst)}$ = 1 ms to 1.5 ms
3	V2SUC[2] VEXTSUC[3]	R/W		V2/VEXT start-up control:
			0[1]	bits V2C/VEXTC set to 00 at power-up
			1	bits V2C/VEXTC set to 11 at power-up
2:0	reserved	R	-	

[1] Factory preset value.

[2] UJA1169TK, UJA1169TK/3, UJA1169TK/F and UJA1169TK/F/3 only.

[3] UJA1169TK/X and UJA1169TK/X/F only.

7.4 Global temperature protection

The temperature of the UJA1169 is monitored continuously, except in Sleep and Off modes. The SBC switches to Overtemp mode if the temperature exceeds the overtemperature protection activation threshold, $T_{th(act)otp}$. In addition, pin RSTN is driven

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LOW and V1, V2/VEXT and the CAN transceiver are switched off (if the optional external PNP transistor is connected, it will also be; see Section 7.5.2). When the temperature drops below the overtemperature protection release threshold, $T_{th(rel)otp}$, the SBC switches to Standby mode via Reset mode.

In addition, the UJA1169 provides an overtemperature warning. When the IC temperature rises about the overtemperature warning threshold ($T_{th(warn)otp}$), status bit OTWS is set and an overtemperature warning event is captured (OTW = 1).

7.5 Power supplies

7.5.1 Battery supply voltage (V_{BAT})

The internal circuitry is supplied from the battery via pin BAT. The device must be protected against negative supply voltages, e.g. by using an external series diode. If V_{BAT} falls below the power-off detection threshold, $V_{th(det)poff}$, the SBC switches to Off mode. However, in the 5 V variants, the microcontroller supply voltage (V1) remains active until V_{BAT} falls below 2 V, ensuring memory in the connected microcontroller remains active for as long as possible (RAM retention feature; not available in the 3.3 V variants).

The SBC switches from Off mode to Reset mode $t_{startup}$ after the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$. Power-on event status bit PO is set to 1 to indicate the UJA1169 has powered up and left Off mode (see Table 26).

7.5.2 Voltage regulator V1

The UJA1169 provides a 5 V or 3.3 V supply (V1), depending on the variant. V1 can deliver up to 250 mA load current. In the UJA1169TK/X and UJA1169TK/X/F variants, the CAN transceiver is supplied internally via V1, reducing the output current available for external components.

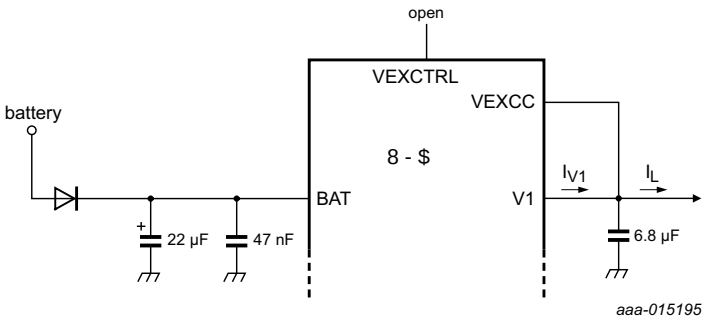

Fig 5. Typical application without external PNP (showing example component values)

To prevent the device overheating at high ambient temperatures or high average currents, an external PNP transistor can be connected as illustrated in Figure 6. In this configuration, the power dissipation is distributed between the SBC (I_{V1}) and the PNP transistor (I_{PNP}).

The PNP transistor is activated when the load current reaches the PNP activation threshold, $I_{th(act)PNP}$. Bit PDC in the Regulator control register (Table 12) is used to regulate how power dissipation is distributed.

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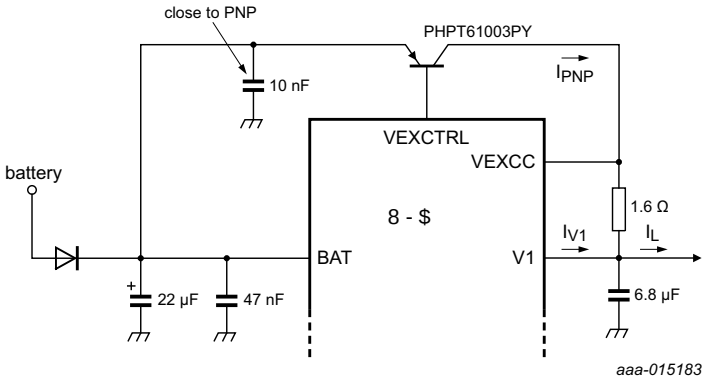

Fig 6. Typical application with external PNP (showing example component values)

For short-circuit protection, a resistor must be connected between pins V1 and VEXCC to allow the current to be monitored. This resistor limits the current delivered by the external transistor. If the voltage difference between pins VEXCC and V1 reaches $V_{th(act)Ilim}$, the PNP current limiting activation threshold voltage, the transistor current will not increase further. In general, any PNP transistor with a current amplification factor (Ē of between 50 and 500 can be used.

The output voltage on V1 is monitored. A system reset is generated if the voltage on V1 drops below the selected undervoltage threshold (60 %, 70 %, 80 % or 90 % of the nominal V1 output voltage for the 5 V variants, selected via V1RTC in the Regulator control register; fixed at 90 % for the 3.3 V variants; see Table 12).

The default value of the undervoltage threshold at power-up is determined by the value of bits V1RTSUC in the SBC configuration control register (Table 9). The SBC configuration control register is in non-volatile memory, allowing the user to define the default undervoltage threshold (V1RTC) at any battery start-up.

In addition, an undervoltage warning (a V1U event; see Section 7.10) is generated if the voltage on V1 falls below 90 % of the nominal value (and V1U event detection is enabled, V1UE = 1; see Table 31). This information can be used as a warning, when the 60 %, 70 % or 80 % threshold is selected in the 5 V variants, to indicate that the level on V1 is outside the nominal supply range. The status of V1, whether it is above or below the 90 % undervoltage threshold, can be polled via bit V1S in the Supply voltage status register (Table 13).

7.5.3 Voltage regulator V2

In the UJA1169TK, UJA1169TK/3, UJA1169TK/F and UJA1169TK/F/3, pin 13 is a voltage regulator output (V2) delivering up to 100 mA.

The CAN transceiver is supplied internally from V2, consuming a portion of the available current. V2 is not protected against shorts to the battery or to negative voltages and should not be used to supply off-board components.

V2 is software controlled and must be turned on (via bit V2C in the Regulator control register; see Table 12) to activate the supply voltage for the internal CAN transceiver. V2 is not required for wake-up detection via the CAN interface.

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The default value of V2C at power-on is defined by bits V2SUC in non-volatile memory (see Section 7.11). The actual status of V2 can be polled from the Supply voltage status register (Table 13).

7.5.4 Voltage regulator VEXT

In the UJA1169TK/X and UJA1169TK/X/F, pin 13 is a voltage regulator output (VEXT) that can be used to supply off-board components, delivering up to 100 mA. VEXT is protected against short-circuits to the battery and negative voltages. Since the CAN controller is supplied internally via V1, the full 100 mA supply current is available for off-board loads connected to VEXT (provided the thermal limits of the PCB are not exceeded).

VEXT is software controlled and must be turned on (via bit VEXTC in the Regulator control register; see Table 12) to activate the supply voltage for off-board components.

The default value of VEXTC at power-on is defined by bits VEXTSUC in non-volatile memory (see Section 7.11). The status of VEXT can be read from the Supply voltage status register (Table 13).

7.5.5 Regulator control register (0x10)

Table 12. Regulator control register (address 10h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	
6	PDC	R/W		power distribution control:
			0	V1 threshold current for activating the external PNP transistor, load current rising; $I_{th(act)PNP}$ (higher value; see Table 52) V1 threshold current for deactivating the external PNP transistor, load current falling; $I_{th(deact)PNP}$ (higher value; see Table 52)
			1	V1 threshold current for activating the

[1] UJA1169TK, UJA1169TK/3, UJA1169TK/F and UJA1169TK/F/3: default value at power-up defined by V2SUC bit setting (see Table 11).

[2] UJA1169TK/X and UJA1169TK/X/F: default value at power-up defined by VEXTSUC bit setting (see Table 11).

[3] 5 V variants only; default value at power-up defined by setting of bits V1RTSUC (see Table 9). The threshold is fixed at 90 % in the 3.3 V variants and V1RTC always reads 00 (regardless of the value written to V1RTC or the start-up threshold defined by V1RTSUC).

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7.5.6 Supply voltage status register (0x1B)

Table 13. Supply voltage status register (address 1Bh)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:1	V2S[1] VEXTS[2]	R/W		V2/VEXT status:
			00[3]	V2/VEXT voltage ok
			01	V2/VEXT output voltage below undervoltage threshold
			10	V2/VEXT output voltage above overvoltage threshold
			11	V2/VEXT disabled
0	V1S	R/W		V1 status:
			0[3]	V1 output voltage above 90 % undervoltage threshold
			1	V1 output voltage below 90 % undervoltage threshold

[1] UJA1169TK, UJA1169TK/3, UJA1169TK/F and UJA1169TK/F/3 only.

[2] UJA1169TK/X and UJA1169TK/X/F only.

[3] Default value at power-up.

7.6 LIMP output

The dedicated LIMP pin can be used to enable so called ‘limp home’ hardware in the event of a serious ECU failure. Detectable failure conditions include SBC overtemperature events, loss of watchdog service, short-circuits on pins RSTN or V1 and user-initiated or external reset events (see Figure 7). The LIMP pin is a battery-robust, active-LOW, open-drain output. The LIMP pin can also be forced LOW by setting bit LHC in the Fail-safe control register (Table 14).

7.6.1 Reset counter

The UJA1169 uses a reset counter to detect serious failures. The reset counter is incremented (bits RCC = RCC + 1; see Table 14) every time the SBC enters Reset mode. When the system is running correctly, it is expected that the system software will reset this counter (RCC = 00) periodically to ensure that routinely expected reset events do not cause it to overflow.

If RCC is equal to 3 when the SBC enters Reset mode, the SBC assumes that a serious failure has occurred and sets the limp-home control bit, LHC. This action forces the external LIMP pin LOW with RCC overflowing to RCC = 0. Bit LHC can also be set via the SPI interface.

The LIMP pin is set floating again if LHC is reset to 0 through software control or at power-up when the SBC leaves Off mode.

The application software can preset the counter value to define how many reset events are tolerated before the limp-home function is activated. If RCC is initialized to 3, for example, the next reset event will immediately trigger the limp-home function. The default counter setting at power-up is RCC = 00.

Besides a reset counter (RCC) overflow, the following events cause bit LHC to be set and immediately trigger the limp-home function:

- overtemperature lasting longer than $t_{d(limp)}$

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7.6.2.1 Fail-safe control register (0x02)

The Fail-safe control register contains the reset counter along with limp home control settings.

Table 14. Fail-safe control register (address 02h)

Bit	Symbol	Access	Value	Description
7:3	reserved			
2	LHC	R/W		LIMP home control:
			0	LIMP pin is floating
			1	LIMP pin is driven LOW
1:0	RCC	R/W		reset counter control:
			xx	incremented every time the SBC enters Reset mode while FNMC = 0; RCC overflows from 11 to 00; default at power-on is 00

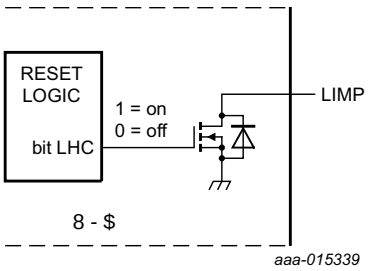

Fig 8. LIMP pin functional diagram

7.7 High-speed CAN transceiver

The integrated high-speed CAN transceiver is designed for active communication at bit rates up to 1 Mbit/s, providing differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2:201x (upcoming merged ISO 11898-2/5/6 standard) compliant. Depending on the derivative, the CAN transmitter is supplied internally from V1 (in /X variants) or V2 (in variants with a V2 regulator). Additional timing parameters defining loop delay symmetry are included to ensure reliable communication in fast phase at data rates up to 2 Mbit/s, as used in CAN FD networks.

The CAN transceiver supports autonomous CAN biasing as defined in ISO 11898-6:2013 and ISO 11898-2:201x. CANH and CANL are always biased to 2.5 V when the transceiver is in Active or Listen-only modes (CMC = 01/10/11; see Table 15).

Autonomous biasing is active in CAN Offline mode, to 2.5 V if there is activity on the bus (CAN Offline Bias mode) and to GND if there is no activity on the bus for $t > t_{to(silence)}$ (CAN Offline mode). The autonomous CAN bias voltage is derived directly from V_{BAT}.

7.7.1 CAN operating modes

The integrated CAN transceiver supports four operating modes: Active, Listen-only, Offline and Offline Bias (see Figure 9). The CAN transceiver operating mode depends on the UJA1169 operating mode and on the setting of bits CMC in the CAN control register (Table 15).

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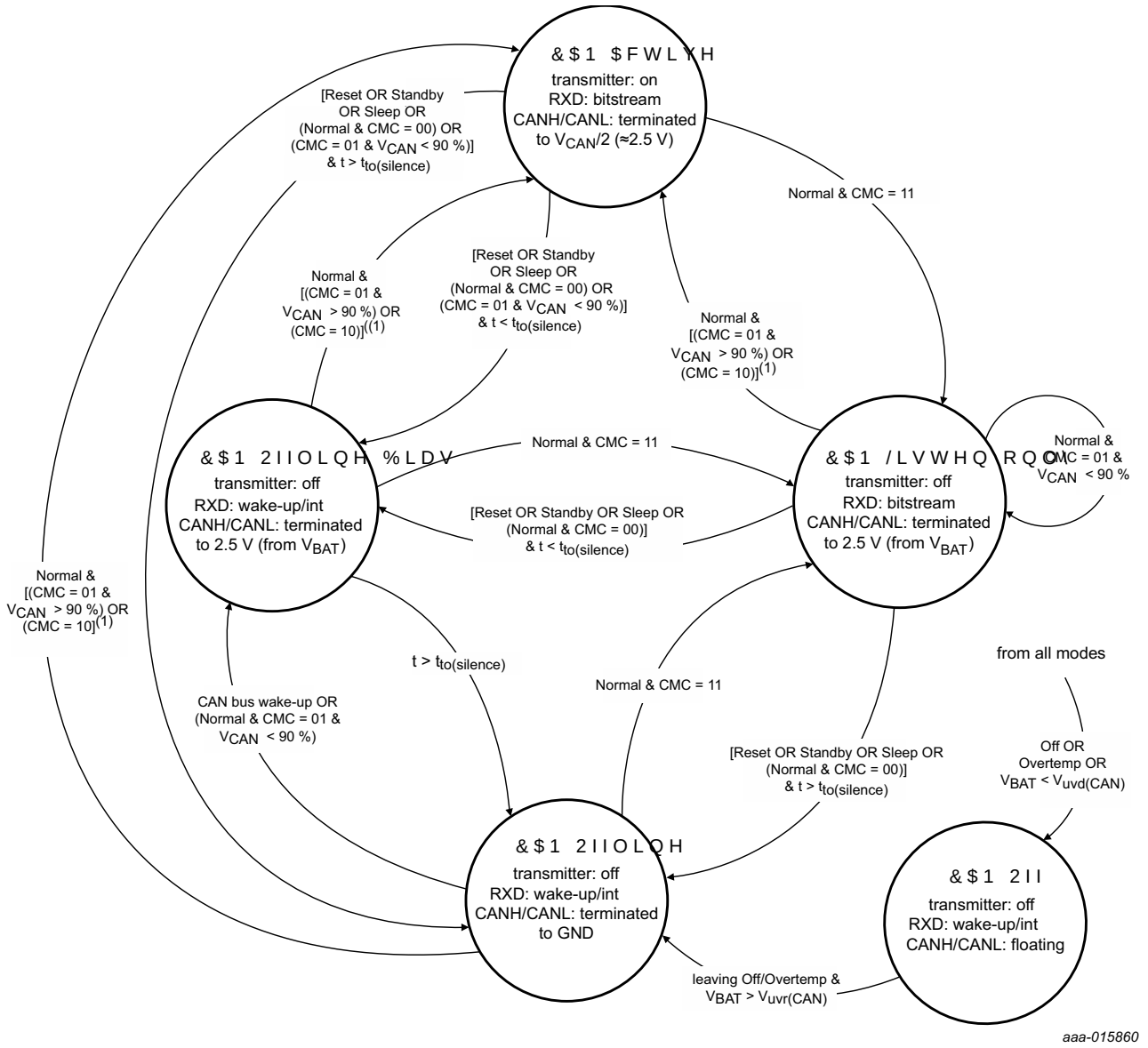
7.7.1.4 CAN Off mode

In CAN Off mode, bus pins CANH and CANL are set floating with respect to GND, which prevents reverse currents flowing from the bus to an unsupplied ECU. The differential input resistance between CANH and CANL remains constant.



(1) To prevent the bus lines being driven to a permanent dominant state, the transceiver will not switch to CAN Active mode or CAN Listen-only mode if pin TXD is held LOW (e.g. by a short-circuit to GND)

Fig 9. CAN transceiver state machine (with FNMC = 0)

7.7.2 CAN standard wake-up (partial networking not enabled)

If the CAN transceiver is in Offline mode and CAN wake-up is enabled (CWE = 1), but CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0), the UJA1169 monitors the bus for a wake-up pattern.

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A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. A dominant-recessive-dominant wake-up pattern must be transmitted on the CAN-bus within the wake-up time-out time ($t_{to(wake)}$) to pass the wake-up filter and trigger a wake-up event (see Figure 10; note that additional pulses may occur between the recessive/dominant phases). The recessive and dominant phases must last at least $t_{wake(busrec)}$ and $t_{wake(busdom)}$, respectively.

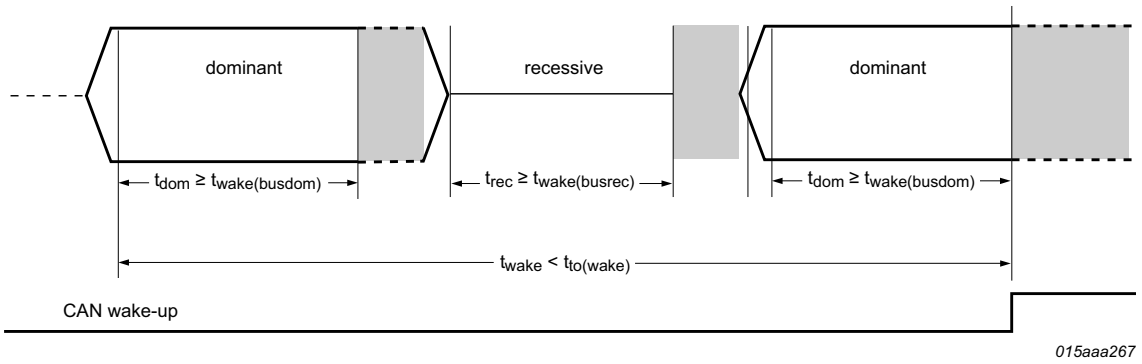

Fig 10. CAN wake-up timing

When a valid CAN wake-up pattern is detected on the bus, wake-up bit CW in the Transceiver event status register is set (see Table 28) and pin RXD is driven LOW. If the SBC was in Sleep mode when the wake-up pattern was detected, V1 is enabled to supply the microcontroller and the SBC switches to Standby mode via Reset mode.

7.7.2.1 CAN control register (0x20)

Table 15. CAN control register (address 20h)

Bit	Symbol	Access	Value	Description
7	reserved	R/W	-	
6	CFDC[1]	R/W		CAN FD control:
			0	CAN FD tolerance disabled
			1	CAN FD tolerance enabled
5	PNCOK[1]	R/W		CAN partial networking configuration OK:
			0	partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	partial networking registers configured successfully
4	CPNC[1]	R/W		CAN partial networking control:
			0	disable CAN selective wake-up
			1	enable CAN selective wake-up
3:2	reserved	R	-	

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Table 15. CAN control register (address 20h) *...continued*

Bit	Symbol	Access	Value	Description
1:0	CMC	R/W		CAN mode control:
			00	Offline mode
			01	Active mode (when the SBC is in Normal mode); CAN supply undervoltage detection active
			10	Active mode (when the SBC is in Normal mode); CAN supply undervoltage detection disabled
			11	Listen-only mode

[1] UJA1169TK/F and UJA1169TK/X/F only; otherwise reserved.

7.7.2.2 Transceiver status register (0x22)

Table 16. Transceiver status register (address 22h)

Bit	Symbol	Access	Value	Description
7	CTS	R		CAN transceiver status:
			0	CAN transceiver not in Active mode
			1	CAN transceiver in Active mode
6	CPNERR[1]	R		CAN partial networking error:
			0	no CAN partial networking error detected (PNFDE = 0 AND PNCOK = 1)
			1	CAN partial networking error detected (PNFDE = 1 OR PNCOK = 0; wake-up via standard wake-up pattern only)
5	CPNS[1]	R		CAN partial networking status:
			0	CAN partial networking configuration error detected (PNCOK = 0)
			1	CAN partial networking configuration ok (PNCOK = 1)
4	COSCS[1]	R		CAN oscillator status:
			0	CAN partial networking oscillator not running at target frequency
			1	CAN partial networking oscillator running at target frequency
3	CBSS	R		CAN-bus silence status:
			0	CAN-bus active (communication detected on bus)
			1	CAN-bus inactive (for longer than $t_{to(silence)}$)
2	reserved	R	-	
1	VCS[2]	R		V_{CAN} status:
			0	CAN supply voltage is above the 90 % threshold
			1	CAN supply voltage is below the 90 % threshold
0	CFS	R		CAN failure status:
			0	no TXD dominant time-out event detected
			1	CAN transmitter disabled due to a TXD dominant time-out event

[1] UJA1169TK/F and UJA1169TK/X/F only; otherwise reserved reading 0.

[2] Only active when CMC = 01.

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7.8 CAN partial networking (UJA1169 /F variants only)

Partial networking allows nodes in a CAN network to be selectively activated in response to dedicated wake-up frames (WUF). Only nodes that are functionally required are active on the bus while the other nodes remain in a low-power mode until needed.

If both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver monitors the bus for dedicated CAN wake-up frames.

7.8.1 Wake-up frame (WUF)

A wake-up frame is a CAN frame according to ISO11898-1:2003, consisting of an identifier field (ID), a Data Length Code (DLC), a data field and a Cyclic Redundancy Check (CRC) code including the CRC delimiter.

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register (Table 20).

A valid WUF identifier is defined and stored in the ID registers (Table 18). An ID mask can be defined to allow a group of identifiers to be recognized as valid by an individual node. The identifier mask is defined in the ID mask registers (Table 19), where a 1 means ‘don’t care’.

In the example illustrated in Figure 11, based on the standard frame format, the 11-bit identifier is defined as 0x1A0. The identifier is stored in ID registers 2 (0x29) and 3 (0x2A). The three least significant bits of the ID mask, bits 2 to 4 of Mask register 2 (0x2D), are ‘don’t care’. This means that any of eight different identifiers will be recognized as valid in the received WUF (from 0x1A0 to 0x1A7).

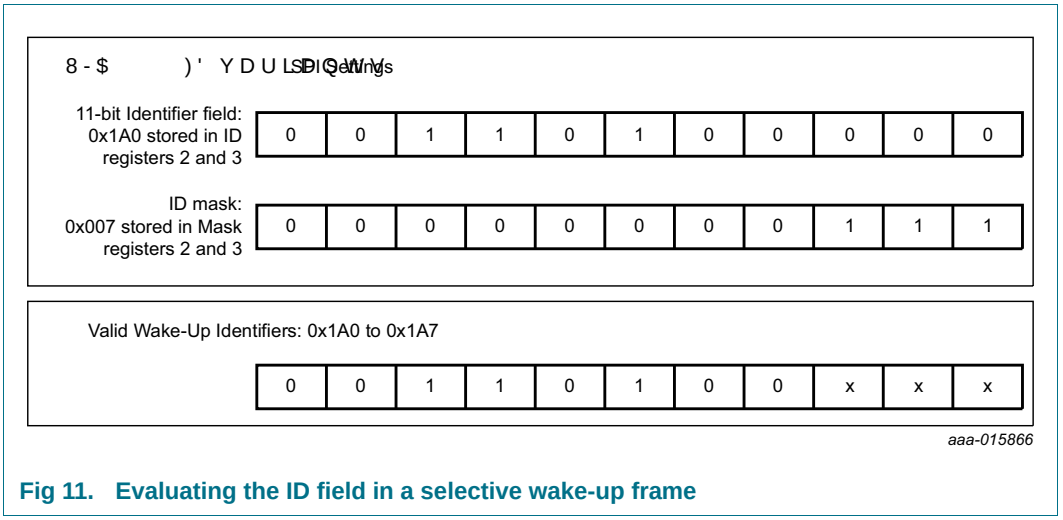

Fig 11. Evaluating the ID field in a selective wake-up frame

The data field indicates the nodes to be woken up. Within the data field, groups of nodes can be predefined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

The data length code (bits DLC in the Frame control register; Table 20) determines the number of data bytes (between 0 and 8) expected in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC ≥ 0000), at least one bit in the data

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field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see Table 21) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined). If DLC = 0, a data field is not expected.

In the example illustrated in Figure 12, the data field consists of a single byte (DLC = 1). This means that the data field in the incoming wake-up frame is evaluated against data mask 7 (stored at address 6Fh; see Table 21 and Figure 13). Data mask 7 is defined as 10101000 in the example, indicating that the node is assigned to three groups (Group1, Group 3 and Group 5).

The received message shown in Figure 12 could, potentially, wake up four groups of nodes: groups 2, 3, 4 and 5. Two matches are found (groups 3 and 5) when the message data bits are compared with the configured data mask (DM7).

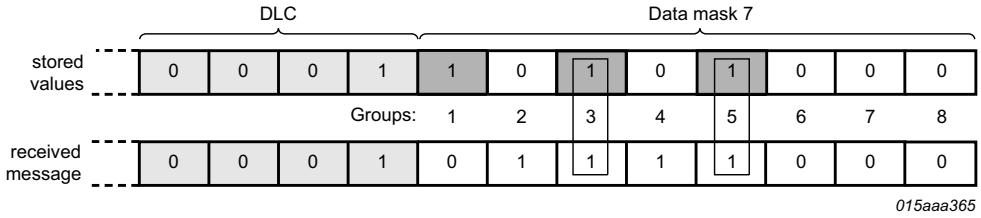

Fig 12. Evaluating the Data field in a selective wake-up frame

Optionally, the data length code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0, only the identifier field is evaluated to determine if the frame contains a valid wake-up message. If PNDM = 1 (the default value), the data field is included for wake-up filtering.

When PNDM = 0, a valid wake-up message is detected and a wake-up event is captured (and CW is set to 1) when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

When PNDM = 1, a valid wake-up message is detected when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the frame is not a Remote frame AND
- the data length code in the received message matches the configured data length code (bits DLC) AND
- if the data length code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated data mask register is also set AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

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If the UJA1169 receives a CAN message containing errors (e.g. a ‘stuffing’ error) that are transmitted in advance of the ACK field, an internal error counter is incremented. If a CAN message is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next Start of Frame (SOF) is ignored by the partial networking module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDE = 1) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

Partial networking is assumed to be configured correctly when PNCOK is set to 1 by the application software. The UJA1169 clears PNCOK after a write access to any of the CAN partial networking configuration registers (see Section 7.8.3).

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), and the CAN transceiver is in Offline mode with wake-up enabled (CWE = 1), then any valid wake-up pattern according to ISO 11898-2:201x (upcoming merged ISO 11898-2/5/6 standard) will trigger a wake-up event.

If the CAN transceiver is not in Offline mode (CMC z00) or CAN wake-up is disabled (CWE = 0), all wake-up patterns on the bus are ignored.

7.8.2 CAN FD frames

CAN FD stands for ‘CAN with Flexible Data-Rate’. It is based on the CAN protocol as specified in the upcoming ISO 11898-1:201x standard.

CAN FD is being gradually introduced into automotive market. In time, all CAN controllers will be required to comply with the new standard (enabling ‘FD-active’ nodes) or at least to tolerate CAN FD communication (enabling ‘FD-passive’ nodes). The UJA1169TK/F, UJA1169TK/F/3 and UJA1169TK/X/F support FD-passive features by means of a dedicated implementation of the partial networking protocol.

The /F variants can be configured to recognize CAN FD frames as valid CAN frames. When CFDC = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The UJA1169xx/F remains in low-power mode (CAN FD-passive) with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the UJA1169xx/F ignores further bus signals until idle is again detected.

CAN FD frames are interpreted as frames with errors by the partial networking module when CFDC = 0. So the error counter is incremented when a CAN FD frame is received. If the ratio of CAN FD frames to valid CAN frames exceeds the threshold that triggers error counter overflow, bit PNFDE is set to 1 and the device wakes up.

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7.8.3 CAN partial networking configuration registers

Dedicated registers are provided for configuring CAN partial networking.

7.8.3.1 Data rate register (0x26)

Table 17. Data rate register (address 26h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	CDR	R/W		CAN data rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100	reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

7.8.3.2 ID registers (0x27 to 0x2A)

Table 18. ID registers 0 to 3 (addresses 27h to 2Ah)

Addr.	Bit	Symbol	Access	Value	Description
27h	7:0	ID07:ID00	R/W	-	bits ID07 to ID00 of the extended frame format
28h	7:0	ID15:ID08	R/W	-	bits ID15 to ID08 of the extended frame format
29h	7:2	ID23:ID18	R/W	-	bits ID23 to ID18 of the extended frame format bits ID05 to ID00 of the standard frame format
	1:0	ID17:ID16	R/W	-	bits ID17 to ID16 of the extended frame format
2Ah	7:5	reserved	R	-	
	4:0	ID28:ID24	R/W	-	bits ID28 to ID24 of the extended frame format bits ID10 to ID06 of the standard frame format

7.8.3.3 ID mask registers (0x2B to 0x2E)

Table 19. ID mask registers 0 to 3 (addresses 2Bh to 2Eh)

Addr.	Bit	Symbol	Access	Value	Description
2Bh	7:0	M07:M00	R/W	-	mask bits ID07 to ID00 of the extended frame format
2Ch	7:0	M15:M08	R/W	-	mask bits ID15 to ID08 of the extended frame format
2Dh	7:2	M23:M18	R/W	-	mask bits ID23 to ID18 of the extended frame format mask bits ID05 to ID00 of the standard frame format
	1:0	M17:M16	R/W	-	mask bits ID17 to ID16 of the extended frame format
2Eh	7:5	reserved	R	-	
	4:0	M28:M24	R/W	-	mask bits ID28 to ID24 of the extended frame format mask. bits ID10 to ID06 of the standard frame format

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7.8.3.4 Frame control register (0x2F)

Table 20. Frame control register (address 2Fh)

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	identifier format:
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W	-	partial networking data mask:
			0	data length code and data field are ‘don’t care’ for wake-up
			1	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	
3:0	DLC	R/W		number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	tolerated, 8 bytes expected

7.8.3.5 Data mask registers (0x68 to 0x6F)

Table 21. Data mask registers (addresses 68h to 6Fh)

Addr.	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	R/W	-	data mask 0 configuration
69h	7:0	DM1	R/W	-	data mask 1 configuration
6Ah	7:0	DM2	R/W	-	data mask 2 configuration
6Bh	7:0	DM3	R/W	-	data mask 3 configuration
6Ch	7:0	DM4	R/W	-	data mask 4 configuration
6Dh	7:0	DM5	R/W	-	data mask 5 configuration
6Eh	7:0	DM6	R/W	-	data mask 6 configuration
6Fh	7:0	DM7	R/W	-	data mask 7 configuration

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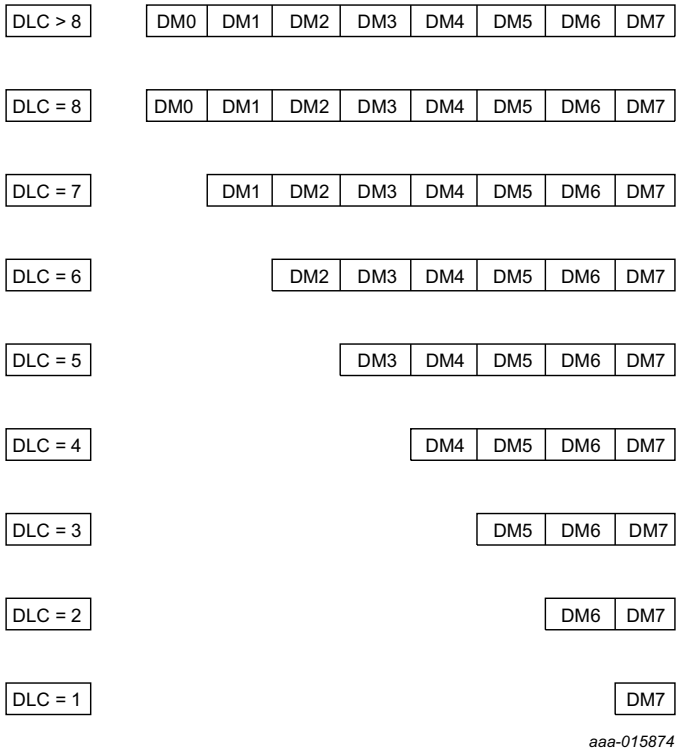

Fig 13. Data mask register usage for different values of DLC

7.9 CAN fail-safe features

7.9.1 TXD dominant time-out

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in CAN Active Mode. The transmitter is disabled if the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), releasing the bus lines to recessive state. The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 4.4 kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure event is captured (CF = 1; see Table 28), if enabled (CFE = 1; see Table 32). In addition, the status of the TXD dominant time-out can be read via the CFS bit in the Transceiver status register (Table 16) and bit CTS is cleared.

7.9.2 Pull-up on TXD pin

Pin TXD has an internal pull-up towards V1 to ensure a safe defined recessive driver state in case the pin is left floating.

7.9.3 V_{CAN} undervoltage event

A CAN failure event is captured (CF = 1), if enabled, when the supply to the CAN transceiver falls below 90 % of its nominal value. In addition, status bit VCS is set to 1.

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7.9.4 Loss of power at pin BAT

When power is lost at pin BAT, the SBC behaves passively towards the CAN-bus pins, disabling the bias circuitry. This ensures that a loss of power at BAT does not affect ongoing communication between nodes on the network.

7.10 Wake-up and interrupt event handling

7.10.1 WAKE pin

Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register (see Table 33). A wake-up event is triggered by a LOW-to-HIGH (if WPRE = 1) and/or a HIGH-to-LOW (if WPFE = 1) transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit. In applications that do not use the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND.

7.10.1.1 WAKE pin status register (0x4B)

Table 22. WAKE pin status register (address 4Bh)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPVS	R		WAKE pin status:
			0	voltage on WAKE pin below switching threshold ($V_{th(sw)}$)
			1	voltage on WAKE pin above switching threshold ($V_{th(sw)}$)
0	reserved	R	-	

While the SBC is in Normal mode, the status of the voltage on pin WAKE can always be read via bit WPVS. Otherwise, WPVS is only valid if local wake-up is enabled (WPRE = 1 and/or WPFE = 1).

7.10.2 Wake-up diagnosis

Wake-up and interrupt event diagnosis in the UJA1169 is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the event status registers (Table 26 to Table 28) and is signaled on pin RXD, if enabled.

A distinction is made between regular wake-up events and interrupt events.

Table 23. Regular events

Symbol	Event	Power-on	Description
CW	CAN wake-up	disabled	see Transceiver event status register (Table 28)
WPR	rising edge on WAKE pin	disabled	see WAKE pin event capture status register (Table 29)
WPF	falling edge on WAKE pin	disabled	

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Table 24. Diagnostic events

Symbol	Event	Power-on	Description
PO	power-on	always enabled	see System event status register (Table 26)
OTW	overtemperature warning	disabled	
SPIF	SPI failure	disabled	
WDF	watchdog failure	always enabled	
V2O[1]	V2 overvoltage	disabled	see Supply event status register (Table 27)
VEXTO[2]	VEXT overvoltage	disabled	
V2U[1]	V2 undervoltage	disabled	
VEXTU[2]	VEXT undervoltage	disabled	
V1U	V1 undervoltage	disabled	
PNFDE[3]	PN frame detection error	always enabled	see Transceiver event status register (Table 28)
CBS	CAN-bus silence	disabled	
CF	CAN failure	disabled	

[1] UJA1169TK, UJA1169TK/3, UJA1169TK/F and UJA1169TK/F/3 only.

[2] UJA1169TK/X and UJA1169TK/X/F only.

[3] UJA1169TK/F, UJA1169TK/F/3 and UJA1169TK/X/F only; otherwise reserved.

PO, WDF and PNFDE interrupts are always enabled and thus captured. Wake-up and interrupt detection can be enabled/disabled for the remaining events individually via the event capture enable registers (Table 30 to Table 32).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in CAN Offline mode with V1 active (SBC Normal or Standby mode), pin RXD is forced LOW to indicate that a wake-up or interrupt event has been detected. If the UJA1169 is in sleep mode when the event occurs, the microcontroller supply, V1, is activated and the SBC switches to Standby mode (via Reset mode).

The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register (Table 25), is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, supply, transceiver or WAKE pin) and then query the relevant event status register (Table 26, Table 27, Table 28 or Table 29 respectively).

After the event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant bit (writing 0 will have no effect). A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits.

Only clear the status bits that were set to 1 when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

7.10.3 Interrupt/wake-up delay

If interrupt or wake-up events occur very frequently while the transceiver is in CAN Offline mode, they can have a significant impact on the software processing time (because pin RXD is repeatedly driven LOW, requiring a response from the microcontroller each time an interrupt/wake-up is generated). The UJA1169 incorporates an event delay timer to limit the disturbance to the software.

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When one of the event capture status bits is cleared, pin RXD is released (HIGH) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after $t_{d(event)}$, pin RXD goes LOW again to alert the microcontroller. In this way, the microcontroller is interrupted once to process a number of events rather than several times to process individual events.

If all events are cleared while the timer is running, RXD remains HIGH after the timer expires, since there are no pending events. The event capture registers can be read at any time.

The event capture delay timer is stopped immediately when pin RSTN goes low (triggered by a HIGH-to-LOW transition on the pin). RSTN is driven LOW when the SBC enters Reset, Sleep, Overtemp and Off modes. A pending event is signaled on pin RXD when the SBC enters Sleep mode.

7.10.4 Sleep mode protection

The wake-up event capture function is critical when the UJA1169 is in Sleep mode, because the SBC only leaves Sleep mode in response to a captured wake-up event. To avoid potential system deadlocks, the SBC distinguishes between regular and diagnostic events (see Section 7.10). Wake-up events (via the CAN-bus or the WAKE pin) are classified as regular events; diagnostic events signal failure/error conditions or state changes. At least one regular wake-up event must be enabled before the UJA1169 can switch to Sleep mode. Any attempt to enter Sleep mode while all regular wake-up events are disabled triggers a system reset.

Another condition that must be satisfied before the UJA1169 can switch to Sleep mode is that all event status bits must be cleared. If an event is pending when the SBC receives a Sleep mode command (MC = 001), it immediately switches to Reset mode. This condition applies to both regular and diagnostic events.

Sleep mode can be permanently disabled in applications where, for safety reasons, the supply voltage to the host controller must never be cut off. Sleep mode is permanently disabled by setting the Sleep control bit (SLPC) in the SBC configuration register (see Table 9) to 1. This register is located in the non-volatile memory area of the device. When SLPC = 1, a Sleep mode SPI command (MC = 001) triggers an SPI failure event instead of a transition to Sleep mode.

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7.10.5 Event status and event capture registers

After an event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant status bit (writing 0 will have no effect).

7.10.5.1 Event status registers (0x60 to 0x64)

Table 25. Global event status register (address 60h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	
3	WPE	R		WAKE pin event:
			0	no pending WAKE pin event
			1	WAKE pin event pending at address 0x64
2	TRXE	R		transceiver event:
			0	no pending transceiver event
			1	transceiver event pendi 14.48 i 0.003sJbC.9(o)-6.(J -0.0014 Tc 16

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Table 26. System event status register (address 61h) *…continued*

Bit	Symbol	Access	Value	Description
0	WDF	R/W		watchdog failure:
			0	no watchdog failure event captured
			1	watchdog overflow in Window or Timeout mode or watchdog triggered too early in Window mode; a system reset is triggered immediately in response to a watchdog failure in Window mode; when the watchdog overflows in Timeout mode, a system reset is only performed if a WDF is already pending (WDF = 1)

Table 27. Supply event status register (address 62h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2	V2O[1]/ VEXTO[2]	R/W		V2/VEXT overvoltage:
			0	no V2/VEXT overvoltage event captured
			1	V2/VEXT overvoltage event captured
1	V2U[1]/ VEXTU[2]	R/W		V2/VEXT undervoltage:
			0	no V2/VEXT undervoltage event captured
			1	V2/VEXT undervoltage event captured
0	V1U	R/W		V1 undervoltage:
			0	no V1 undervoltage event captured
			1	voltage on V1 has dropped below the 90 % undervoltage threshold while V1 is active (event is not captured in Sleep mode because V1 is off); V1U event capture is independent of the setting of bits V1RTC

[1] UJA1169TK, UJA1169TK/3, UJA1169TK/F and UJA1169TK/F/3 only.

[2] UJA1169TK/X and UJA1169TK/X/F only.

Table 28. Transceiver event status register (address 63h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5	PNFDE	R/W		partial networking frame detection error:
			0	no partial networking frame detection error detected
			1	partial networking frame detection error detected
4	CBS	R/W		CAN-bus status:
			0	CAN-bus active
			1	no activity on CAN-bus for $t_{to(silence)}$ (detected only when CBSE = 1 while bus active)
3:2	reserved	R	-	

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Table 28. Transceiver event status register (address 63h) *...continued*

Bit	Symbol	Access	Value	Description
1	CF	R/W		CAN failure:
			0	no CAN failure detected
			1	CAN transceiver deactivated due to V_{CAN} undervoltage OR dominant clamped TXD (not in Sleep mode)
0	CW	R/W		CAN wake-up:
			0	no CAN wake-up event detected
			1	CAN wake-up event detected while the transceiver is in CAN Offline Mode

Table 29. WAKE pin event status register (address 64h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPR	R/W		WAKE pin rising edge:
			0	no rising edge detected on WAKE pin
			1	rising edge detected on WAKE pin
0	WPF	R/W		WAKE pin falling edge:
			0	no falling edge detected on WAKE pin
			1	falling edge detected on WAKE pin

7.10.5.2 Event capture enable registers (0x04, 0x1C, 0x23, 0x4C)

Table 30. System event capture enable register (address 04h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2	OTWE	R/W		overtemperature warning enable:
			0	overtemperature warning disabled
			1	overtemperature warning enabled
1	SPIFE	R/W		SPI failure enable:
			0	SPI failure detection disabled
			1	SPI failure detection enabled
0	reserved	R	-	

Table 31. Supply event capture enable register (address 1Ch)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2	V2OE[1]/ VEXTOE[2]	R/W		V2/VEXT overvoltage enable:
			0	V2/VEXT overvoltage detection disabled
			1	V2/VEXT overvoltage detection enabled
1	V2UE[1]/ VEXTUE[2]	R/W		V2/VEXT undervoltage enable:
			0	V2/VEXT undervoltage detection disabled
			1	V2/VEXT undervoltage detection enabled

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Table 31. Supply event capture enable register (address 1Ch) *…continued*

Bit	Symbol	Access	Value	Description
0	V1UE	R/W		V1 undervoltage enable:
			0	V1 undervoltage detection disabled
			1	V1 undervoltage detection enabled

[1] UJA1169TK, UJA1169TK/3, UJA1169TK/F and UJA1169TK/F/3 only.

[2] UJA1169TK/X and UJA1169TK/X/F only.

Table 32. Transceiver event capture enable register (address 23h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	CBSE	R/W		CAN-bus silence enable:
			0	CAN-bus silence detection disabled
			1	CAN-bus silence detection enabled
3:2	reserved	R	-	
1	CFE	R/W		CAN failure enable:
			0	CAN failure detection disabled
			1	CAN failure detection enabled
0	CWE	R/W		CAN wake-up enable:
			0	CAN wake-up detection disabled
			1	CAN wake-up detection enabled

Table 33. WAKE pin event capture enable register (address 4Ch)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPRE	R/W		WAKE pin rising-edge enable:
			0	rising-edge detection on WAKE pin disabled
			1	rising-edge detection on WAKE pin enabled
0	WPFE	R/W		WAKE pin falling-edge enable:
			0	falling-edge detection on WAKE pin disabled
			1	falling-edge detection on WAKE pin enabled

7.11 Non-volatile SBC configuration

The UJA1169 contains Multiple Time Programmable Non-Volatile (MTPNV) memory cells that allow some of the default device settings to be reconfigured. The MTPNV memory address range is from 0x73 to 0x74. For details, see Table 9 and Table 11.

7.11.1 Programming MTPNV cells

NXP delivers the UJA1169 in so-called ‘Forced Normal’ mode, also referred to as the ‘factory preset’ configuration. In order to change the default settings, the device must be in Forced Normal mode with FNMC = 1 and NVMPS = 1. In Forced Normal mode, the watchdog is disabled, all regulators are on and the CAN transceiver is in Active mode.

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If the device has been programmed previously, the factory presets may need to be restored before reprogramming can begin (see Section 7.11.2). When the factory presets have been restored successfully, a system reset is generated automatically and UJA1169 switches back to Forced Normal mode.

Programming of the non-volatile memory (NVM) registers is performed in two steps. First, the required values are written to addresses 0x73 and 0x74. In the second step, reprogramming is confirmed by writing the correct CRC value to the MTPNV CRC control register (see Section 7.11.1.2). The SBC starts reprogramming the MTPNV cells as soon as the CRC value has been validated. If the CRC value is not correct, reprogramming is aborted. On completion, a system reset is generated to indicate that the MTPNV cells have been reprogrammed successfully. Note that the MTPNV cells cannot be read while they are being reprogrammed.

After an MTPNV programming cycle has been completed, the NVM is protected from being overwritten.

The MTPNV cells can be reprogrammed a maximum of 200 times ($N_{cy(W)MTP}$; see Table 52). Bit NVMPS in the MTPNV status register (Table 34) indicates whether the non-volatile cells can be reprogrammed. This register also contains a write counter, WRCNTS, that is incremented each time the MTPNV cells are reprogrammed (up to a maximum value of 111111; there is no overflow; performing a factory reset also increments the counter). This counter is provided for information purposes only; reprogramming will not be rejected when it reaches its maximum value.

An error correction code status bit, ECCS, is set to indicate the CRC check mechanism in the SBC has detected and corrected a single bit failure in non-volatile memory. If more than one bit failure is detected, the SBC will not restart after MTPNV reprogramming. Check the ECCS flag at the end of the production cycle to verify the content of non-volatile memory. When this flag is set, it indicates a device or ECU failure.

7.11.1.1 MTPNV status register (0x70)

Table 34. MTPNV status register (address 70h)

Bit	Symbol	Access	Value	Description
7:2	WRCNTS	R		write counter status:
			xxxxxx	contains the number of times the MTPNV cells were reprogrammed
1	ECCS	R/W		error correction code status:
			0	no bit failure detected in non-volatile memory
			1	bit failure detected and corrected in non-volatile memory
0	NVMPS	R/W		non-volatile memory programming status:
			0	MTPNV memory cannot be overwritten
			1[1]	MTPNV memory is ready to be reprogrammed

[1] Factory preset value.

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7.11.1.2 MTPNV CRC control register (0x75)

The cyclic redundancy check value stored in bits CRCC in the MTPNV CRC control register is calculated using the data written to registers 0x73 and 0x74.

Table 35. MTPNV CRC control register (address 75h)

Bit	Symbol	Access	Value	Description
7:0	CRCC	R/W		cyclic redundancy check control:
			-	CRC control data

The CRC value is calculated using the data representation shown in Figure 14 and the modulo-2 division with the generator polynomial: $X^8 + X^5 + X^3 + X^2 + X + 1$. The result of this operation must be bitwise inverted.

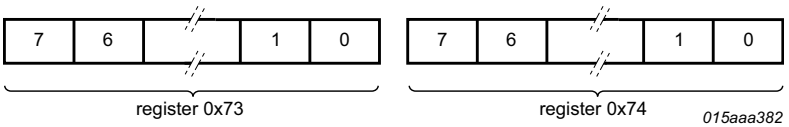

Fig 14. Data representation for CRC calculation

The following parameters can be used to calculate the CRC value (e.g. via the Autosar method):

Table 36. Parameters for CRC coding

Parameter	Value
CRC result width	8 bits
Polynomial	0x2F
Initial value	0xFF
Input data reflected	no
Result data reflected	no
XOR value	0xFF

Alternatively, the following algorithm can be used:

```
data = 0   // unsigned byte
crc = 0xFF
for i = 0 to 1
     data = content_of_address(0x73 + i) EXOR crc
     for j = 0 to 7
          if data t 128
               data = data * 2  // shift left by 1
               data = data EXOR 0x2F
          else
               data = data * 2 // shift left by 1
     next j
     crc = data
next i
crc = crc EXOR 0xFF
```


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