

IRFB4620PbF

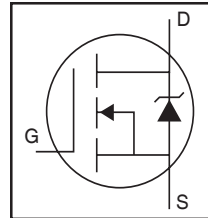
HEXFET® Power MOSFET

Applications

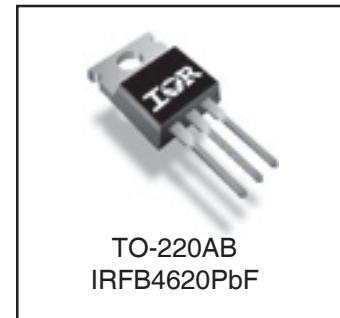
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



V_{DSS}		200V
$R_{DS(on)}$	typ.	60mΩ
	max.	72.5mΩ
I_D		25A



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	25	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	18	
I_{DM}	Pulsed Drain Current ①	100	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	144	W
	Linear Derating Factor	0.96	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	54	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	113	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ④		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	1.045	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50		
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦⑧	—	62	

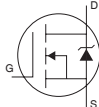
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.23	—	V/°C	Reference to 25°C, I _D = 5mA①
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	60	72.5	mΩ	V _{GS} = 10V, I _D = 15A ④
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 100μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 200V, V _{GS} = 0V
		—	—	250		V _{DS} = 200V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
R _{G(int)}	Internal Gate Resistance	—	2.6	—	Ω	

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	37	—	—	S	V _{DS} = 50V, I _D = 15A
Q _g	Total Gate Charge	—	25	38	nC	I _D = 15A
Q _{gs}	Gate-to-Source Charge	—	8.2	—		V _{DS} = 100V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	7.9	—		V _{GS} = 10V ④
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	17	—		I _D = 15A, V _{DS} = 0V, V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	13.4	—	ns	V _{DD} = 130V
t _r	Rise Time	—	22.4	—		I _D = 15A
t _{d(off)}	Turn-Off Delay Time	—	25.4	—		R _G = 7.3Ω
t _f	Fall Time	—	14.8	—		V _{GS} = 10V ④
C _{iss}	Input Capacitance	—	1710	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	125	—		V _{DS} = 50V
C _{rss}	Reverse Transfer Capacitance	—	30	—		f = 1.0MHz (See Fig.5)
C _{oss} eff. (ER)	Effective Output Capacitance (Energy Related)⑥	—	113	—		V _{GS} = 0V, V _{DS} = 0V to 160V ⑥(See Fig.11)
C _{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑤	—	317	—		V _{GS} = 0V, V _{DS} = 0V to 160V ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	25	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	100		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 15A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	78	—	ns	T _J = 25°C V _R = 100V,
		—	99	—		T _J = 125°C I _F = 15A
Q _{rr}	Reverse Recovery Charge	—	294	—	nC	T _J = 25°C di/dt = 100A/μs ④
		—	432	—		T _J = 125°C
I _{RRM}	Reverse Recovery Current	—	7.6	—	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 1.0mH
R_G = 25Ω, I_{AS} = 15A, V_{GS} = 10V. Part not recommended for use above this value .
- ③ I_{SD} ≤ 15A, di/dt ≤ 634A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

- ⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_θ is measured at T_J approximately 90°C

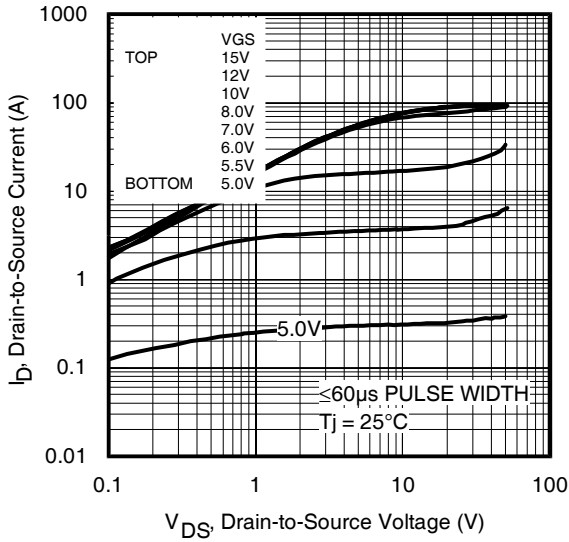


Fig 1. Typical Output Characteristics

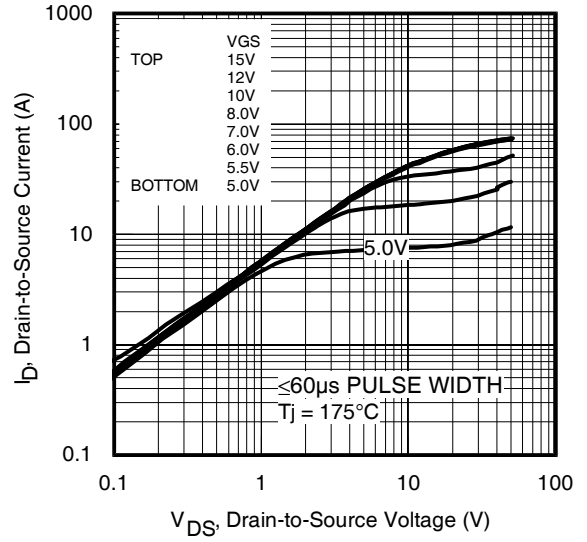


Fig 2. Typical Output Characteristics

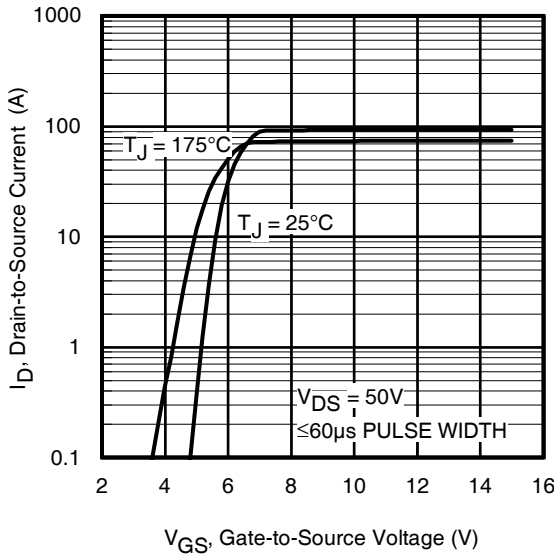


Fig 3. Typical Transfer Characteristics

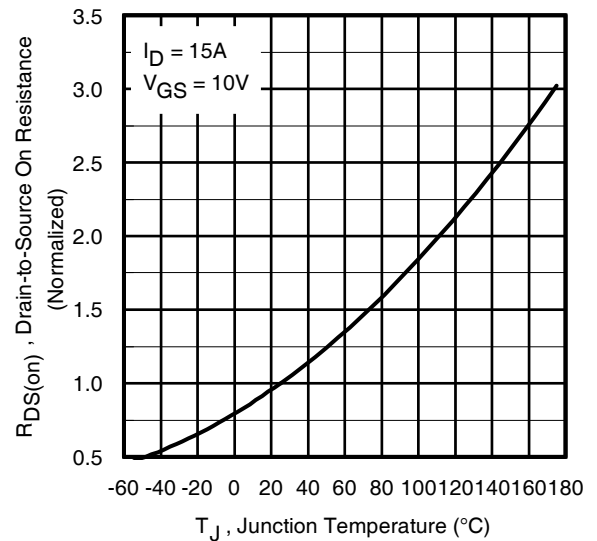


Fig 4. Normalized On-Resistance vs. Temperature

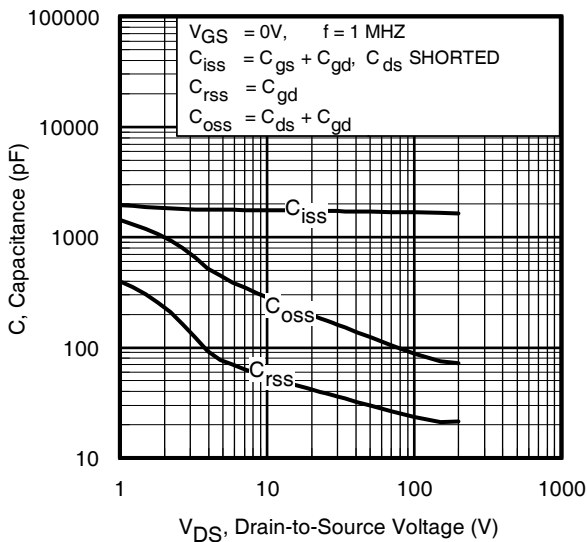


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

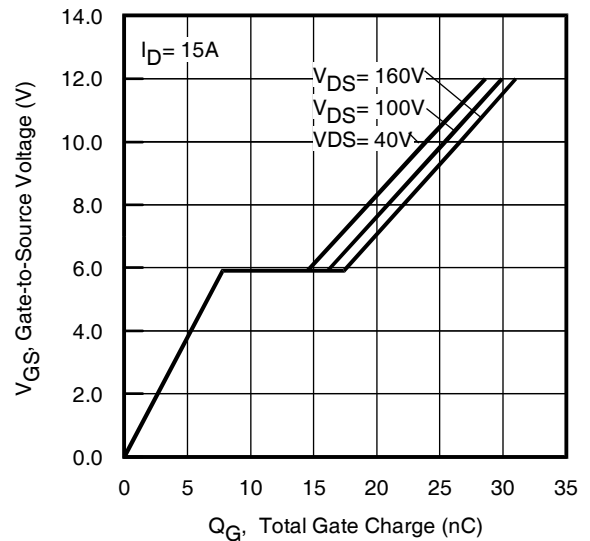


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

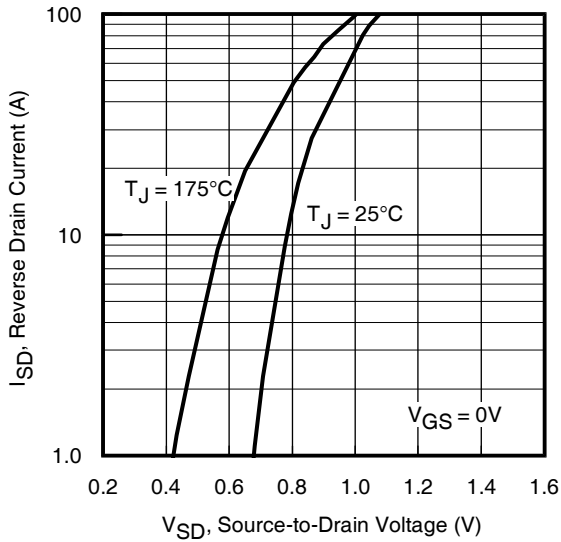


Fig 7. Typical Source-Drain Diode Forward Voltage

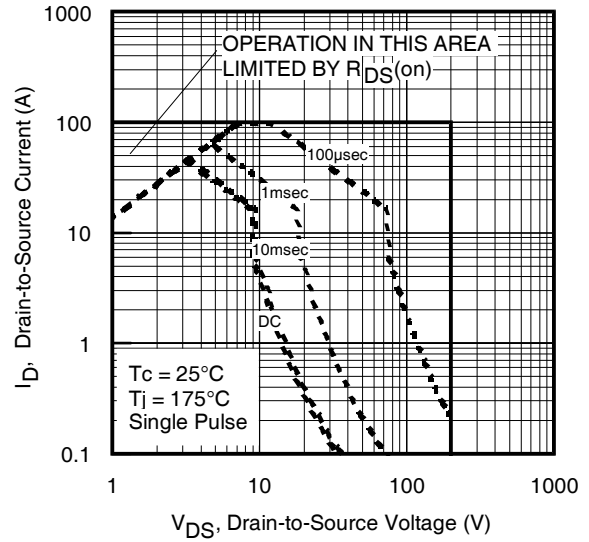


Fig 8. Maximum Safe Operating Area

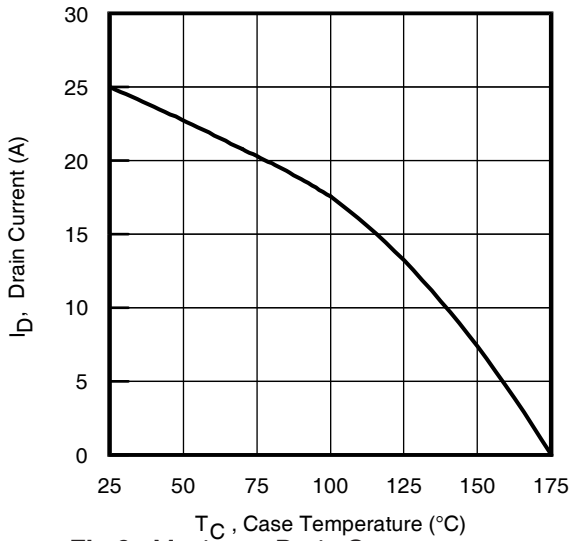


Fig 9. Maximum Drain Current vs. Case Temperature

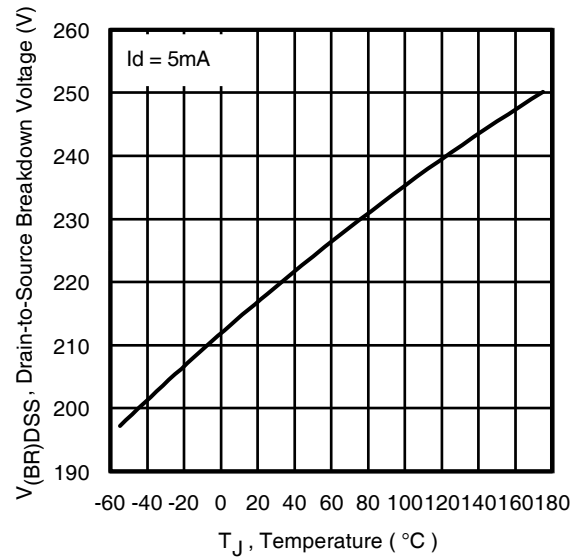


Fig 10. Drain-to-Source Breakdown Voltage

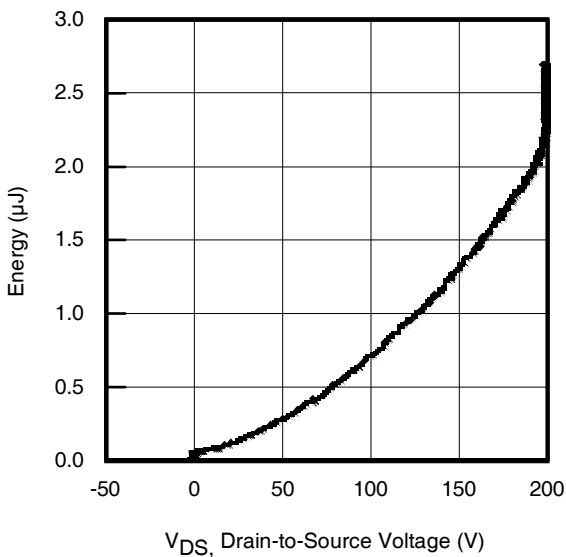


Fig 11. Typical C_{OSS} Stored Energy

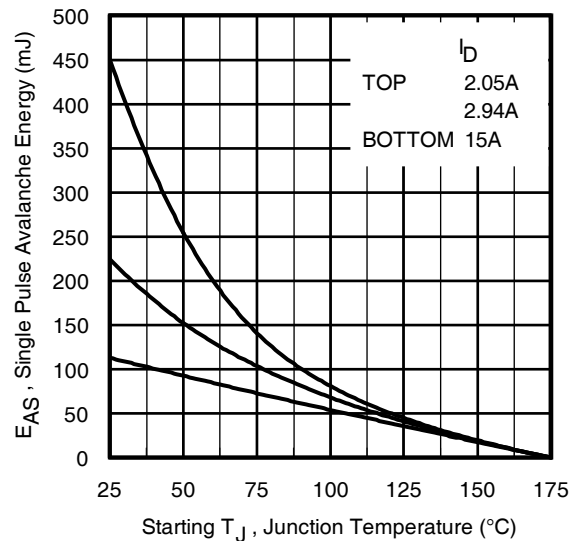


Fig 12. Maximum Avalanche Energy vs. Drain Current

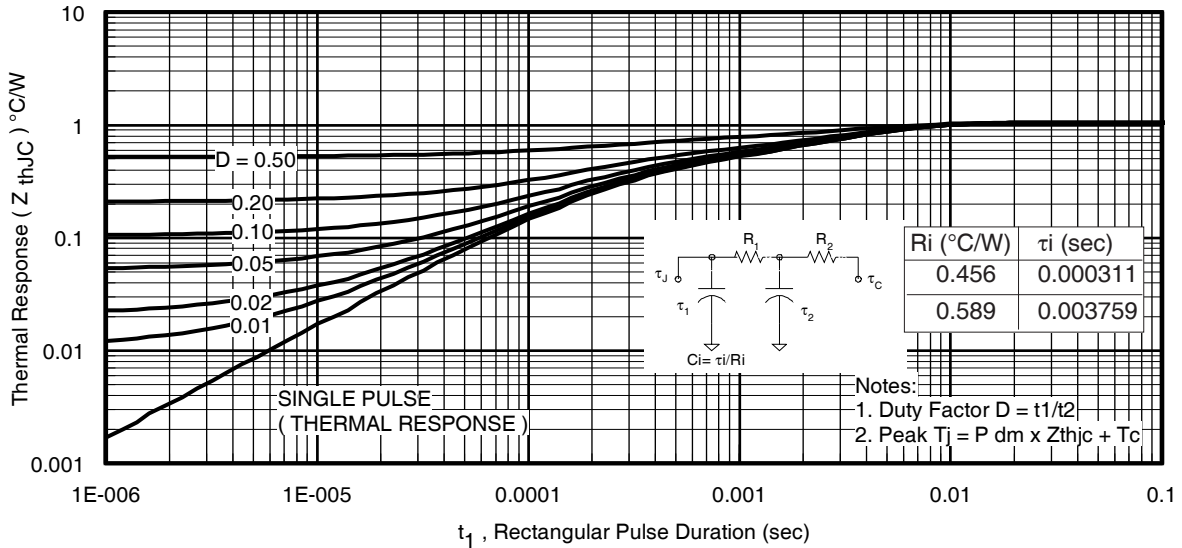


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

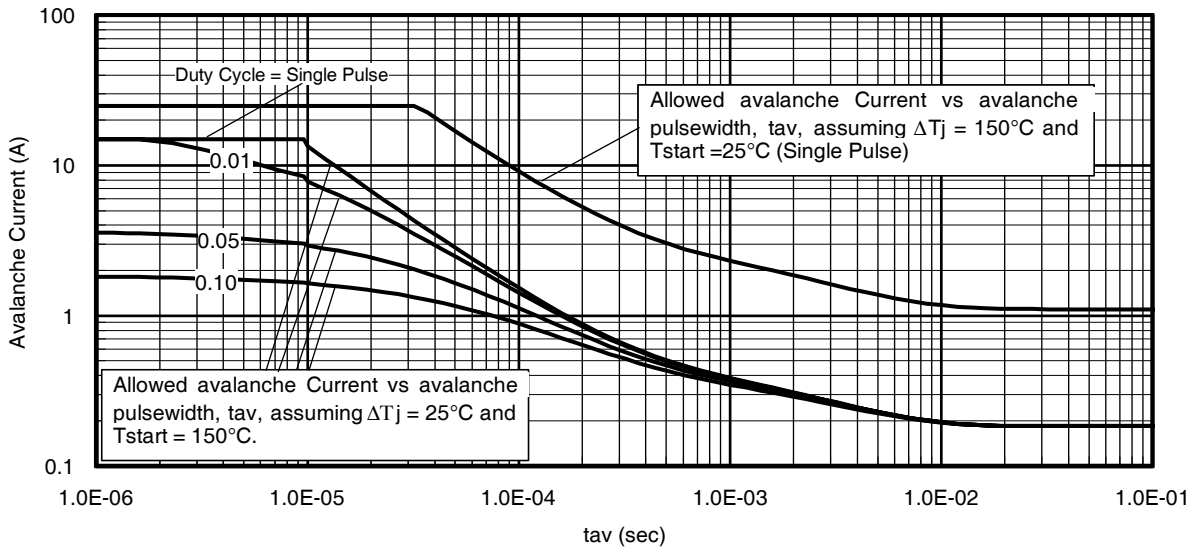
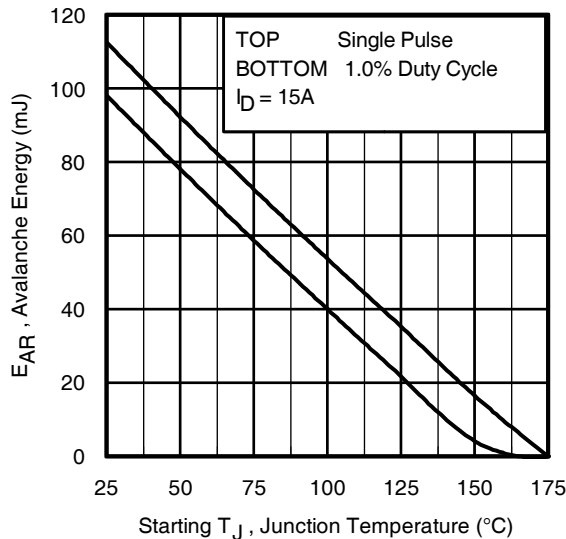


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

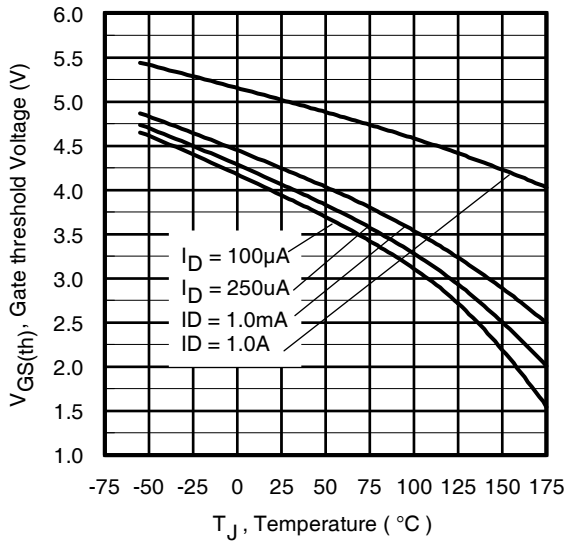


Fig 16. Threshold Voltage vs. Temperature

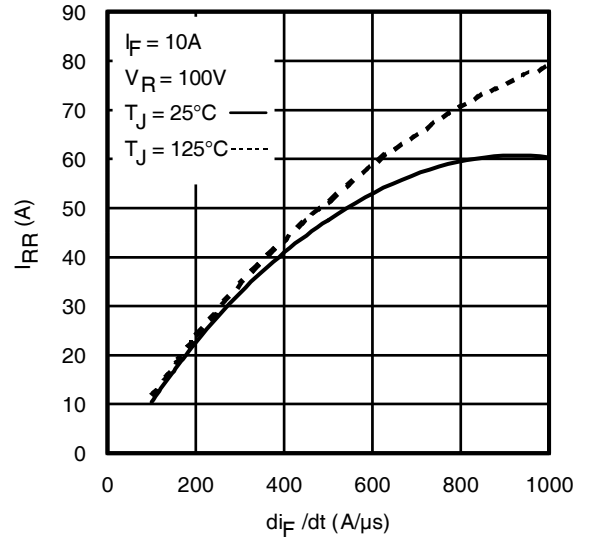


Fig. 17 - Typical Recovery Current vs. di_F/dt

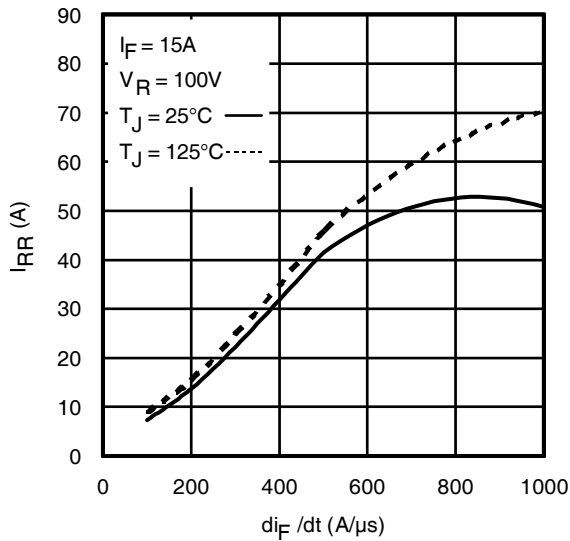


Fig. 18 - Typical Recovery Current vs. di_F/dt

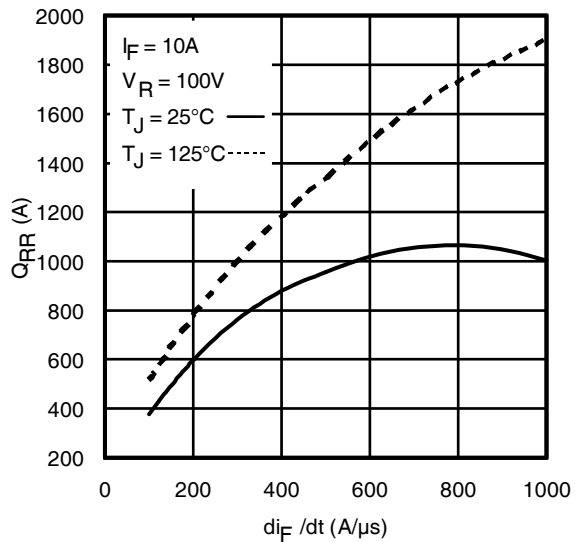


Fig. 19 - Typical Stored Charge vs. di_F/dt

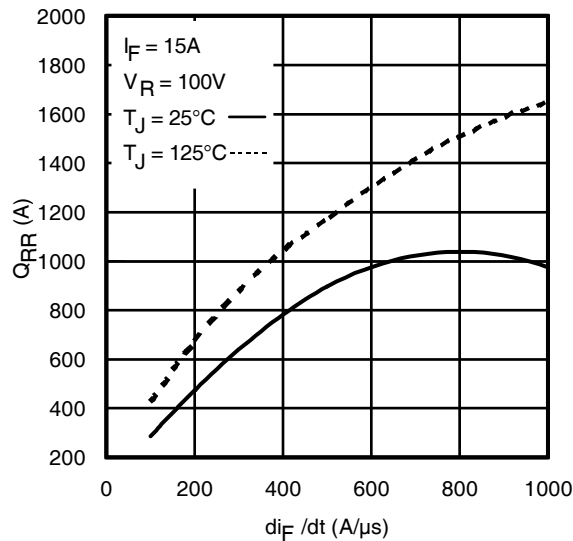


Fig. 20 - Typical Stored Charge vs. di_F/dt



Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



* $V_{GS} = 5V$ for Logic Level Devices



Fig 22a. Unclamped Inductive Test Circuit



Fig 22b. Unclamped Inductive Waveforms

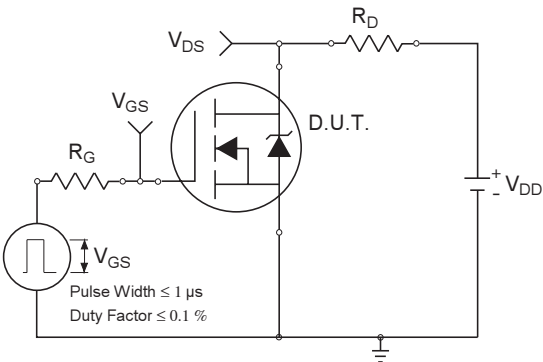


Fig 23a. Switching Time Test Circuit



Fig 23b. Switching Time Waveforms

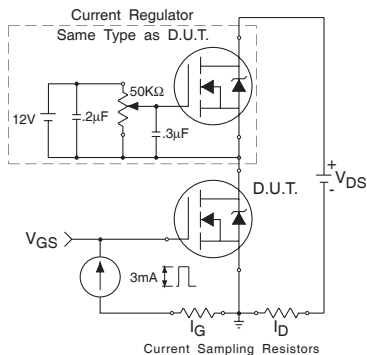


Fig 24a. Gate Charge Test Circuit

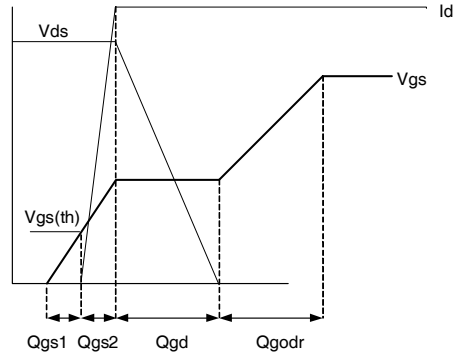
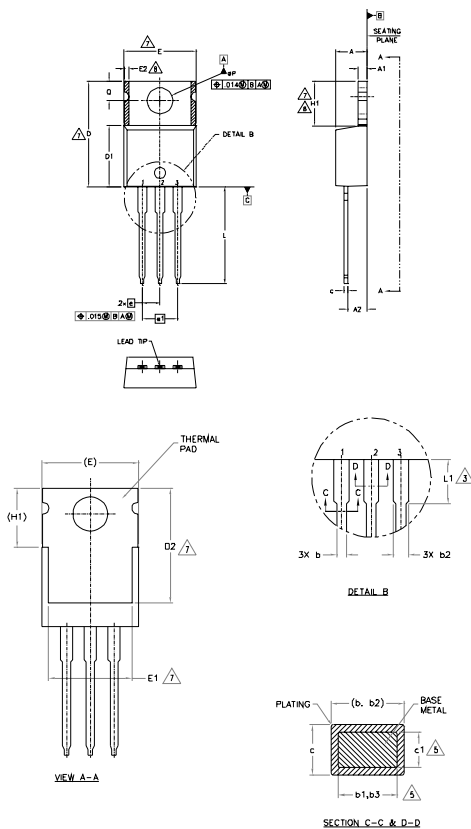


Fig 24b. Gate Charge Waveform

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
 - 2.- DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS).
 - 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
 - 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
 - 6.- CONTROLLING DIMENSION : INCHES.
 - 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
 - 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
 - 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max) AND D2 (min) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

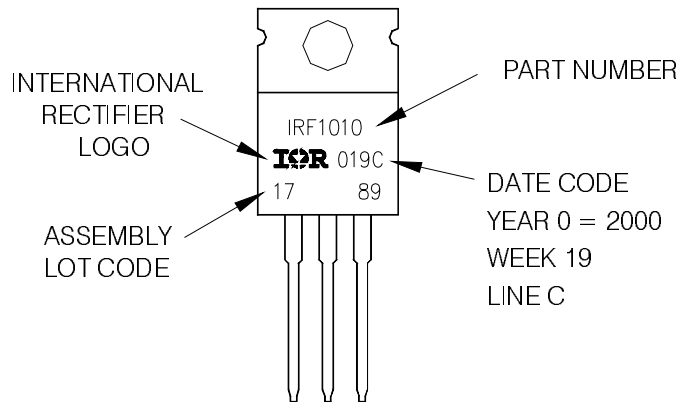
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	5
b1	0.38	0.97	.015	.038	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		100 BSC		
e1	5.08 BSC		200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
ØP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

- LEAD ASSIGNMENTS
- HEBECT
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
- SEM. G-PACK
- 1.- GATE
 - 2.- COLLECTOR
 - 3.- EMITTER
- DIODES
- 1.- ANODE
 - 2.- CATHODE
 - 3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 2000
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.