CY2544
CY2546
CY2548

Quad-PLL Programmable Clock Generator with Spread Spectrum

Features

- Four fully integrated phase locked loops (PLLs)
- Input frequency range
  - External crystal: 8 to 48 MHz for CY2544 and CY2546
  - External reference: 8 to 166 MHz clock
- Reference clock input voltage range
  - 2.5 V, 3.0 V, and 3.3 V for CY2548
  - 1.8 V for CY2544 and CY2546
- Wide operating output frequency range
  - 3 to 166 MHz
- Programmable spread spectrum with center and down spread option and Lexmark and Linear modulation profiles
- VDD supply voltage options:
  - 2.5 V, 3.0 V, and 3.3 V for CY2544 and CY2548
  - 1.8 V for CY2546
- Selectable output clock voltages:
  - 2.5 V, 3.0 V, and 3.3 V for CY2544 and CY2548
  - 1.8 V for CY2546
- Frequency select feature with option to select eight different frequencies over nine clock outputs
- Power down, output enable, and SS ON/OFF controls
- Low jitter, high accuracy outputs
- Ability to synthesize nonstandard frequencies with Fractional-N capability
- Up to nine clock outputs with programmable drive strength
- Glitch free outputs while frequency switching
- 24-pin QFN package
- Commercial and Industrial temperature ranges

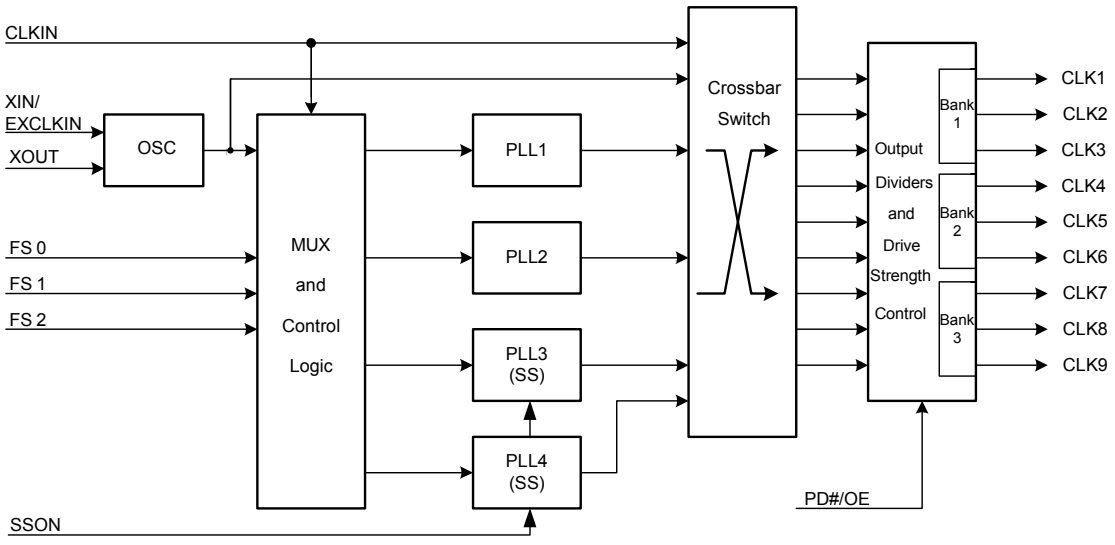
Benefits

- Multiple high performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for personalization of PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Application specific programmable EMI reduction using spread spectrum for clocks
- Programmable PLLs for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitability for PC, consumer, portable, and networking applications
- Capable of Zero PPM frequency synthesis error
- Uninterrupted system operation during clock frequency switch
- Application compatibility in standard and low power systems

Functional Description

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

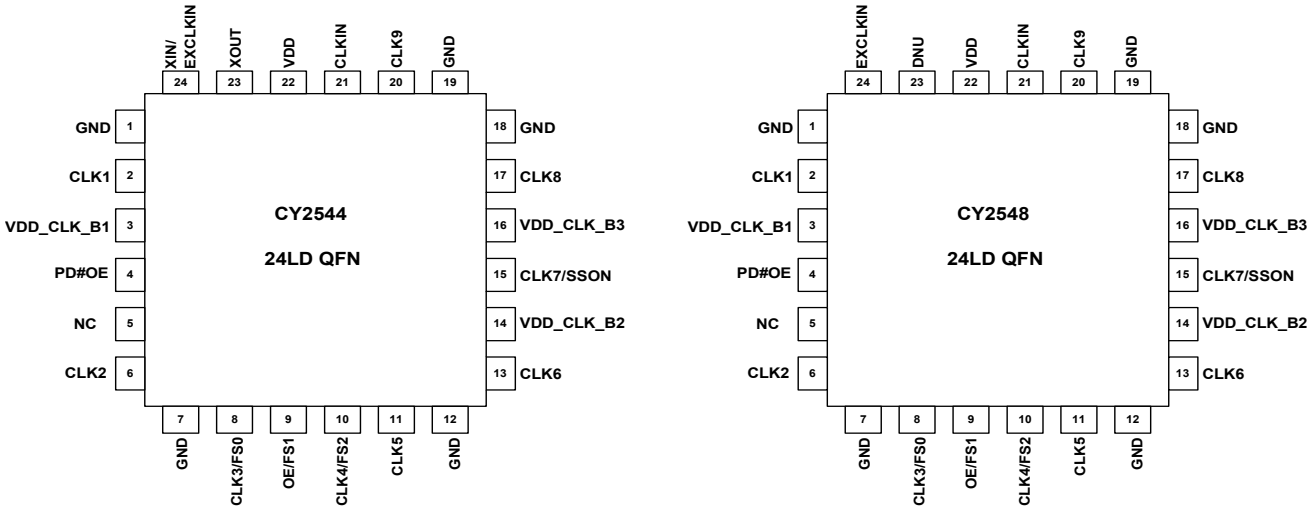
Device Selection Guide

Device	Crystal Input	EXCKLKIN Input	CLKIN Input	VDD	VDD_CLK_BX
CY2544	Yes	1.8 V LVCMOS	2.5 V, 3.0 V, 3.3 V LVCMOS	2.5 V, 3.0 V, 3.3 V	2.5 V, 3.0 V, 3.3 V
CY2546	Yes	1.8 V LVCMOS	1.8 V LVCMOS	1.8 V	1.8 V
CY2548	No	2.5 V, 3.0 V, 3.3 V LVCMOS	2.5 V, 3.0 V, 3.3 V LVCMOS	2.5 V, 3.0 V, 3.3 V	2.5 V, 3.0 V, 3.3 V

Pinout

Figure 1. 24-pin QFN pinout

CY2544 / CY2548



Pin Definitions

CY2544/CY2548 (VDD = 2.5 V, 3.0 V or 3.3 V Supply)

Pin Number	Name	I/O	Description
1	GND	Power	**Power supply ground**
2	CLK1	Output	**Programmable clock output.** Output voltage depends on VDD_CLK_B1 voltage
3	VDD_CLK_B1	Power	**Power supply for bank1, (CLK1, CLK2, CLK3) Outputs:** 2.5 V/3.0 V/3.3 V
4	PD#/OE	Input	**Multifunction programmable pin.** Output enable or power-down mode
5	NC	NC	**No Connect**
6	CLK2	Output	**Programmable Clock Output.** Output voltage depends on VDD_CLK_B1 voltage
7	GND	Power	**Power supply ground**
8	CLK3/FS0	Output/input	**Multifunction programmable pin.** Programmable clock output clock or frequency select pin. Output voltage of CLK3 depends on VDD_CLK_B1 voltage
9	OE/FS1	Input	**Multifunction programmable pin.** Output enable or frequency select pin
10	CLK4/FS2	Output/input	**Multifunction programmable pin.** Programmable clock output or frequency select input pin. Output voltage of CLK4 depends on VDD_CLK_B2 voltage

Pin Definitions (continued)

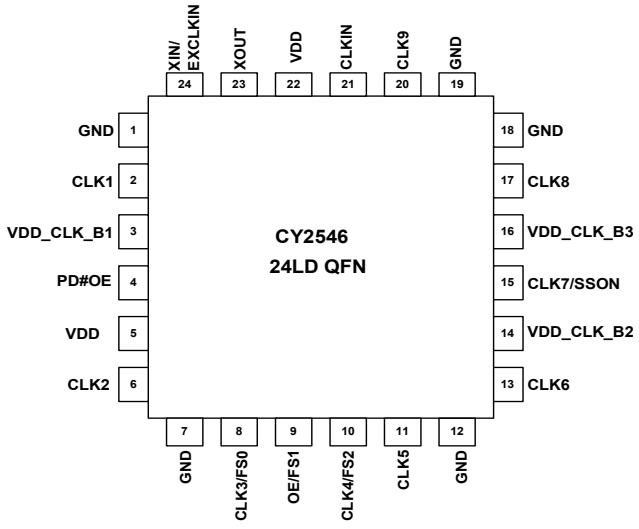
CY2544/CY2548 (VDD = 2.5 V, 3.0 V or 3.3 V Supply)

Pin Number	Name	I/O	Description
11	CLK5	Output	**Programmable clock output.** Output voltage depends on VDD_CLK_B2 voltage
12	GND	Power	**Power supply ground**
13	CLK6	Output	**Programmable clock output.** Output voltage depends on VDD_CLK_B2 voltage
14	VDD_CLK_B2	Power	**Power supply for bank2, (CLK4, CLK5, CLK6) Outputs.** 2.5 V/3.0 V/3.3 V
15	CLK7/SSON	Output/input	**Multifunction programmable pin.** Programmable clock output or spread spectrum ON/OFF control input pin. Output voltage of CLK7 depends on Bank3 voltage
16	VDD_CLK_B3	Power	**Power supply for bank3, (CLK7, CLK8, CLK9) Outputs.** 2.5 V/3.0 V/3.3 V
17	CLK8	Output	**Programmable output clock.** Output voltage depends on Bank3 voltage
18	GND	Power	**Power supply ground**
19	GND	Power	**Power supply ground**
20	CLK9	Output	**Programmable clock output.** Output voltage depends on VDD_CLK_B3 voltage
21	CLKIN	Input	**2.5 V/3.0 V/3.3 V reference clock input.** The signal level of CLKIN input must track VDD power supply on pin 22.
22	VDD	Power	**Power supply.** 2.5 V/3.0 V/3.3 V
23	XOUT	Output	**Crystal output for CY2544**
	DNU	Output	**Do not use this pin for CY2548**
24	XIN/EXCLKIN	Input	**Crystal input or 1.8 V external clock input for CY2544**
	EXCLKIN	Input	**2.5 V/3.0 V/3.3 V external clock input for CY2548**

Pinout

Figure 2. 24-pin QFN pinout

CY2546



Pin Definitions

CY2546 (VDD = 1.8 V Supply)

Pin Number	Name	I/O	Description
1	GND	Power	**Power supply ground**
2	CLK1	Output	**Programmable clock output.** Output voltage depends on VDD_CLK_B1 voltage
3	VDD_CLK_B1	Power	**Power supply for bank1, (CLK1, CLK2, CLK3) Outputs.** 1.8 V
4	PD#/OE	Input	**Multifunction programmable pin.** Output enable or power down mode
5	VDD	Power	**Power supply.** 1.8 V
6	CLK2	Output	**Programmable clock output.** Output voltage depends on VDD_CLK_B1 voltage
7	GND	Power	**Power supply ground**
8	CLK3/FS0	Output/Input	**Multifunction programmable pin.** Programmable clock output or frequency select input pin. Output voltage of CLK3 depends on VDD_CLK_B1 voltage
9	OE/FS1	Input	**Multifunction programmable pin.** Output enable or frequency select pin
10	CLK4/FS2	Output/Input	**Multifunction programmable pin.** Programmable clock output or frequency select input pin. Output voltage of CLK4 depends on VDD_CLK_B2 voltage
11	CLK5	Output	**Programmable clock output.** Output voltage depends on VDD_CLK_B2 voltage
12	GND	Power	**Power supply ground**
13	CLK6	Output	**Programmable clock output.** Output voltage depends on VDD_CLK_B2 voltage
14	VDD_CLK_B2	Power	**Power supply for bank2, (CLK4, CLK5, CLK6) Outputs.** 1.8 V
15	CLK7/SSON	Output/input	**Multifunction programmable pin.** Programmable clock output or spread spectrum ON/OFF control input pin. Output voltage of CLK7 depends on VDD_CLK_B3 voltage
16	VDD_CLK_B3	Power	**Power supply for bank3, (CLK7, CLK8, CLK9) Outputs.** 1.8 V
17	CLK8	Output	**Programmable clock output.** Output voltage depends on VDD_CLK_B3 voltage
18	GND	Power	**Power supply ground**
19	GND	Power	**Power supply ground**
20	CLK9	Output	**Programmable clock output.** Output voltage depends on VDD_CLK_B3 voltage
21	CLKIN	Input	**External 1.8 V low voltage reference clock input**
22	VDD	Power	**Power supply.** 1.8 V
23	XOUT	Output	**Crystal output**
24	XIN/EXCLKIN	Input	**Crystal input or 1.8 V external clock input**

Functional Overview

Four Configurable PLLs

The CY2544, CY2548 and CY2546 have four programmable PLLs that can be used to generate output frequencies ranging from 3 to 166 MHz. The advantage of having four PLLs is that a single device generates up to four independent frequencies from a single crystal.

Input Reference Clocks

The input to the CY2544, CY2548 and CY2546 can be either a crystal or a clock signal. The input frequency range for crystal (XIN) is 8 MHz to 48 MHz and that for external reference clock (EXCLKIN) is 8 MHz to 166 MHz. The voltage range for the reference clock input of CY2548 is 2.5 V/3.0 V/3.3 V while that for CY2544 and CY2546 is 1.8 V. This gives user an option for this device to be compatible for different input clock voltage levels in the system.

There is provision for a secondary reference clock input, CLKIN with applied frequency range of 8 MHz to 166 MHz. When CLKIN signal at pin 21 is used as a reference input to the PLL, a valid signal at EXCLKIN (as specified in the AC and DC Electrical Specification table) must be present for the devices to operate properly.

Multiple Power Supplies

These devices are designed to operate at internal supply voltage of 1.8 V. In the case of the high voltage part (CY2544/CY2548), an internal regulator is used to generate 1.8 V from the 2.5 V/3.0 V/3.3 V VDD supply voltage at pin 22. For the low

voltage part (CY2546), this internal regulator is bypassed and 1.8 V at VDD pin 22 is directly used.

Output Bank Settings

There are nine clock outputs grouped in three output driver banks. The Bank 1, Bank 2, and Bank 3 correspond to (CLK1, CLK2, CLK3), (CLK4, CLK5, CLK6), and (CLK7, CLK8, CLK9) respectively. Separate power supplies are used for each of these banks and they can be any of 2.5 V, 3.0 V, or 3.3 V for CY2544/CY2548 and 1.8 V for CY2546 giving user multiple choice of output clock voltage levels.

Output Source Selection

These devices have programmable input sources for each of its nine clock outputs (CLK1–9). There are six available clock sources for these outputs. These clock sources are: XIN/EXCLKIN, CLKIN, PLL1, PLL2, PLL3, or PLL4. Output clock source selection is done using four out of six crossbar switch. Thus, any one of these six available clock sources can be arbitrarily selected for the clock outputs. This gives user a flexibility to have up to four independent clock outputs.

Spread Spectrum Control

Two of the four PLLs (PLL3 and PLL4) have spread spectrum capability for EMI reduction in the system. The device uses a Cypress proprietary PLL and spread spectrum clock (SSC) technology to synthesize and modulate the frequency of the PLL. The spread spectrum feature can be turned on or off using a multifunction control pin (CLK7/SSON). It can be programmed to either center spread range from ±0.125% to ±2.50% or down spread range from –0.25% to –5.0% with Lexmark or Linear profile.

Frequency Select

There are three multifunction frequency select pins (FS0, FS1 and FS2) that provide an option to select eight different sets of frequencies among each of the four PLLs. Each output has programmable output divider options.

Glitch-Free Frequency Switch

When the frequency select pin (FS) is used to switch frequency, the outputs are glitch-free provided frequency is switched using output dividers. This feature enables uninterrupted system operation while clock frequency is being switched.

PD#/OE Mode

PD#/OE (Pin 4) can be programmed to operate as either power down (PD#) or output enable (OE) mode. PD# is a low-true input. If activated it shuts off the entire chip, resulting in minimum power consumption for the device. Setting this signal high brings the device in the operational mode with default register settings.

When this pin is programmed as Output Enable (OE), clock outputs can be enabled or disabled using OE (pin 4). Individual clock outputs can be programmed to be sensitive to this OE pin.

Output Drive Strength

The DC drive strength of the individual clock output can be programmed for different values. Table 1 shows the typical rise and fall times for different drive strength settings.

Table 1. Output Drive Strength

Output Drive Strength	Rise/Fall Time (ns) (Typical Value)
Low	6.8
Mid Low	3.4
Mid High	2.0
High	1.0

Generic Configuration and Custom Frequency

There is a generic set of output frequencies available from the factory that can be used for the device evaluation purposes. The devices, CY2544, CY2548 and CY2546 can be custom programmed to any desired frequencies and listed features. For customer specific programming, please contact local Cypress Field application engineer (FAE) or sales representative.

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage for CY2544/CY2548		–0.5	4.5	V
V_{DD}	Supply voltage for CY2546		–0.5	2.6	V
$V_{DD\_CLK\_BX}$	Output bank supply voltage		–0.5	4.5	V
V_{IN}	Input voltage for CY2544/CY2548	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
V_{IN}	Input voltage for CY2546	Relative to V_{SS}	–0.5	2.2	V
T_S	Temperature, storage	Non functional	–65	+150	°C
ESD_{HBM}	ESD protection (Human body model)	JEDEC EIA/JESD22-A114-E	2000	–	V
UL-94	Flammability rating	V-0 at 1/8 in.	–	10	ppm
MSL	Moisture sensitivity level		3		

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	VDD Operating voltage for CY2544/CY2548	2.25	–	3.60	V
V_{DD}	VDD Operating voltage for CY2546	1.65	1.8	1.95	V
$V_{DD\_CLK\_BX}$	Output driver voltage for Bank 1, 2 and 3	1.65	–	3.60	V
T_{AC}	Commercial ambient temperature	0	–	+70	°C
T_{AI}	Industrial ambient temperature	–40	--	+85	°C
C_{LOAD}	Maximum load capacitance	–	–	15	pF
t_{PU}	Power up time for all V_{DD} to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL}	Output low voltage	I_{OL} = 2 mA, drive strength = [00]	–	–	0.4	V
		I_{OL} = 3 mA, drive strength = [01]				
		I_{OL} = 7 mA, drive strength = [10]				
		I_{OL} = 12 mA, drive strength = [11]				
V_{OH}	Output high voltage	I_{OH} = –2 mA, drive strength = [00]	$V_{DD\_CLK\_BX}$ – 0.4	–	–	V
		I_{OH} = –3 mA, drive strength = [01]				
		I_{OH} = –7 mA, drive strength = [10]				
		I_{OH} = –12 mA, drive strength = [11]				
V_{IL1}	Input low voltage of PD#/OE, FS0, FS1, FS2 and SSON	–	–	–	0.2 × V_{DD}	V
V_{IL2}	Input low voltage of CLKIN for CY2544/CY2548	–	–	–	0.1 × V_{DD}	V
V_{IL3}	Input low voltage of EXCLKIN for CY2544	–	–	–	0.15	V

DC Electrical Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL4}	Input low voltage of EXCLKIN for CY2548	–	–	–	0.1 × V_{DD}	V
V_{IL5}	Input low voltage of CLKIN, EXCLKIN for CY2546	–	–	–	0.1 × V_{DD}	V
V_{IH1}	Input high voltage of PD#/OE, FS0, FS1, FS2 and SSON	–	0.8 × V_{DD}	–	–	V
V_{IH2}	Input high voltage of CLKIN for CY2544/CY2548	–	0.9 × V_{DD}	–	–	V
V_{IH3}	Input high voltage of EXCLKIN for CY2544	–	1.6	–	2.2	V
V_{IH4}	Input high voltage of EXCLKIN for CY2548	–	0.9 × V_{DD}	–	–	V
V_{IH5}	Input high voltage of CLKIN, EXCLKIN for CY2546	–	0.9 × V_{DD}	–	–	V
I_{IL1}	Input low current of PD#/OE and FS1	V_{IL} = 0 V	–	–	10	µA
I_{IH1}	Input high current of PD#/OE and FS1	V_{IH} = V_{DD}	–	–	10	µA
I_{IL2}	Input low current of SSON, FS0, and FS2	V_{IL} = 0 V (Internal pull dn = 160k typ)	–	–	10	µA
I_{IH2}	Input high current of SSON, FS0, and FS2	V_{IH} = V_{DD} (Internal pull dn = 160k typ)	14	–	36	µA
R_{DN}	Pull down resistor of SSON, FS0, FS2 and clocks (CLK1–CLK9) in off-state	Clock outputs in off-state by setting PD# = Low	100	160	250	kΩ
I_{DD}[1, 2]	Supply current for CY2546	PD# = High, No load	–	20	–	mA
	Supply current for CY2544/CY2548	PD# = High, No load	–	22	–	mA
I_{DDS}[1]	Standby current	PD# = Low	–	3	–	µA
C_{IN}[1]	Input capacitance	SSON, CLKIN, PD#/OE, FS0, FS1, and FS2 pins	–	–	7	pF

Notes
1. Guaranteed by design but not 100% tested.
2. Configuration dependent.

AC Electrical Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{IN} (crystal)	Crystal frequency, XIN	–	8	–	48	MHz
F_{IN} (clock)	Input clock frequency (CLKIN or EXCLKIN)	–	8	–	166	MHz
F_{CLK}	Output clock frequency	–	3	–	166	MHz
DC1	Output duty cycle, All clocks except ref out	Duty cycle is defined in Figure 4; t_1/t_2, measured at 50% of $V_{DD\_CLK\_BX}$	45	50	55	%
DC2	Ref Out clock duty cycle	Ref In Min 45%, Max 55%	40	–	60	%
T_{RF1}[3]	Output rise/fall Time	Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 5, C_{LOAD} = 15 pF, Drive strength [00]	–	6.8	–	ns
T_{RF2}[3]	Output rise/fall time	Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 5, C_{LOAD} = 15 pF, Drive strength [01]	–	3.4	–	ns
T_{RF3}[3]	Output rise/fall time	Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 5, C_{LOAD} = 15 pF, Drive strength [10]	–	2.0	–	ns
T_{RF4}[3]	Output rise/fall time	Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 5, C_{LOAD} = 15 pF, Drive strength [11]	–	1.0	–	ns
T_{CCJ}[3,4]	Cycle-to-cycle Jitter (peak)	Configuration dependent. See Configuration Example for C-C Jitter	–	150	–	ps
T_{LOCK}[3]	PLL lock time	Measured from 90% of the applied power supply level	–	1	3	ms

Configuration Example for C-C Jitter

Ref. Freq. (MHz)	CLK1 Output		CLK2 Output		CLK3 Output		CLK4 Output		CLK5 Output	
	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)
14.3181	8.0	134	166	103	48	92	74.25	81	Not Used	
19.2	74.25	99	166	94	8	91	27	110	48	75
27	48	67	27	109	166	103	74.25	97	Not Used	
48	48	93	27	123	166	137	166	138	8	103

Recommended Crystal Specification

For SMD Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
F_{IN}	Crystal frequency	8–14	14–28	28–48	MHz
R1	Maximum motional resistance (ESR)	135	50	30	Ω
CL	Parallel load capacitance (see Note 3 below)	8–18	8–14	8–12	pF
DL(max)	Maximum crystal drive level	300	300	300	µW

Notes
3. Guaranteed by design but not 100% tested.
4. Configuration dependent.

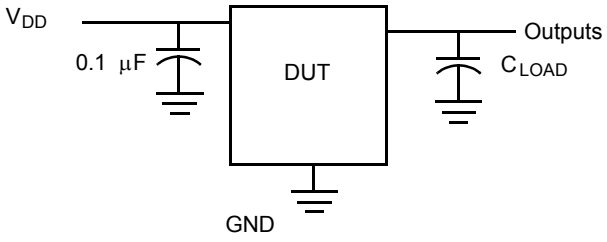
Recommended Crystal Specification

For Thru-Hole Package

Parameter [5]	Description	Range 1	Range 2	Range 3	Unit
F_{IN}	Crystal frequency	8–14	14–24	24–32	MHz
R1	Maximum motional resistance (ESR)	90	50	30	Ω
CL	Parallel load capacitance (see Note 6 below)	8–18	8–12	8–12	pF
DL(max)	Maximum crystal drive level	1000	1000	1000	µW

Test and Measurement Setup

Figure 3. Test and Measurement Setup



Voltage and Timing Definitions

Figure 4. Duty Cycle Definition

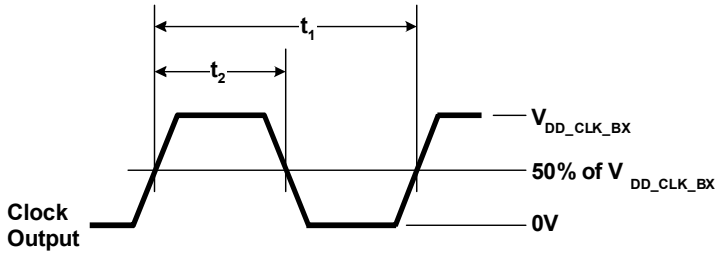
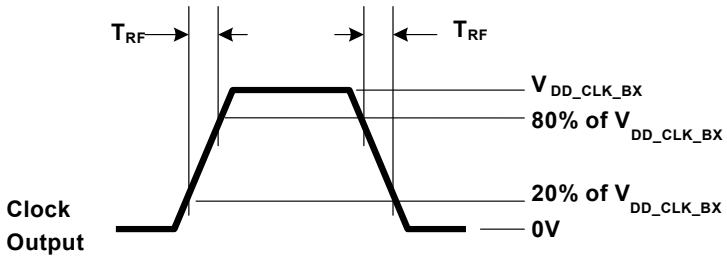


Figure 5. Rise Time = T_{RF}, Fall Time = T_{RF}



Notes
5. CY2544, CY2548 and CY2546 have internal crystal load capacitance (CL) adjustment feature.
6. Guaranteed by design but not 100% tested.

Ordering Information

Part Number	Type [7]	Package	Supply Voltage	Operating Range
Pb-free				
CY2544QFC	Field Programmable	24-pin QFN	2.5 V, 3.0 V or 3.3 V	Commercial, 0 °C to 70 °C
CY2544QFCT	Field Programmable	24-pin QFN – Tape and Reel	2.5 V, 3.0 V or 3.3 V	Commercial, 0 °C to 70 °C
CY2544QFI	Field Programmable	24-pin QFN	2.5 V, 3.0 V or 3.3 V	Industrial, –40 °C to +85 °C
CY2544QFIT	Field Programmable	24-pin QFN – Tape and Reel	2.5 V, 3.0 V or 3.3 V	Industrial, –40 °C to +85 °C
CY2548QI	Field Programmable	24-pin QFN	2.5 V, 3.0 V or 3.3 V	Industrial, –40 °C to +85 °C
CY2548QIT	Field Programmable	24-pin QFN – Tape and Reel	2.5 V, 3.0 V or 3.3 V	Industrial, –40 °C to +85 °C
Programmer				
CY3675-CLKMAKER1		Programming kit		
CY3675-QFN24A		Socket adapter board, for programming CY2544 and CY2548[8]		

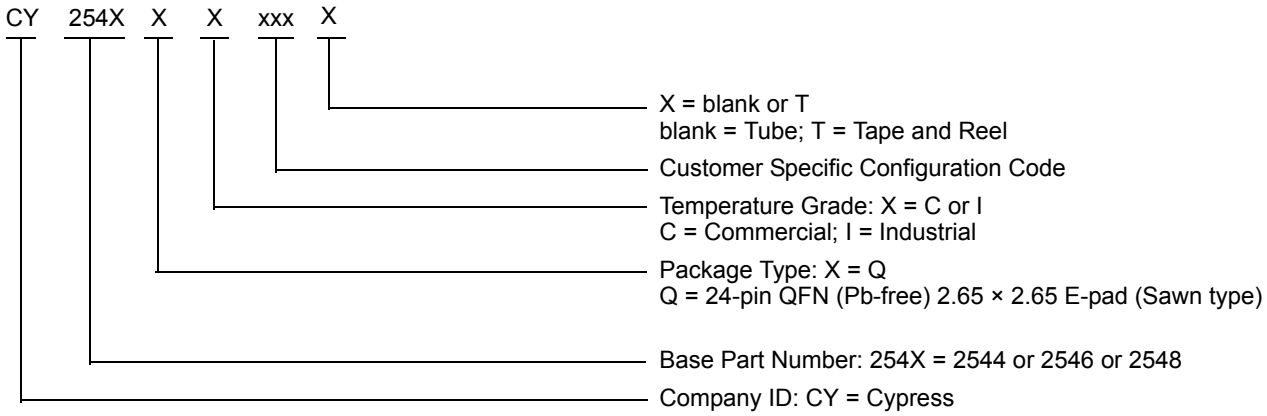
Some product offerings are factory programmed customer specific devices with customized part numbers.
The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

Possible Configurations

Part Number [9]	Type [7]	Package	Supply Voltage	Operating Range
Pb-free				
CY2544QCxxx	Factory Programmed	24-pin QFN	2.5 V, 3.0 V or 3.3 V	Commercial, 0 °C to 70 °C
CY2544QCxxxT	Factory Programmed	24-pin QFN – Tape and Reel	2.5 V, 3.0 V or 3.3 V	Commercial, 0 °C to 70 °C
CY2548QCxxx	Factory Programmed	24-pin QFN	2.5 V, 3.0 V or 3.3 V	Commercial, 0 °C to 70 °C
CY2548QCxxxT	Factory Programmed	24-pin QFN – Tape and Reel	2.5 V, 3.0 V or 3.3 V	Commercial, 0 °C to 70 °C
CY2546QCxxx	Factory Programmed	24-pin QFN	1.8 V	Commercial, 0 °C to 70 °C
CY2546QCxxxT	Factory Programmed	24-pin QFN – Tape and Reel	1.8 V	Commercial, 0 °C to 70 °C
CY2544QIxxx	Factory Programmed	24-pin QFN	2.5 V, 3.0 V or 3.3 V	Industrial, –40 °C to +85 °C
CY2544QIxxxT	Factory Programmed	24-pin QFN – Tape and Reel	2.5 V, 3.0 V or 3.3 V	Industrial, –40 °C to +85 °C
CY2548QIxxx	Factory Programmed	24-pin QFN	2.5 V, 3.0 V or 3.3 V	Industrial, –40 °C to +85 °C
CY2548QIxxxT	Factory Programmed	24-pin QFN – Tape and Reel	2.5 V, 3.0 V or 3.3 V	Industrial, –40 °C to +85 °C
CY2546QIxxx	Factory Programmed	24-pin QFN	1.8 V	Industrial, –40 °C to +85 °C
CY2546QIxxxT	Factory Programmed	24-pin QFN – Tape and Reel	1.8 V	Industrial, –40 °C to +85 °C

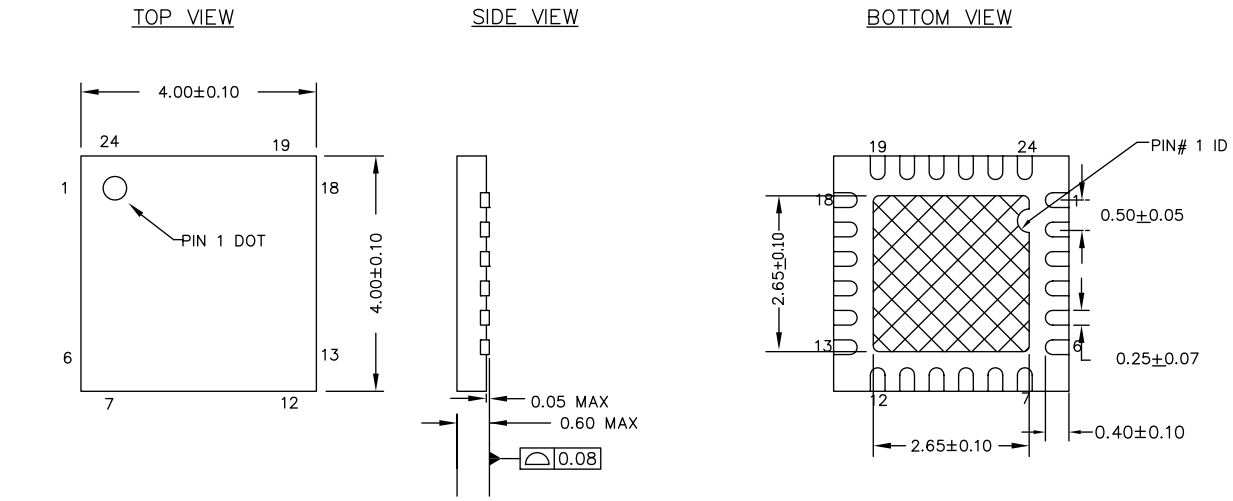
Notes
7. Field Programmable devices are shipped unprogrammed, and must be programmed before being installed on a board. Factory Programmed devices are shipped fully configured and ready to install on a board.
8. The CY3675-QFN24A cannot be used to program the CY2546.
9. “xxx” is a variable that denotes a specific device configuration. For more details, contact your local Cypress FAE or Cypress Sales Representative.

Ordering Code Definitions



Package Drawing and Dimensions

Figure 6. 24-pin QFN (4 × 4 × 0.55 mm) LQ24A 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Acronyms

Acronym	Description
DL	Drive Level
DNU	Do Not Use
DUT	Device Under Test
EIA	Electronic Industries Alliance
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FAE	Field Application Engineer
FS	Frequency Select
JEDEC	Joint Electron Devices Engineering Council
LVCMOS	Low Voltage Complimentary Metal Oxide Semiconductor
OE	Output Enable
OSC	Oscillator
PD	Power Down
PLL	Phase Locked Loop
PPM	Parts Per Million
SS	Spread Spectrum
SSC	Spread Spectrum Clock
SSON	Spread Spectrum On

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
fF	femtofarad
MHz	megahertz
µs	microsecond
µW	microwatt
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
ppm	parts per million
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2544/CY2546/CY2548, Quad-PLL Programmable Clock Generator with Spread Spectrum Document Number: 001-12563				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	690257	RGL	See ECN	New data sheet.
*A	790516	RGL	See ECN	Separated the Pin Configuration drawing into two to show the difference between CY2544 and CY2546 pinouts. Updated DC Electrical Specifications: Updated Test Conditions of I_{ILPDOE} parameter (Replaced “Internal pull up = 100k typical” with “No Internal pull up”). Changed maximum value of I_{ILPDOE} parameter from 10 µA to 1 µA. Updated Test Conditions of I_{IHPDOE} parameter (Replaced “Internal pull up = 100k typical” with “No Internal pull up”). Updated Test Conditions of I_{ILSR} parameter (Replaced “Internal pull down = 100k typical” with “Internal pull down = 160k typical”). Updated Test Conditions of I_{IHSR} parameter (Replaced “Internal pull down = 100k typical” with “Internal pull down = 160k typical”). Changed the maximum value of I_{IHSR} parameter from 10 µA to 25 µA. Removed maximum value of I_{DD} parameter (22 mA). Added typical value of I_{DD} parameter (15 mA).
*B	1508943	RGL / AESA	See ECN	Changed status from Preliminary to Final. Added Device Selection Guide. Updated Absolute Maximum Conditions: Changed condition of ESD_{HBM} parameter from “MIL-STD-883, Method 3015” to “JEDEC EIA/JESD22-A114-E”. Updated DC Electrical Specifications: Removed V_{IL}, V_{IH}, V_{ILX}, V_{IHX} parameters and their details. Added V_{IL1}, V_{IH1}, V_{IL2}, V_{IH2}, V_{IL3}, V_{IH3}, V_{IL4}, V_{IH4}, V_{IL5}, V_{IH5} parameters and their details. Renamed I_{ILPDOE} parameter as I_{IL1}, updated test conditions and changed maximum value of the same parameter from 1 µA to 10 µA. Renamed I_{IHPDOE} parameter as I_{IH1}, updated test conditions and changed maximum value of the same parameter from 1 µA to 10 µA. Renamed I_{ILSR} parameter as I_{IL2} and changed maximum value of the same parameter from 1 µA to 10 µA. Renamed I_{IHSR} parameter as I_{IH2}, changed maximum value of the same parameter from 25 µA to 36 µA and also added minimum value of the same parameter as 14 µA. Added R_{DN} parameter and its details. Changed typical value of I_{DDS} value from 50 µA to 3 µA. Updated AC Electrical Specifications: Added T_{RF1}, T_{RF2}, T_{RF3}, T_{RF4} parameters and their details. Renamed T_{CCJ1} parameter as T_{CCJ} and added typical value. Removed T_{LTJ} parameter and its details. Updated Configuration Example for C-C Jitter: Removed details of “Long Term Jitter”. Updated details corresponding to “Cycle-to-Cycle Jitter”. Updated Recommended Crystal Specification: Removed C0 parameter and its details. Updated Recommended Crystal Specification: Removed C0 parameter and its details. Updated Ordering Information: Deleted generic part numbers.
*C	2748211	TSAI	08/10/09	Post to external web.
*D	2764011	CXQ	09/15/09	Updated Ordering Information: Fixed typo (Changed CY2548Cxxx and CY2548CxxxT to CY2548Ixxx and CY2548IxxxT for industrial temp parts).

Document History Page (continued)

Document Title: CY2544/CY2546/CY2548, Quad-PLL Programmable Clock Generator with Spread Spectrum Document Number: 001-12563				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	2899758	KVM	03/26/10	Updated Ordering Information. Updated Package Drawing and Dimensions. Updated copyright section.
*F	2969587	KVM	07/09/2010	Minor change: Added “with Spread Spectrum” in first page title to match spec title on the first page with spec title on the document history page.
*G	3115710	BASH	12/21/2010	Added Ordering Code Definitions. Added Acronyms and Units of Measure.
*H	4239875	CINM	01/08/2014	Updated Package Drawing and Dimensions: spec 51-85203 – Changed revision from *B to *D. Updated to new template. Completing Sunset Review.
*I	4586478	AJU	03/12/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*J	5208624	PSR	04/06/2016	Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions. Updated Package Drawing and Dimensions: Added spec 001-13937 *F (Figure 6). Updated to new template.
*K	5563470	PSR	12/22/2016	Updated Ordering Information: Updated part numbers. Updated Possible Configurations: Updated part numbers. Updated Ordering Code Definitions. Updated Package Drawing and Dimensions: Removed spec 51-85203 *D. Updated to new template. Completing Sunset Review.

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