Author: Tu Bui

ISL8500EVAL2Z 2A Negative Output Buck-Boost Converter

Description

The ISL8500EVAL2Z REV A kit is intended for use by individuals with requirements for Point-of-Load applications sourcing from 9V to 14V. The ISL8500EVAL2Z evaluation board is used to demonstrate the performance of the ISL8500 standard buck-boost regulator.

The ISL8500 is offered in a 4mmx3mm 12 Ld DFN package with 1mm maximum height. The complete converter occupies less than 0.385in^2 area.

Features

- Standard Buck Controller with Integrated Switching Power MOSFET
- Integrated Boot Diode
- Input Voltage Range
  - Variable 9V to14V
- PWM Output Voltage Adjustable from -12.6V to -0.6V with Continuous Output Current up to 2A
- Voltage Mode Control with Voltage Feed Forward
- Fixed 500kHz Switching Frequency
- Externally Adjustable Soft-Start Time
- Output Undervoltage Protection
- PGOOD Output
- Overcurrent Protection
- Thermal Overload Protection
- Internal 5V LDO regulator

Applications

- General Purpose
- Hand-Held Instruments

What's Inside

The Evaluation Board Kit contains the following materials:

- The ISL8500 EVAL2Z REV A Board
- The ISL8500 Datasheet
- This EVAL KIT Document

Recommended Equipment

The following materials are recommended to perform testing:

- 0V to 15V power supply with at least 5A source current capability, battery, notebook AC adapter
- One electronic load capable of sinking current up to 5A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope
- Signal generator

Quick Set-up Guide

1. Ensure that the circuit is correctly connected to the supply and loads prior to applying any power.
2. Connect the bias supply to V_{IN}, the plus terminal to TP1 (VIN) and the negative return to TP2 (GND).
3. Verify that SW1 is on ENABLE.
4. Turn on the power supply.
5. Verify the PG is on and the output voltage is 2.5V for VOUT(TP3).

Evaluating the Other Output Voltage

The ISL8500EVAL kit outputs are preset to -12V; however, it can be programmed using resistor dividers using Equation 1:

$$R_4 = \frac{R_2 \cdot 0.6V}{|V_{OUT}| - 0.6V} \quad \text{(EQ. 1)}$$

The output voltage programming resistor R_2 will depend on on the feedback resistor R_1, as referred to in Figure 1. The value of R_1 is typically between 1kΩ and 10kΩ. If the output voltage desired is 0.6V, then R_2 is left opened.

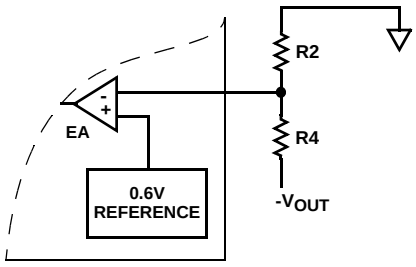
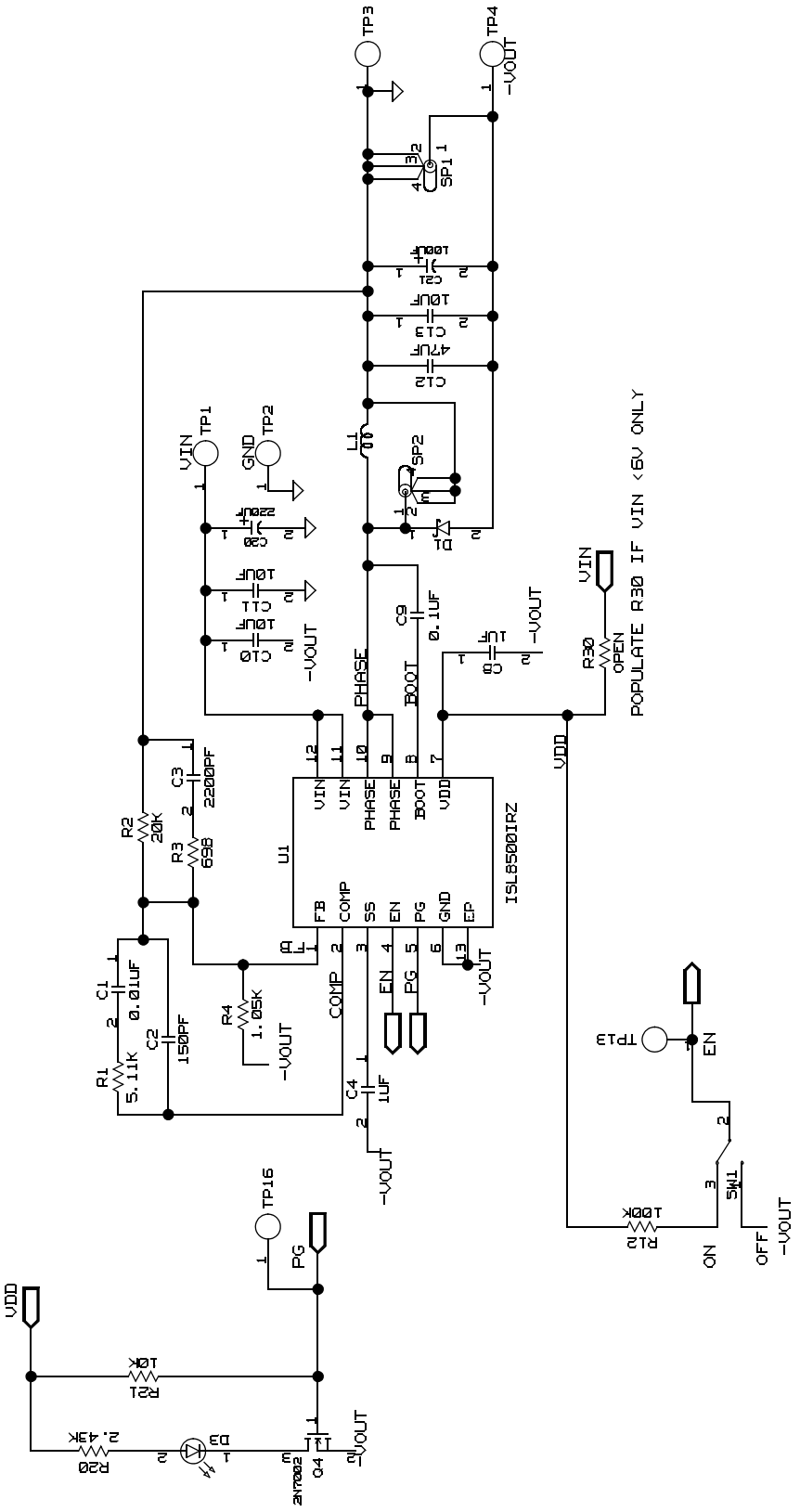


FIGURE 1. EXTERNAL RESISTOR DIVIDER

TABLE 1. SWITCH 1 SETTINGS

SW1	ENABLE	OPERATING MODE
1	SW1	Enable or disable the buck controller

Schematic


TP3
TP4
-VOUT
SP1
L2
C21
100UF
C13
10UF
C12
47UF
L1
0.1UH
SP2
D1
TP1
VIN
TP2
GND
C20
220UF
C11
10UF
C10
10UF
-VOUT
C9
0.1UF
C8
1UF
-VOUT
VIN
R30
OPEN
POPULATE R30 IF VIN <6V ONLY
PHASE
BOOT
VDD
U1
ISL85001IRZ
VIN
VIN
PHASE
PHASE
BOOT
VDD
FB
COMP
SS
EN
PG
GND
EP
R2
20K
R3
698
C3
2200PF
C1
0.01UF
C2
150PF
R1
5.11K
R4
1.05K
C4
1UF
-VOUT
TP13
EN
SW1
R12
100K
ON
OFF
-VOUT
TP16
PG
VDD
R21
10K
R20
2.43K
D3
Q4
2N7002
-VOUT

ISL8500EVAL2Z Bill of Materials

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MFTR	MANUFACTURER PART
ISL8500EVAL2ZREVAPCB	1	ea		PWB-PCB, ISL8500EVAL2Z, REVA, ROHS	TITAN	ISL8500EVAL2ZREVAPCB
H1044-00103-50V10-T	1	ea	C1	CAP, SMD, 0402, 10nF, 50V, 10%, X7R, ROHS	PANASONIC	ECJ-0EB1H103K
H1065-00106-25V10-T	2	ea	C10, C11	CAP, SMD, 1206, 10µF, 25V, 10%, X5R, ROHS	VENKEL	C1206X5R250-106KNE
DNP	0	ea	C13, C20, C21	DO NOT POPULATE OR PURCHASE		
H1082-00476-16V20-T	1	ea	C12	CAP, SMD, 1210, 47µF, 16V, 20%, X5R, ROHS	TDK	C3225X5R1C476M
					PANASONIC	ECJ-4YB1E476M
					AVX	1210YD476MAT
H1044-00151-50V5-T	1	ea	C2	CAP, SMD, 0402, 150pF, 50V, 5%, NPO, ROHS	VENKEL	C0402COG500-151JNE
H1044-00222-50V10-T	1	ea	C3	CAP, SMD, 0402, 2200pF, 50V, 10%, X7R, ROHS	PANASONIC	ECJ-0EB1H222K
					VENKEL	C0402X74500-471KNE
H1045-00105-6R3V10-T	2	ea	C4,C8	CAP, SMD, 0603, 1µF, 6.3V, 10%, X5R, ROHS	PANASONIC	ECJ1VB0J105K
C1608X7R1H104K-T	1	ea	C9	CAPACITOR, SMD, 0603, 0.10µF, 50V, 10%, X7R	TDK	C1608X7R1H104K
B340LB-13-F-T	1	ea	D1	DIODE-SCHOTTKY SMD, SMB, 2P, 40V, 3A LOW VF, ROHS	DIODES INC.	B340LB-13-F
DNP	0	ea	D3	DO NOT POPULATE OR PURCHASE		
IHLP2525CZRZ220M01	1	ea	L1	COIL-PWR INDUCTOR, SMD, 6.9x6.5, 22µH, 20%, 2.5A, ROHS	VISHAY	IHLP2525CZRZ220M01
DNP	0	ea	Q4	DO NOT POPULATE OR PURCHASE		
H2510-05111-1/16W1-T	1	ea	R1	RES, SMD, 0402, 5.11k, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF5111X
					VENKEL	CR0402-16W-5111FT
H2510-01003-1/16W1-T	1	ea	R12	RES, SMD, 0402, 100k, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ2RKF1003
H2510-02002-1/16W1-T	1	ea	R2	RES, SMD, 0402, 20k, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF2002
					VENKEL	CR0402-16W-2002FT
DNP	0	ea	R20	DO NOT POPULATE OR PURCHASE		
H2511-01002-1/10W1-T	1	ea	R21	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	KOA	RK73H1JT1002F
					VENKEL	CR0603-10W-1002FT
H2510-06980-1/16W1-T	1	ea	R3	RES, SMD, 0402, 698Ω, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF6980X
					VENKEL	CR0402-16W-6980-FT

ISL8500EVAL2Z Bill of Materials (Continued)

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MFTR	MANUFACTURER PART
H2511-DNP	0	ea	R30	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS		
H2510-01051-1/16W1-T	1	ea	R4	RES, SMD, 0402, 1.05k, 1/16W, 1%, TF, ROHS	VENKEL	CR0402-16W-1051FT
					PANASONIC	ERJ-2RKF1051X
					VISHAY/DALE	CRCW04021K05FKED
131-4353-00	2	ea	SP1, SP2	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS	TEKTRONIX	131-4353-00
GT11MSCBE-T	1	ea	SW1	SWITCH-TOGGLE, SMD, ULTRAMINI, 1P, SPST MINI	C&K COMPONENTS	GT11MSCKE
5002	2	ea	TP13, TP16	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	5002
1514-2	4	ea	TP1-TP4	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE	1514-2
ISL8500IRZ	1	ea	U1	IC-2A BUCK REGULATOR, 12P, DFN, 4x3, ROHS	INTERSIL	ISL8500IRZ

ISL8500EVAL2Z Board Layout

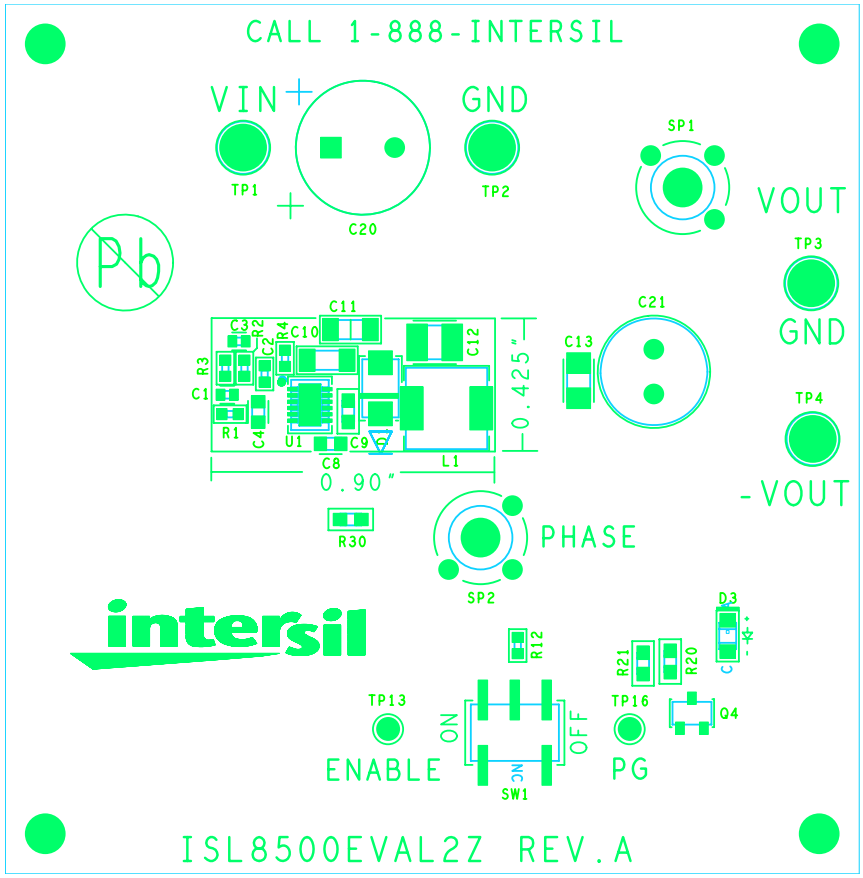


FIGURE 2. TOP COMPONENTS

ISL8500EVAL2Z Board Layout (Continued)

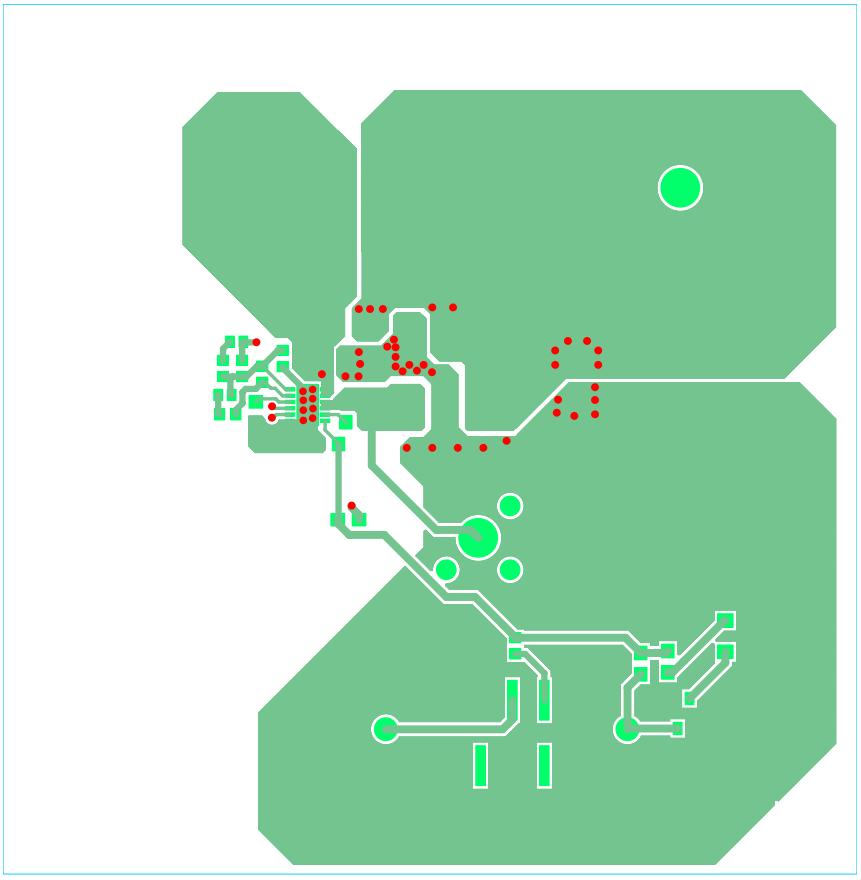


FIGURE 3. TOP LAYER ETCH

ISL8500EVAL2Z Board Layout (Continued)

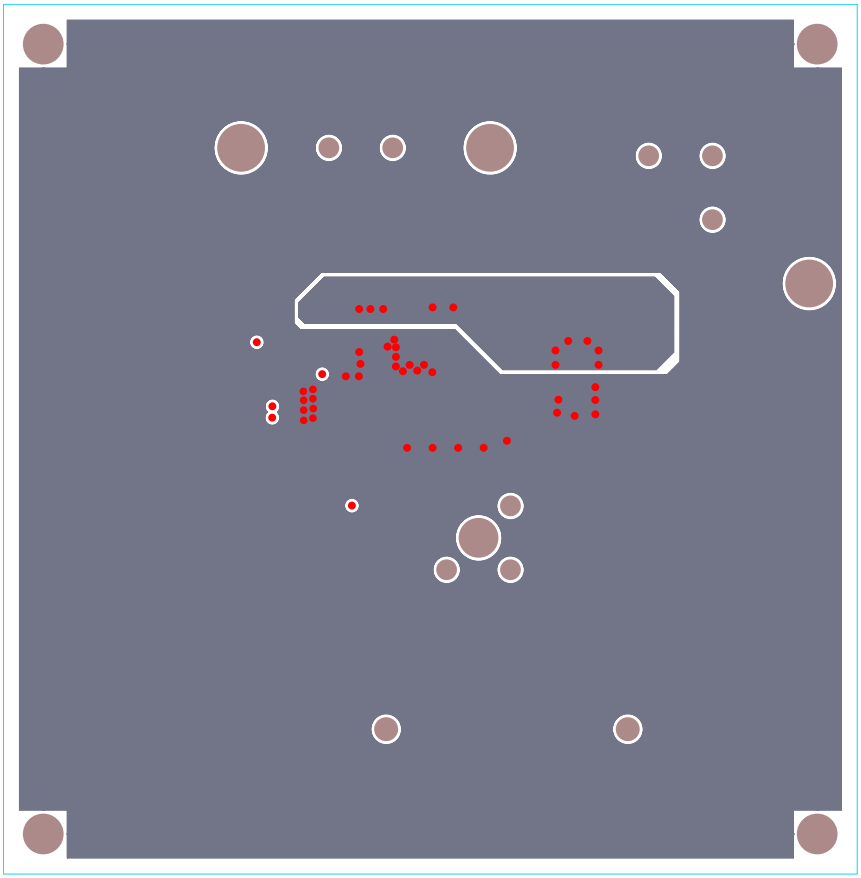


FIGURE 4. 2nd LAYER ETCH

ISL8500EVAL2Z Board Layout (Continued)

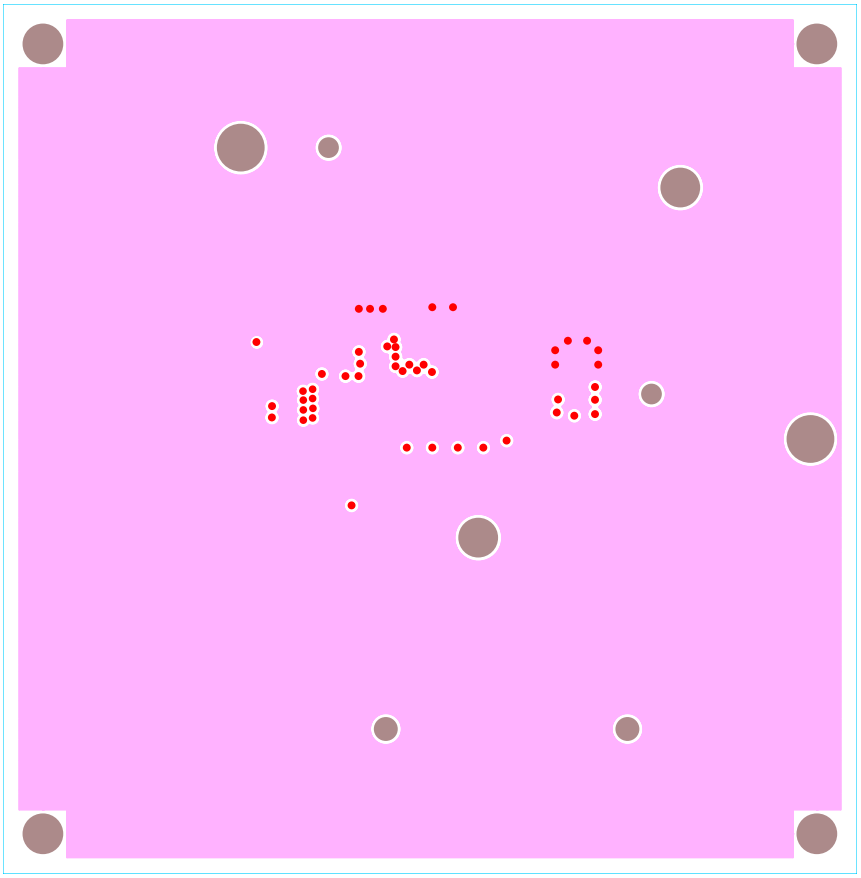


FIGURE 5. 3rd LAYER ETCH

ISL8500EVAL2Z Board Layout (Continued)

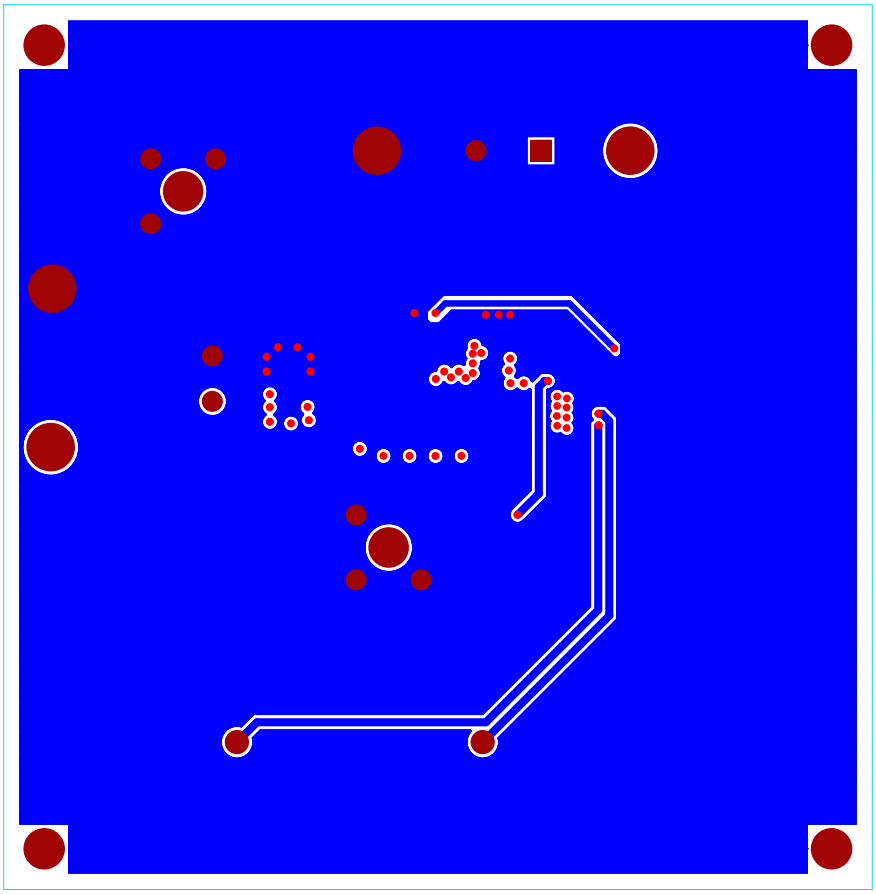


FIGURE 6. BOTTOM LAYER ETCH (Mirrored)

Theory of Operation

The ISL8500 in this configuration is a non-sysnchronous positive to negative switching regulator which can handle input voltages above, below, or equal to the absolute value of the output. The ISL8500EVAL2Z circuit design is optimized for 12V input to -12V output applications. The regulator operates at 500kHz fixed switching frequency, F_S, under heavy load conditions to allow smaller external inductors and capacitors to be used for minimal printed-circuit board (PCB) area. At light load, the regulator reduces the switching frequency by skipping pulses to maintain regulation and increase efficiency.

The principle of operation is shown in Figure 7 and uses the energy storage of the inductor L during the on period, and then transfers the energy through the free wheeling diode, D, to the output. When the HS MOSFET switch turns on, the diode is reverse biased, and the inductor current will ramp up. When the switch is off, as shown in Figure 8, the inductor will reverse its polarity to maintain its peak current. The forward biased diode and the stored energy of the inductor gets transferred to the load and the output capacitor. Since the voltage of the inductor is negative with respect to GND, the output voltage across the capacitor will be negative. This type of converter can step up and down the magnitude of the input voltage. Therefore, this circuit is called a buck-boost converter. For steady state operation, the volt-second of the inductor must equal, $DV_L = (1-D)V_L$. V_L is equal to V_{IN} during the ON time and V_L is equal to $-V_{OUT}$ during the OFF time. Therefore, the DC steady state transfer is $V_{OUT}/V_{IN} = -D/(1-D)$. Figure 9 is the voltage and current waveforms.

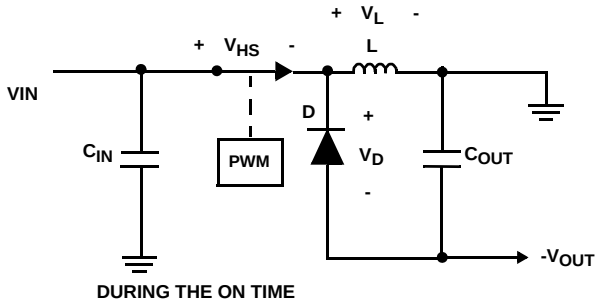


FIGURE 7. VOLTAGE ACROSS THE ELEMENT DURING THE ON TIME

Equation 2 for Figure 7:

$$V_L = V_{IN}$$
$$V_D = V_{IN} + V_{OUT} \quad \text{(EQ. 2)}$$
$$V_{HS} \approx 0V$$

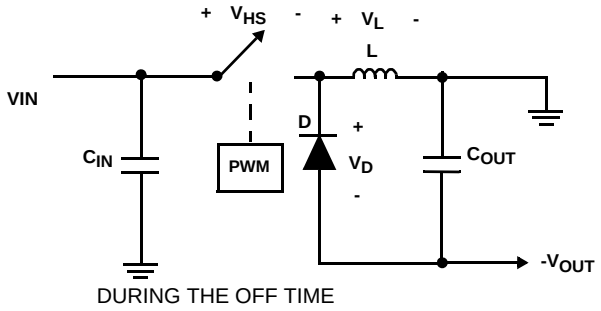


FIGURE 8. VOLTAGE ACROSS THE ELEMENT DURING THE OFF TIME

Equation 3 for Figure 8:

$$V_L = V_{OUT}$$
$$V_D \approx 0V \quad \text{(EQ. 3)}$$
$$V_{HS} = V_{IN} + V_{OUT}$$

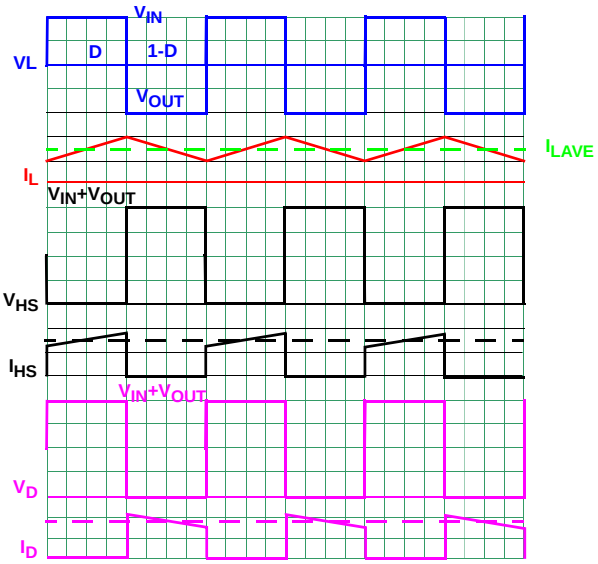


FIGURE 9. SIMPLIFICATION OF THE BUCK BOOST CONVERTER

Equation 4 for Figure 9:

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}}$$
$$I_{LAVE} = I_{OUT}\left(1 + \frac{D}{1-D}\right) \quad \text{(EQ. 4)}$$
$$\Delta I_L = V_{IN} \cdot \frac{D}{L \cdot F_S}$$

Component Selection

This section will detail the calculation and selection of the components. Calculations are done in continuous operation mode.

Inductor Selection

From Equation 3 and ignoring the diode V_D and $r_{DS(ON)}$ of the FET, the duty cycle is shown in Equation 5.

$$D \approx \frac{|V_{OUT}|}{V_{IN} + |V_{OUT}|} \quad \text{(EQ. 5)}$$

For this example, D is 12V/(12V+12V) = 0.5.
The average inductor current is shown in Equation 6.

$$I_{LAVE} = I_{OUT}\left(1 + \frac{D}{1-D}\right) = I_{OUT}\left(\frac{1}{1-D}\right) \quad \text{(EQ. 6)}$$

The higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. It is recommended to set the ripple inductor current approximately 20% to 30% of the maximum average inductor current for optimized performance. The inductor ripple current can be expressed as shown in Equation 7:

$$L = \frac{V_{IN} \cdot V_{OUT}}{(V_{IN} + V_{OUT})(0.3 \cdot I_{LAVE}) \cdot f_S} \quad \text{(EQ. 7)}$$

where f_S is the switching frequency. The inductor's saturation current rating needs to be at least larger than the peak current. The ISL8500 protects the typical peak current 3.1A. The saturation current needs be over 4A for maximum output current application. For I_{OUT} of 1A, the inductor L is 24µH. Then use 22µH.

Diode Selection

The free wheeling diode had to be able to handle the maximum voltage and current stress. The voltage stress is equal to V_{IN} plus V_{OUT} and the current stress is $I_{LAVE}+0.5\Delta I_L$. The power dissipation is shown in Equation 8.

$$P_D = (I_{LAVE} + 0.5\Delta I_L) \cdot V_D \cdot (1 + D) \quad \text{(EQ. 8)}$$

where V_D is the forward voltage of the diode. This value is typically 0.5V for 3A Schottky diode. A 30V or 40V 3A, B340LB is a good choice.

Output Capacitor Selection

The output capacitor has to be selected based on its R_{ESR} value, and the capacitance must be high enough to hold the charges for the load during the off time. The output ripple is shown in Equation 9.

$$\Delta V_{OUT} = R_{ESR} \cdot (I_{LAVE} + 0.5\Delta I_L) \quad \text{(EQ. 9)}$$

where ΔV_{OUT} is the desired output ripple. The minimum output capacitor value for tis output ripple is shown in Equation 10.

$$C_{OUT} = \frac{I_{OUT} \cdot D}{f_S \cdot \Delta V_{OUT}} \quad \text{(EQ.10)}$$

Use 47µF 16V ceramic for this example.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. Two 10µF X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection. One capacitor connecting from V_{IN} to $-V_{OUT}$ and another one connecting from V_{IN} to GND.

Compensation Selection

The buck-boost typology is difficult to stabilize because it has a right-half-plane zero in its control to output transfer function. The small signal AC model of the buck-boost power section in relationship to d(s) is shown in Figure 10.

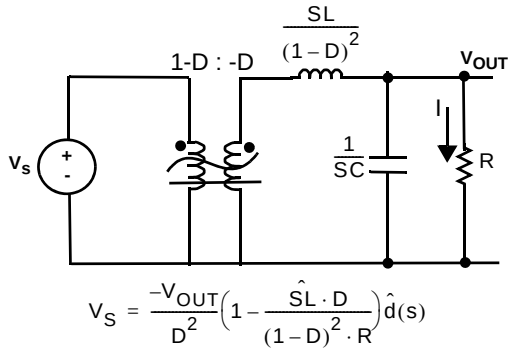


FIGURE 10. SMALL SIGNAL AC MODEL

To solve the power transfer function, see Equation 11.

$$H(S) = \frac{\hat{V}_{OUT}(S)}{\hat{d}(S)} = -\frac{V_{IN} - V_{OUT}}{1-D}\left(\frac{1 - \frac{SLI}{(1-D)(V_{IN} - V_{OUT})}}{1 + \frac{SL}{(1-D)^2 R} + \frac{S^2 LC}{(1-D)^2}}\right) \quad \text{(EQ.11)}$$

The salent characteristics are shown in Equation 12.

$$H(0) = -\frac{V_{IN} - V_{OUT}}{1-D} = \frac{V_{OUT}}{D(1-D)} = \frac{12V}{0.5 \cdot 0.5} = 48$$

$$\rightarrow H(0)=33.8dB$$

$$\omega_Z = \frac{(1-D)(V_{IN} - V_{OUT})}{LI} = \frac{(1-D)^2 R}{DL}, \text{ this is RHPZ}$$

$$\omega_Z = \frac{0.5^2 \cdot 12\Omega}{22\mu H \cdot 1A} = 136 \times 10^3 \rightarrow F_Z = 43.4 \times 10^3 Hz$$

$$Q = (1-D)R\sqrt{\frac{C}{L}} = 0.5 \cdot 12\Omega \cdot \sqrt{\frac{44\mu F}{22\mu H}} = 8.77 \quad \text{(EQ.12)}$$

$$\rightarrow Q=18.9dB$$

$$\omega_{LC} = \frac{(1-D)}{\sqrt{LC}} = \frac{0.5}{\sqrt{22\mu H \cdot 47\mu F}} = 12 \times 10^3$$

$$\rightarrow F_{LC}=2.4kHz$$

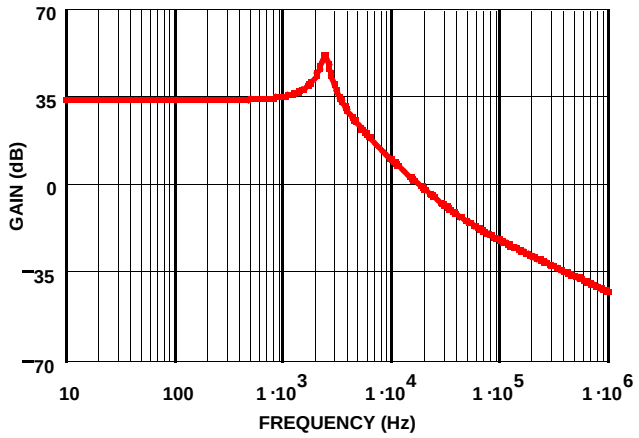


FIGURE 11. GAIN ON H(S) IN dB

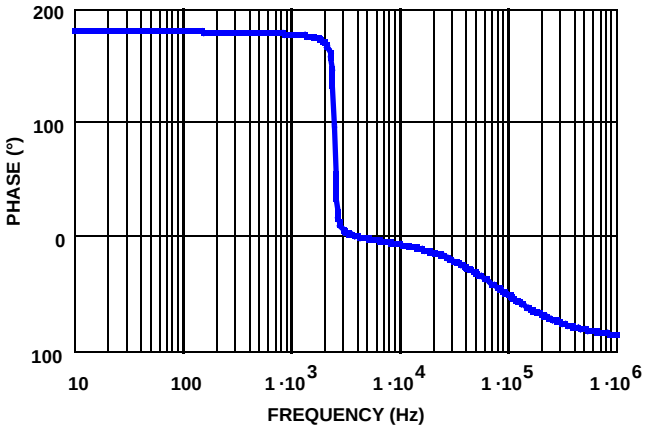


FIGURE 12. PHASE OF H(S) IN °

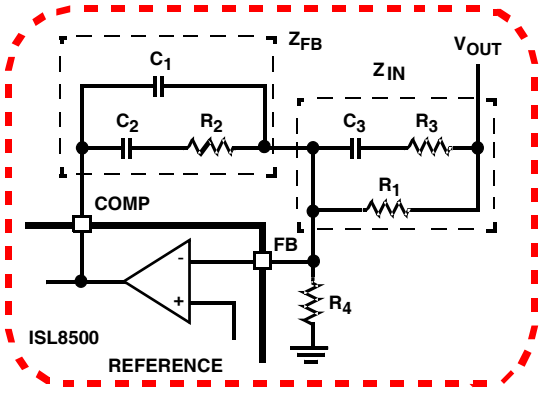


FIGURE 13. DETAILED COMPENSATION NETWORK

The compensation network consists of the error amplifier (internal to the ISL8500) and the impedance networks. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin.

From the transfer function, there is a right-half-plane-zero. Therefore, it is highly recommended to insure that the crossover frequency, F_c, is well before the F_Z. Figures 11 and 12 are the bode plot of the gain and phase for H(S).

Phase margin is the difference between the closed loop phase at f_{0dB} and 180°. Equation 13 relates the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 14. Use the following guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R_2/R_1) for converter bandwidth (~30% F_Z).
2. Place 1ST Zero Below Filter's Double Pole (~30% F_{LC}).
3. Place 2ND Zero at Filter's Double Pole.
4. Place 1ST Pole at half the Switching Frequency.
5. Place 2ND Pole at the 2.5x of RHP Zero.
6. Check Gain against Error Amplifier's Open-Loop Gain.

Estimate Phase Margin - Repeat if Necessary.

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_2} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)} \qquad \text{(EQ. 13)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad F_{P2} = \frac{1}{2\pi \times R_3 \times C_3}$$

Figures 14 and 15 shows the bode plot of the gain and phase for the closed loop response.

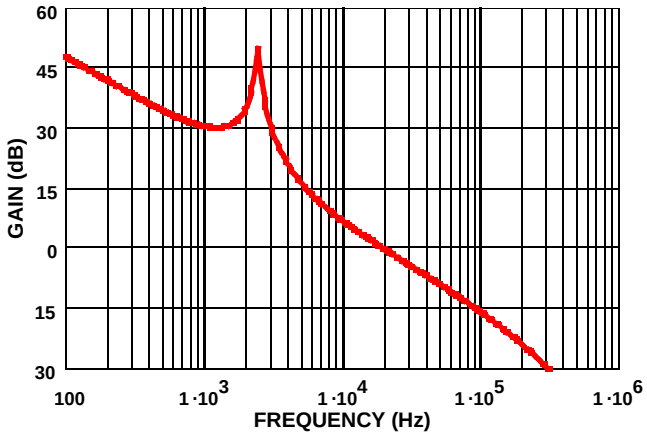


FIGURE 14. GAIN OF CLOSED LOOP IN dB

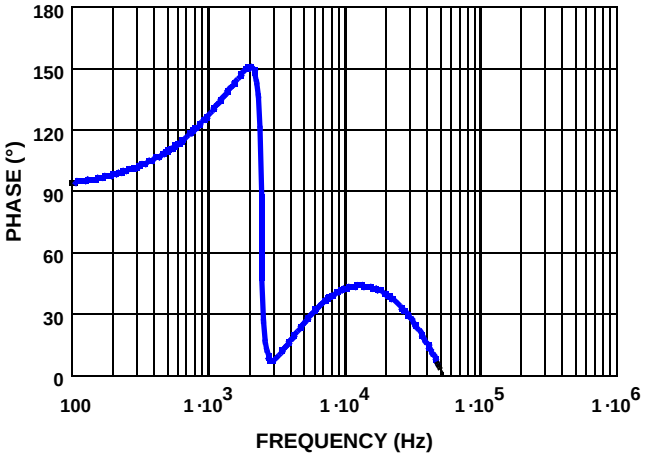


FIGURE 15. PHASE OF CLOSED LOOP IN °

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope, and a phase margin greater than 40°. Include worst case component variations when determining phase margin.

Typical Performace Curves

T_A = +25°C, Unless Otherwise Specified, operating conditions are: T_A = +25°C, V_{IN} = 12V, EN = V_{DD}, L = 22µH, C12 = 100µF, C10 = C11 = 10µF, I_{OUT} = 0A to 1A.

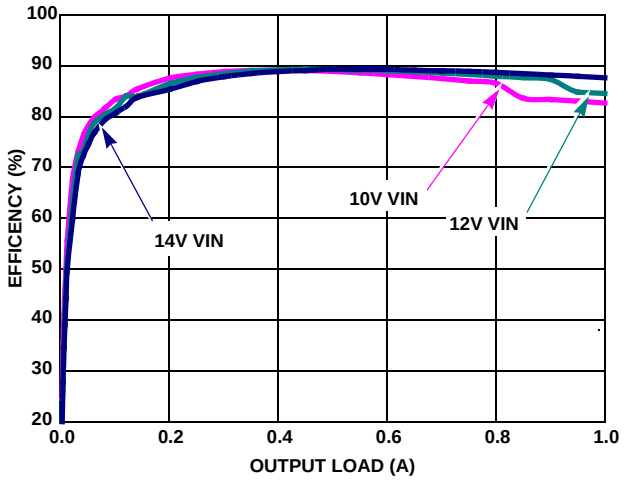


FIGURE 16. EFFICIENCY vs LOAD

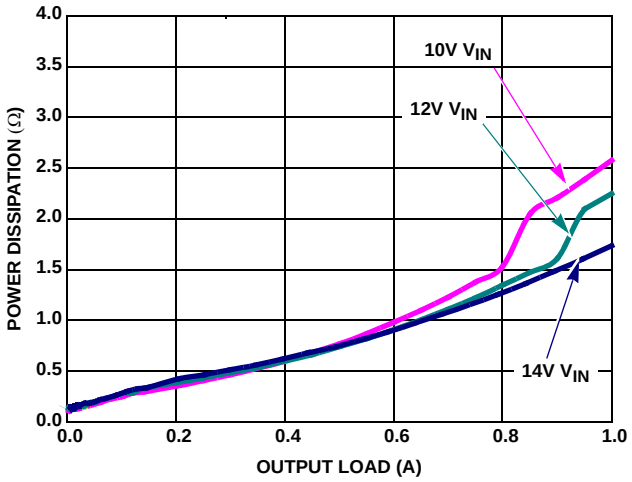


FIGURE 17. POWER DISSIPATION vs LOAD

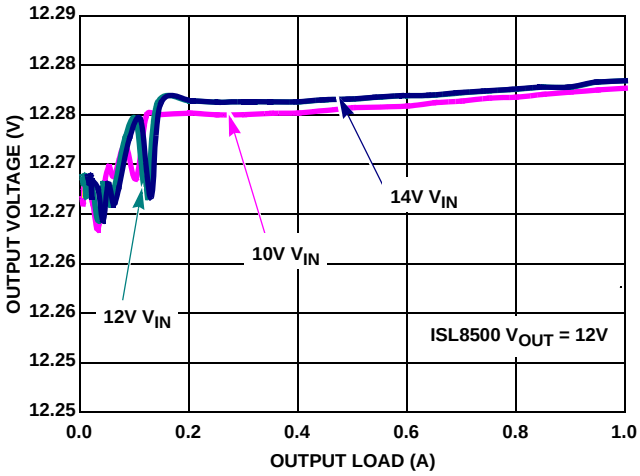


FIGURE 18. V_{OUT} REGULATION vs LOAD

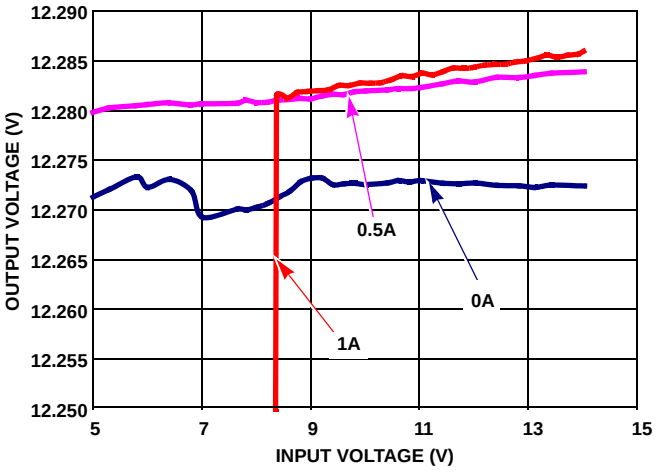


FIGURE 19. OUTPUT VOLTAGE REGULATION vs V_{IN}

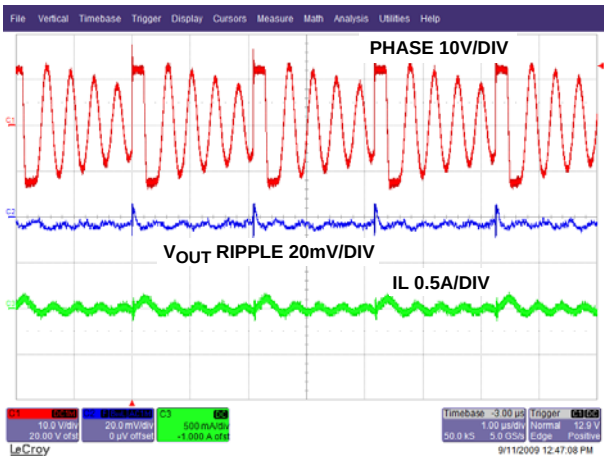


FIGURE 20. STEADY STATE OPERATION AT NO LOAD

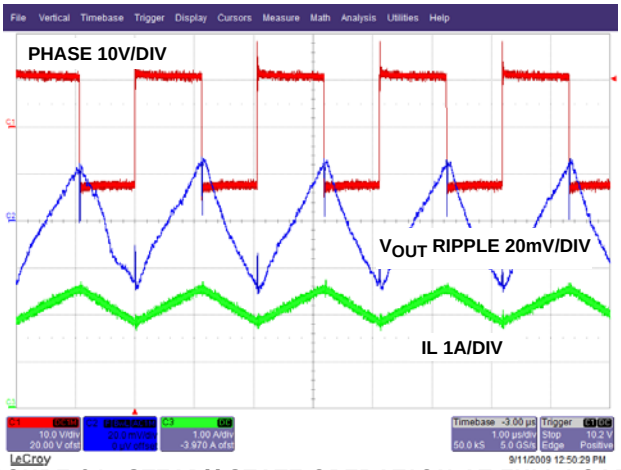


FIGURE 21. STEADY STATE OPERATION AT FULL LOAD

Typical Performace Curves

T_A = +25°C, Unless Otherwise Specified, operating conditions are: T_A = +25°C, V_{IN} = 12V, EN = V_{DD}, L = 22µH, C12 = 100µF, C10 = C11 = 10µF, I_{OUT} = 0A to 1A. **(Continued)**

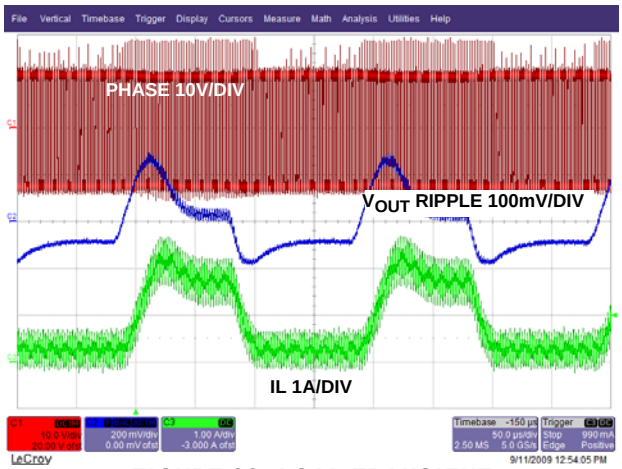


FIGURE 22. LOAD TRANSIENT

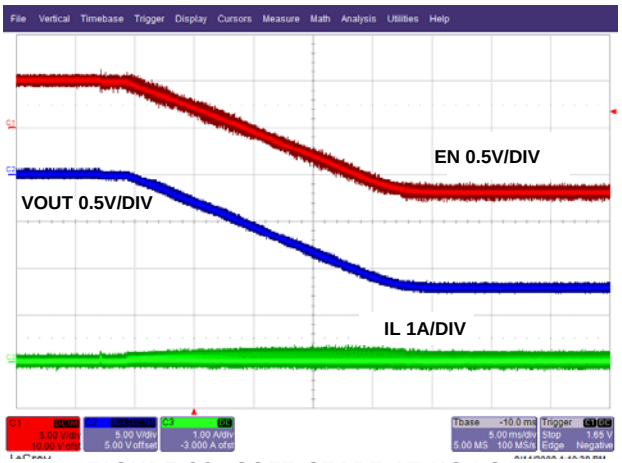


FIGURE 23. SOFT-START AT NO LOAD

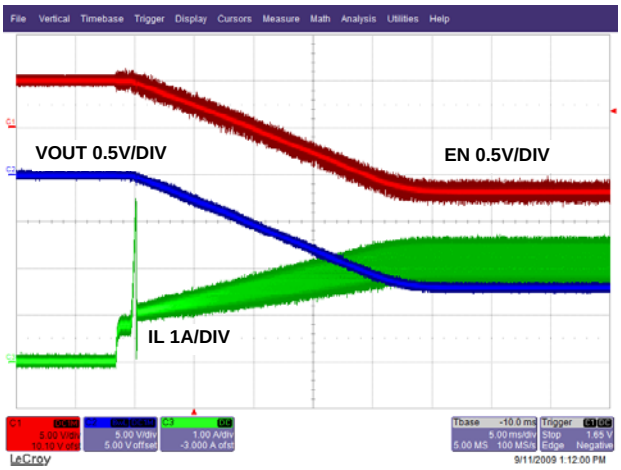


FIGURE 24. SOFT-START AT FULL LOAD

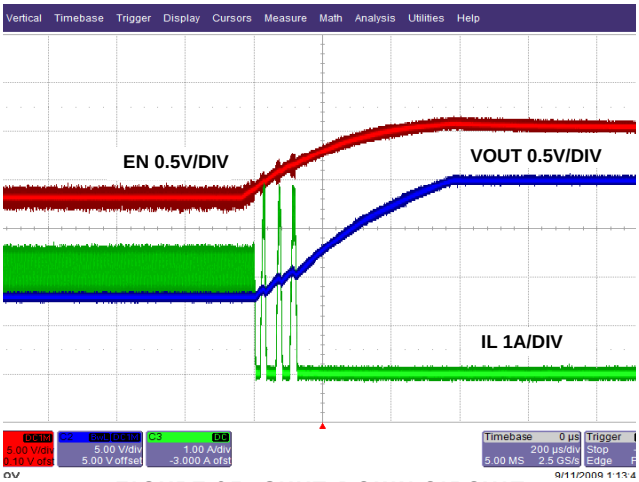


FIGURE 25. SHUT-DOWN CIRCUIT

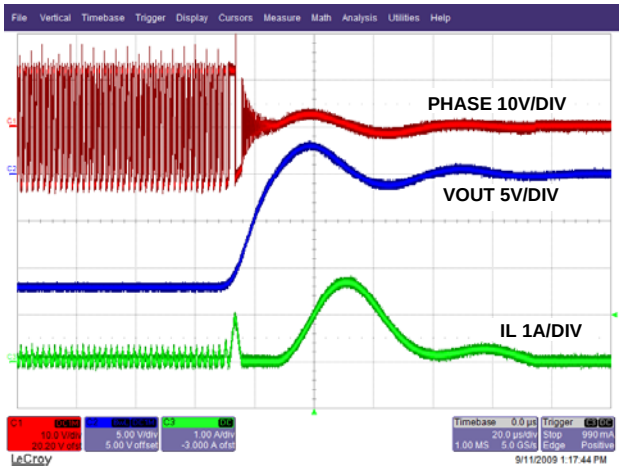


FIGURE 26. OUTPUT SHORT CIRCUIT

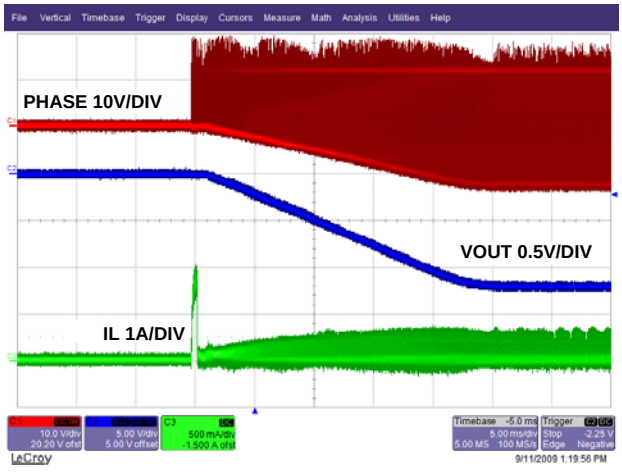


FIGURE 27. OUTPUT SHORT CIRCUIT RECOVERY