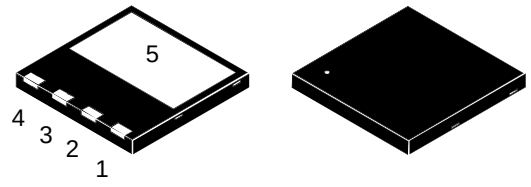
STL25N60M2-EP

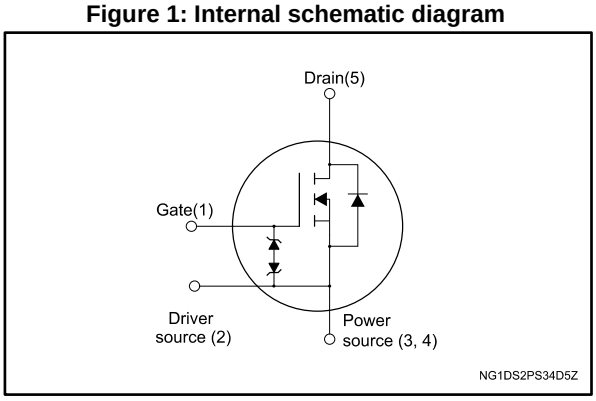
N-channel 600 V, 0.184 Ω typ., 16 A MDmesh™ M2 EP Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data



PowerFLAT™ 8x8 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STL25N60M2-EP	650 V	0.206 Ω	16 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for Very High Frequency Converters (f > 150 kHz)

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 EP enhanced performance technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL25N60M2-EP	25N60M2EP	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	16(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	10(1)	A
I_{DM}(2)	Drain current (pulsed)	64(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	W
dv/dt(3)	Peak diode recovery voltage slope	15	V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Operating junction temperature		

Notes:

(1)The value is limited by package.

(2)Pulse width limited by safe operating area.

(3)$I_{SD} \leq 16$ A, di/dt ≤ 400 A/µs; $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD} = 400 V.

(4)$V_{DS} \leq 480$ V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb max	45	°C/W

Notes:

(1)When mounted on FR-4 board of inch², 2oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	3.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$; V_{DD} = 50 V)	180	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 8 A		0.184	0.205	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	1090	-	pF
C_{oss}	Output capacitance		-	56	-	pF
C_{rss}	Reverse transfer capacitance		-	1.6	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	255	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 18 A, V_{GS} = 10 V (see *Figure 16: "Gate charge test circuit"*)	-	29	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching Energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% V_{GS} to 0% I_D)	V_{DD} = 400 V, I_D = 2 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	7	-	µJ
		V_{DD} = 400 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	8	-	µJ

Table 8: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 9 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15: "Switching times test circuit for resistive load"* and *Figure 20: "Switching time waveform"*)	-	15	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	61	-	ns
t_f	Fall time		-	16	-	ns

Table 9: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		16	A
I_{SDM} (1), (2)	Source-drain current (pulsed)		-		64	A
V_{SD} (3)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 16 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 100 V (see *Figure 17: " Test circuit for inductive load switching and diode recovery times"*)	-	360		ns
Q_{rr}	Reverse recovery charge		-	5		µC
I_{RRM}	Reverse recovery current		-	28		A
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150 °C (see *Figure 17: " Test circuit for inductive load switching and diode recovery times"*)	-	445		ns
Q_{rr}	Reverse recovery charge		-	6.5		µC
I_{RRM}	Reverse recovery current		-	29		A

Notes:

(1)The value is limited by package.

(2)Pulse width is limited by safe operating area

(3)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

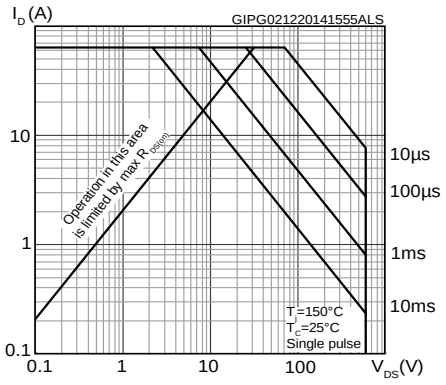


Figure 3: Thermal impedance

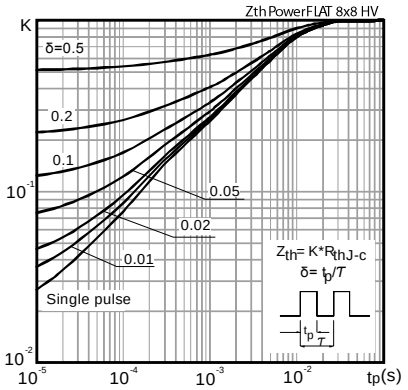


Figure 4: Output characteristics

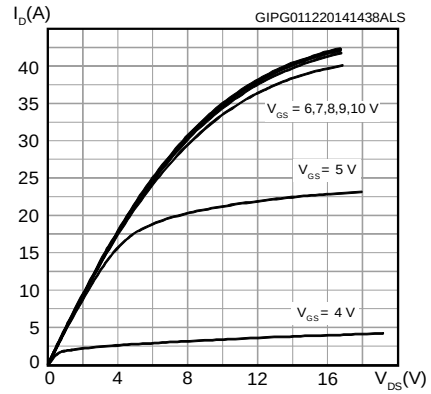


Figure 5: Transfer characteristics

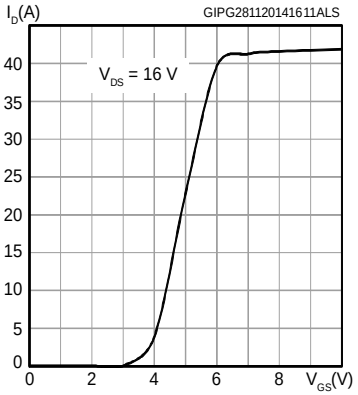


Figure 6: Gate charge vs gate-source voltage

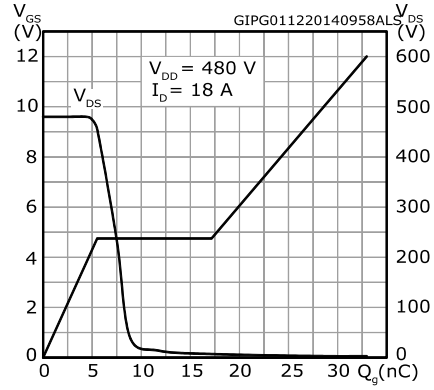


Figure 7: Static drain-source on-resistance

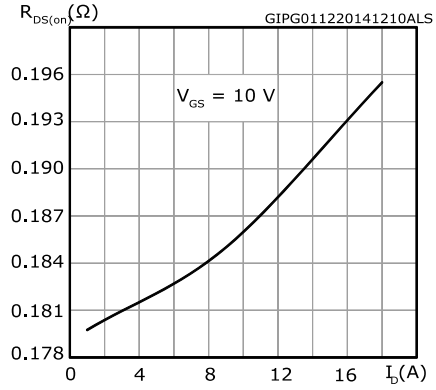


Figure 8: Capacitance variations

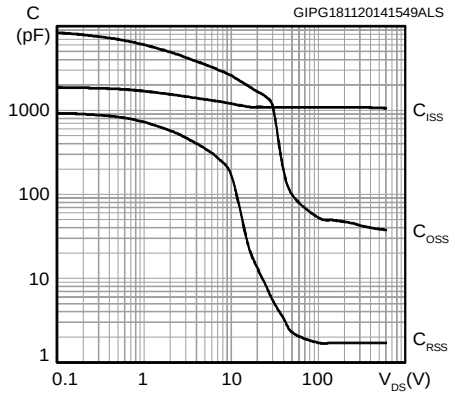


Figure 9: Output capacitance stored energy

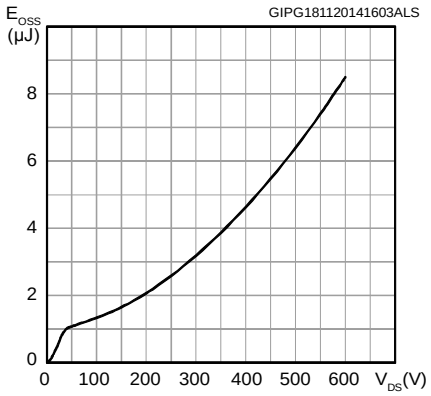


Figure 10: Turn-off switching loss vs drain current

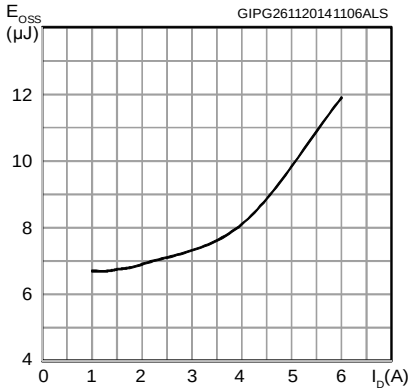


Figure 11: Normalized gate threshold voltage vs temperature

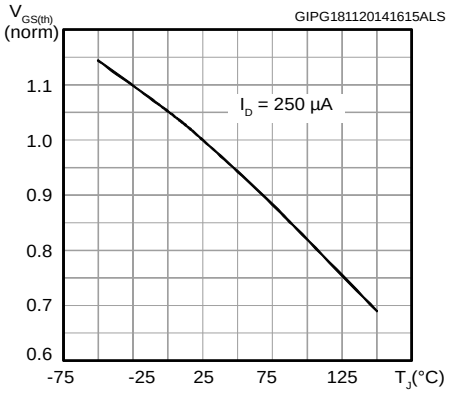


Figure 12: Normalized on-resistance vs temperature

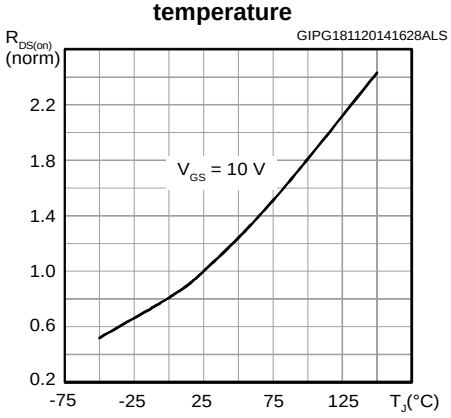


Figure 13: Source-drain diode forward characteristics

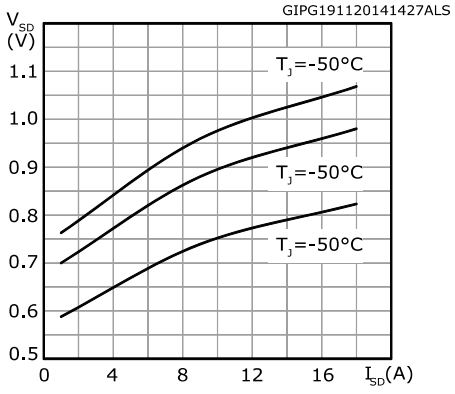
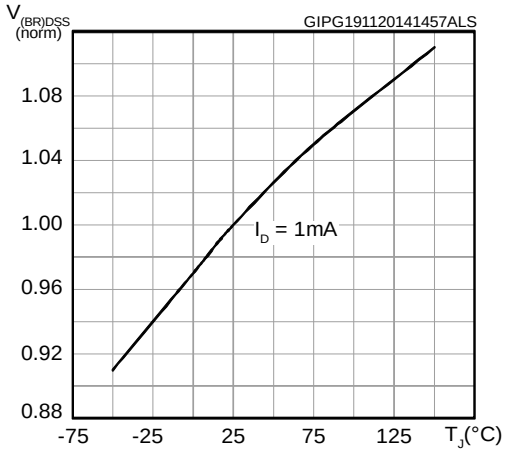


Figure 14: Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 15: Switching times test circuit for resistive load

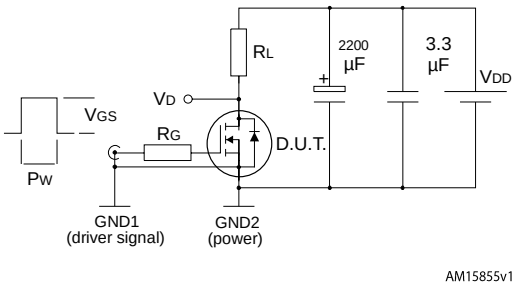


Figure 16: Gate charge test circuit

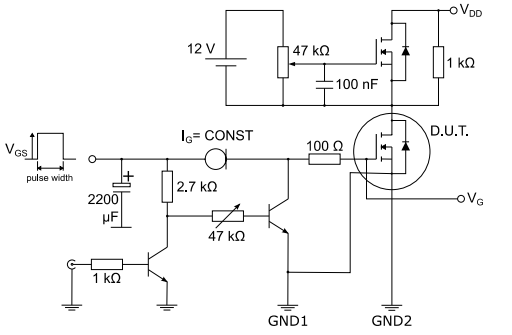


Figure 17: Test circuit for inductive load switching and diode recovery times

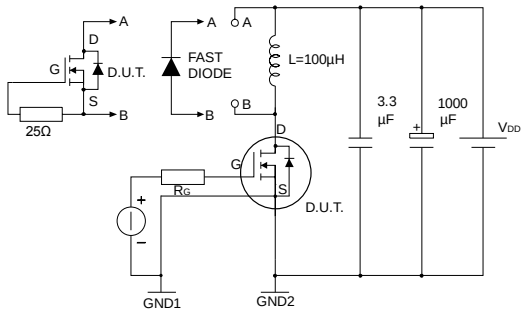


Figure 18: Unclamped inductive load test circuit

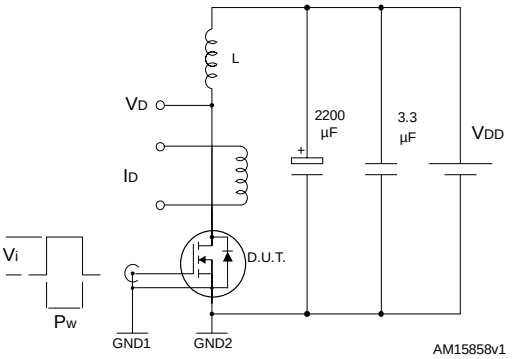


Figure 19: Unclamped inductive waveform

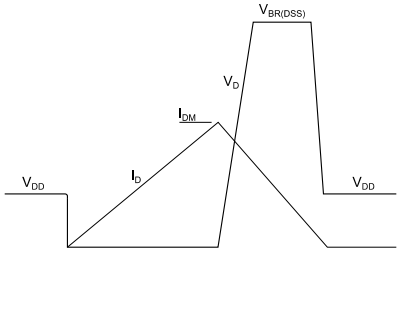
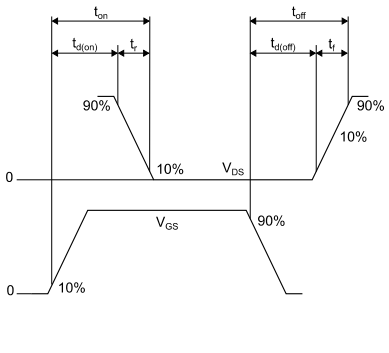


Figure 20: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT 8x8 HV package information

Figure 21: PowerFLAT™ 8x8 HV package outline

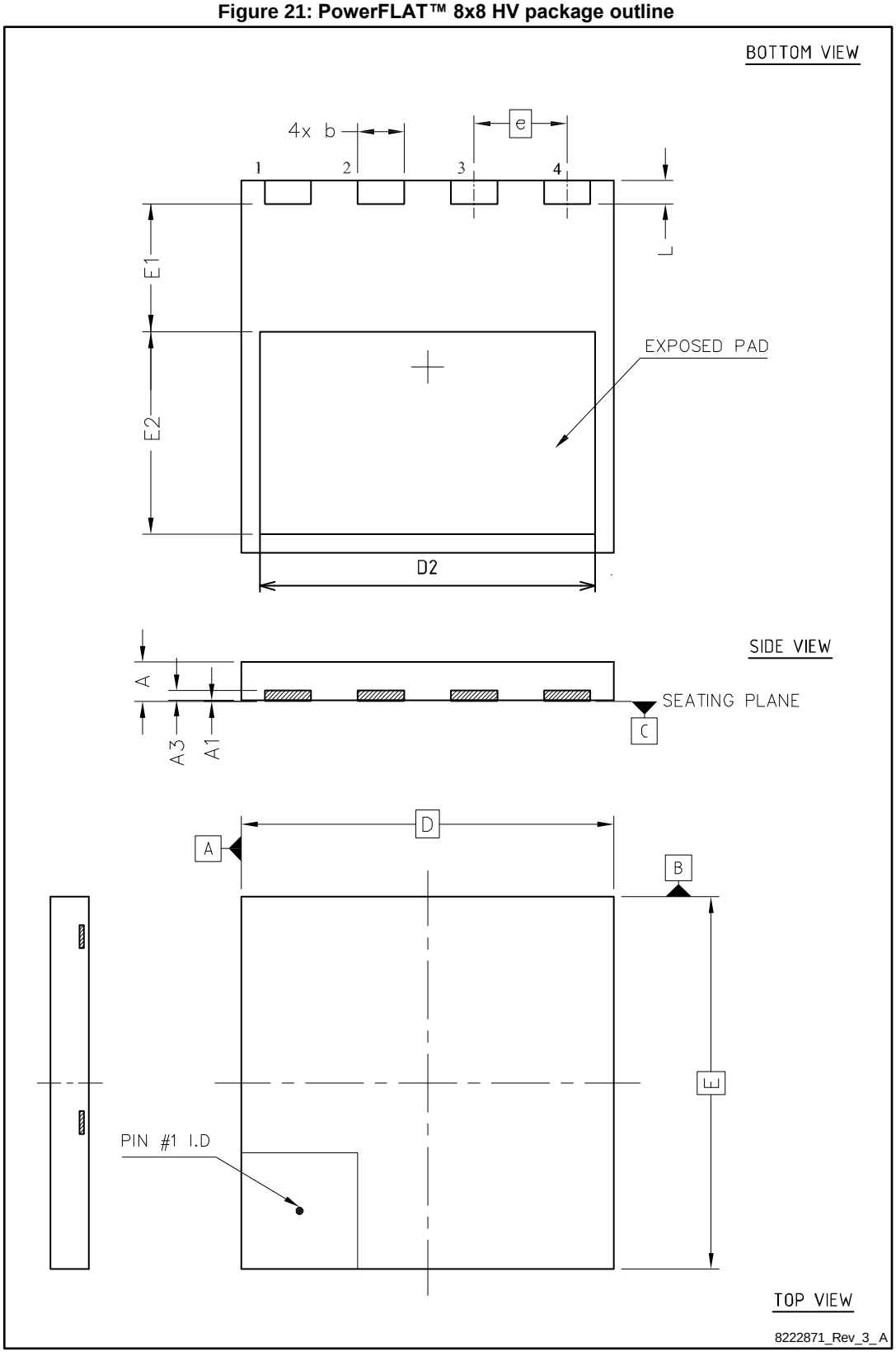
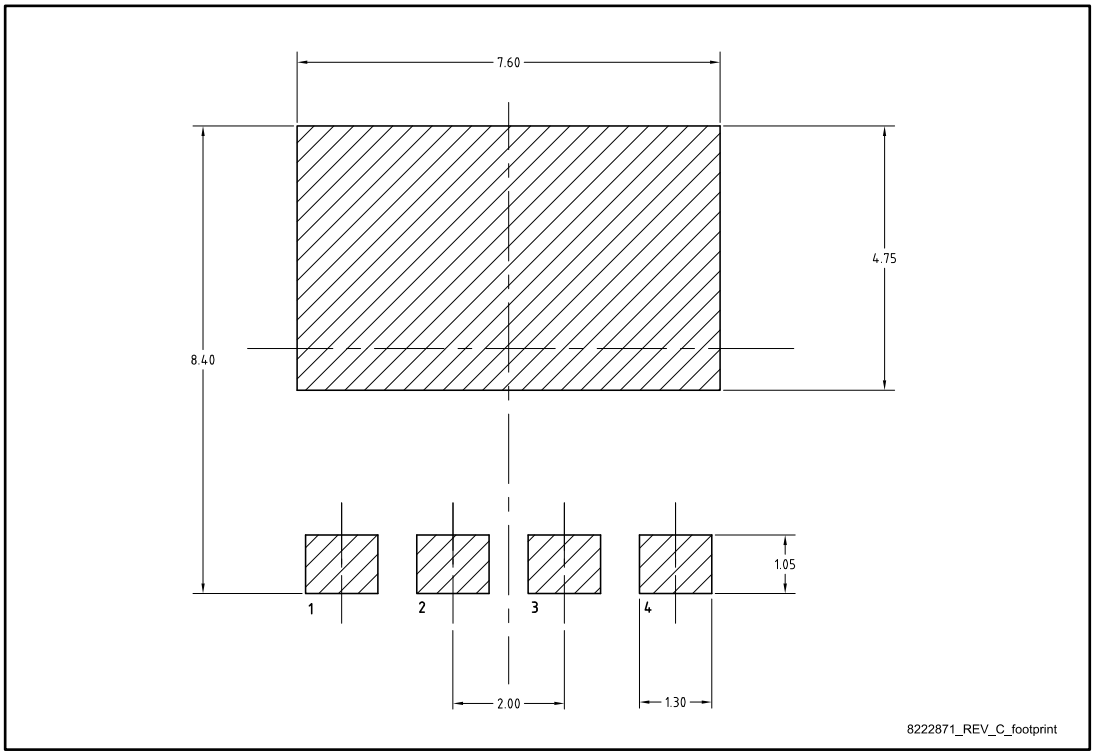


Table 10: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

Figure 22: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

5 PowerFLAT 8x8 HV packing information

Figure 23: PowerFLAT™ 8x8 HV tape

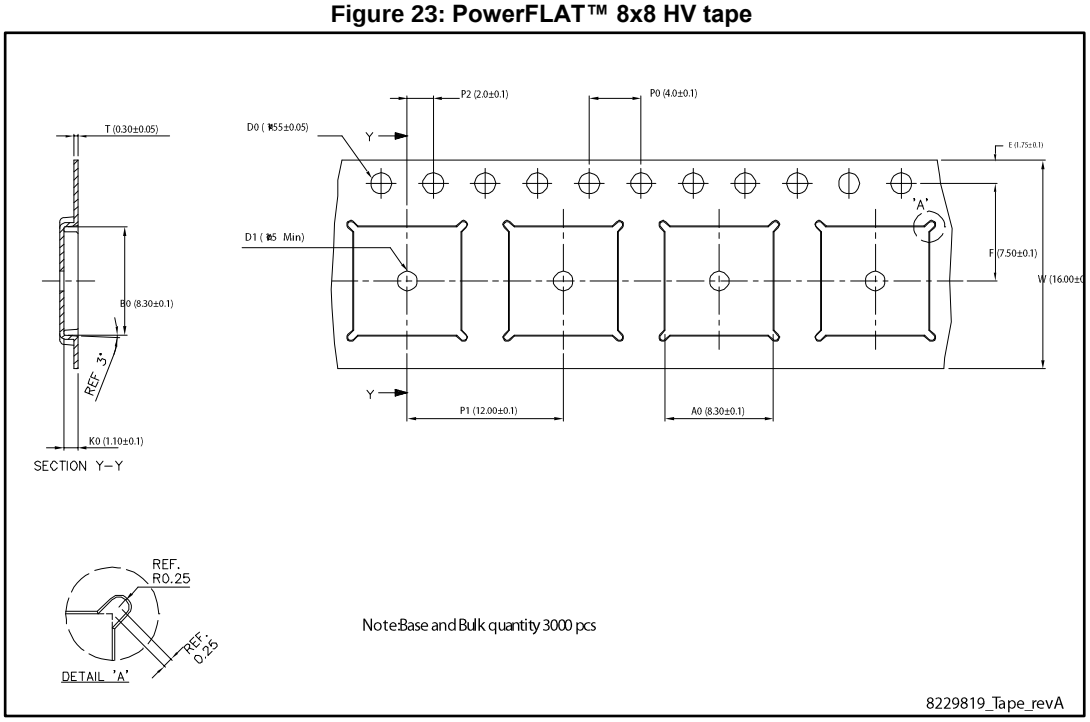


Figure 24: PowerFLAT™ 8x8 HV package orientation in carrier tape

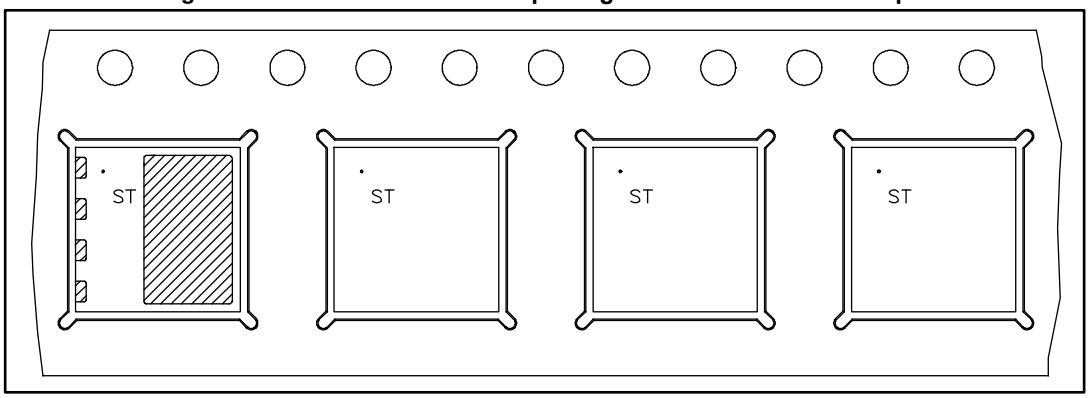
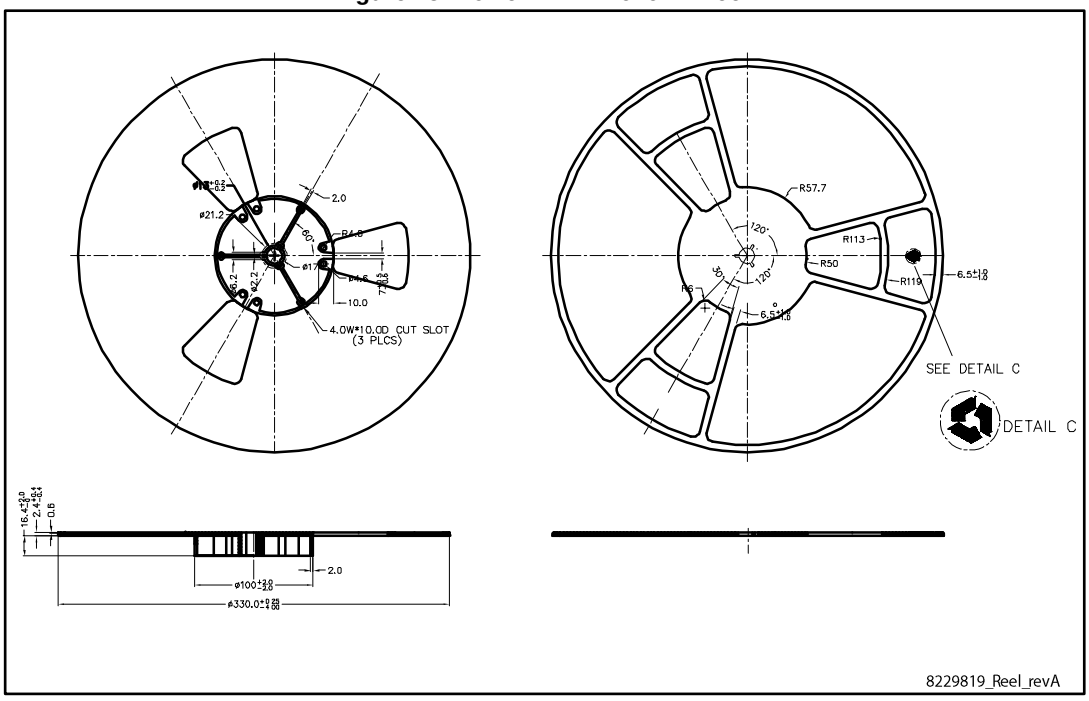


Figure 25: PowerFLAT™ 8x8 HV reel



6 Revision history

Table 11: Document revision history

Date	Revision	Changes
02-Dec-2014	1	First release.
12-Jan-2015	2	Updated product status from “preliminary data” to “production data”.
20-Nov-2015	3	Updated: cover image and *Figure 1: "Internal schematic diagram"* Updated: *Section 3: "Test circuits"* Modified: *Section 4.1: "PowerFLAT 8x8 HV package information"* Minor text changes

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