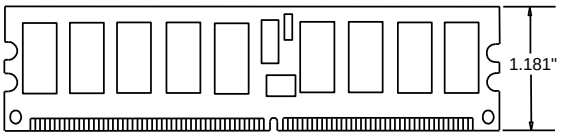
512MB - WD2RE512X809
1GB - WD2RE01GX809
2GB - WD2RE02GX809

Features:

- 240-pin Registered ECC DDR2 SDRAM Dual-In-Line Memory Module for DDR2-400,533,667 and 800.
- JEDEC standard VDD=1.8V (+/- 0.1V) power supply
- One rank 512MB, 1GB, and 2GB
- Modules are built with 9 x8 DDR2 SDRAM devices in a **FBGA 60-ball Pb-Free** package
- ECC error detection and correction
- Programmable CAS Latency of 3,4,5 and 6; Burst Length of 4 and 8
- Auto Refresh and Self Refresh Mode
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- SPD (Serial Presence Detect) with EEPROM
- All input/output are SSTL_18 compatible
- All contacts are gold plated
- One clock delay for register
- **ROHS compliant**

Figure 1: Available profiles

Standard:



Description:

The following specification covers the family of One-Rank Registered ECC DDR2 modules using x8 FBGA SDRAMs. Please reference Figure 1 for available profiles and the product ordering guide for available options including speed grade and silicon manufacturer.

Speed Grades:

Speed Grade	Data Rate (MHz)				Clock/Data Rate	Latency	Module Speed
	CL3	CL4	CL5	CL6			
-400C	400	-	-	-	5.0ns/400MHz	3-3-3	PC2-3200
-533E	400	533	-	-	3.75ns/533MHz	4-4-4	PC2-4200
-667G	-	-	667	-	3ns/667MHz	5-5-5	PC2-5300
-800G	-	-	800	-	2.5ns/800MHz	5-5-5	PC2-6400
-800I	-	-	-	800	2.5ns/800MHz	6-6-6	PC2-6400

Address Summary Table:

	512MB	1GB	2GB
Module Configuration	64M x 72	128M x 72	256M x 72
Refresh	8K	8K	8K
Device Configuration	64M x 8 (9 components)	128M x 8 (9 components)	256M x 8 (9 components)
Row Addressing	A0-A13(16K)	A0-A13(16K)	A0-A14 (32K)
Column Addressing	A0-A9 (1K)	A0-A9 (1K)	A0-A9 (1K)
Bank Address	BA0-BA2	BA0-BA2	BA0-BA2
Module Rank	1	1	1

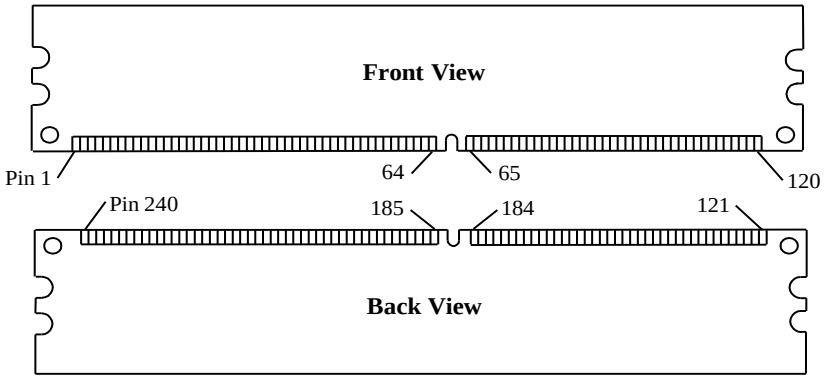
***Specifications are for reference purposes only and are subject to change by Wintec without notice.**

Pin Configuration:

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	31	DQ19	61	A4	91	VSS	121	VSS	151	VSS	181	VDDQ	211	DM5/DQS14
2	VSS	32	VSS	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC/DQS14#
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	VSS
4	DQ1	34	DQ25	64	VDD	94	VSS	124	VSS	154	VSS	184	VDD	214	DQ46
5	VSS	35	VSS	KEY		95	DQ42	125	DM0/DQS9	155	DM3/DQS12	KEY		215	DQ47
6	DQS0#	36	DQS3#	65	VSS	96	DQ43	126	NC/DQS9#	156	NC/DQS12#	185	CK0	216	VSS
7	DQS0	37	DQS3	66	VSS	97	VSS	127	VSS	157	VSS	186	CK0#	217	DQ52
8	VSS	38	VSS	67	VDD	98	DQ48	128	DQ6	158	DQ30	187	VDD	218	DQ53
9	DQ2	39	DQ26	68	PAR_IN	99	DQ49	129	DQ7	159	DQ31	188	A0	219	VSS
10	DQ3	40	DQ27	69	VDD	100	VSS	130	VSS	160	VSS	189	VDD	220	RFU
11	VSS	41	VSS	70	A10/AP	101	SA2	131	DQ12	161	CB4	190	BA1	221	RFU
12	DQ8	42	CB0	71	BA0	102	NC,TEST[1]	132	DQ13	162	CB5	191	VDDQ	222	VSS
13	DQ9	43	CB1	72	VDDQ	103	VSS	133	VSS	163	VSS	192	RAS#	223	DM6/DQS15
14	VSS	44	VSS	73	WE#	104	DQS6#	134	DM1/DQS10	164	DM8/DQS17	193	S0#	224	NC/DQS15#
15	DQS1#	45	DQS8#	74	CAS#	105	DQS6	135	NC/DQS10#	165	NC/DQS17#	194	VDDQ	225	VSS
16	DQS1	46	DQS8	75	VDDQ	106	VSS	136	VSS	166	VSS	195	ODT0	226	DQ54
17	VSS	47	VSS	76	NC/S1#	107	DQ50	137	RFU	167	CB6	196	A13	227	DQ55
18	RESET#	48	CB2	77	ODT1	108	DQ51	138	RFU	168	CB7	197	VDD	228	VSS
19	NC	49	CB3	78	VDDQ	109	VSS	139	VSS	169	VSS	198	VSS	229	DQ60
20	VSS	50	VSS	79	VSS	110	DQ56	140	DQ14	170	VDDQ	199	DQ36	230	DQ61
21	DQ10	51	VDDQ	80	DQ32	111	DQ57	141	DQ15	171	NC/CKE1	200	DQ37	231	VSS
22	DQ11	52	CKE0	81	DQ33	112	VSS	142	VSS	172	VDD	201	VSS	232	DM7/DQS16
23	VSS	53	VDD	82	VSS	113	DQS7#	143	DQ20	173	NC/A15	202	DM4/DQS13	233	NC/DQS16#
24	DQ16	54	BA2	83	DQS4#	114	DQS7	144	DQ21	174	NC/A14	203	NC/DQS13#	234	VSS
25	DQ17	55	ERR_OUT	84	DQS4	115	VSS	145	VSS	175	VDDQ	204	VSS	235	DQ62
26	VSS	56	VDDQ	85	VSS	116	DQ58	146	DM2/DQS11	176	A12	205	DQ38	236	DQ63
27	DQS2#	57	A11	86	DQ34	117	DQ59	147	NC/DQS11#	177	A9	206	DQ39	237	VSS
28	DQS2	58	A7	87	DQ35	118	VSS	148	VSS	178	VDD	207	VSS	238	VDDSPD
29	VSS	59	VDD	88	VSS	119	SDA	149	DQ22	179	A8	208	DQ44	239	SA0
30	DQ18	60	A5	89	DQ40	120	SCL	150	DQ23	180	A6	209	DQ45	240	SA1
				90	DQ41							210	VSS		

NC - No Connect, RFU - Reserved for Future Use
1. The Test pin (Pin 102) is reserved for bus analysis and is not connected on normal memory modules
2. CKE1 and S1# pin are used for dual-rank Registered DIMM
3. A13 (Pin 196) is for 512MB and above DIMM.

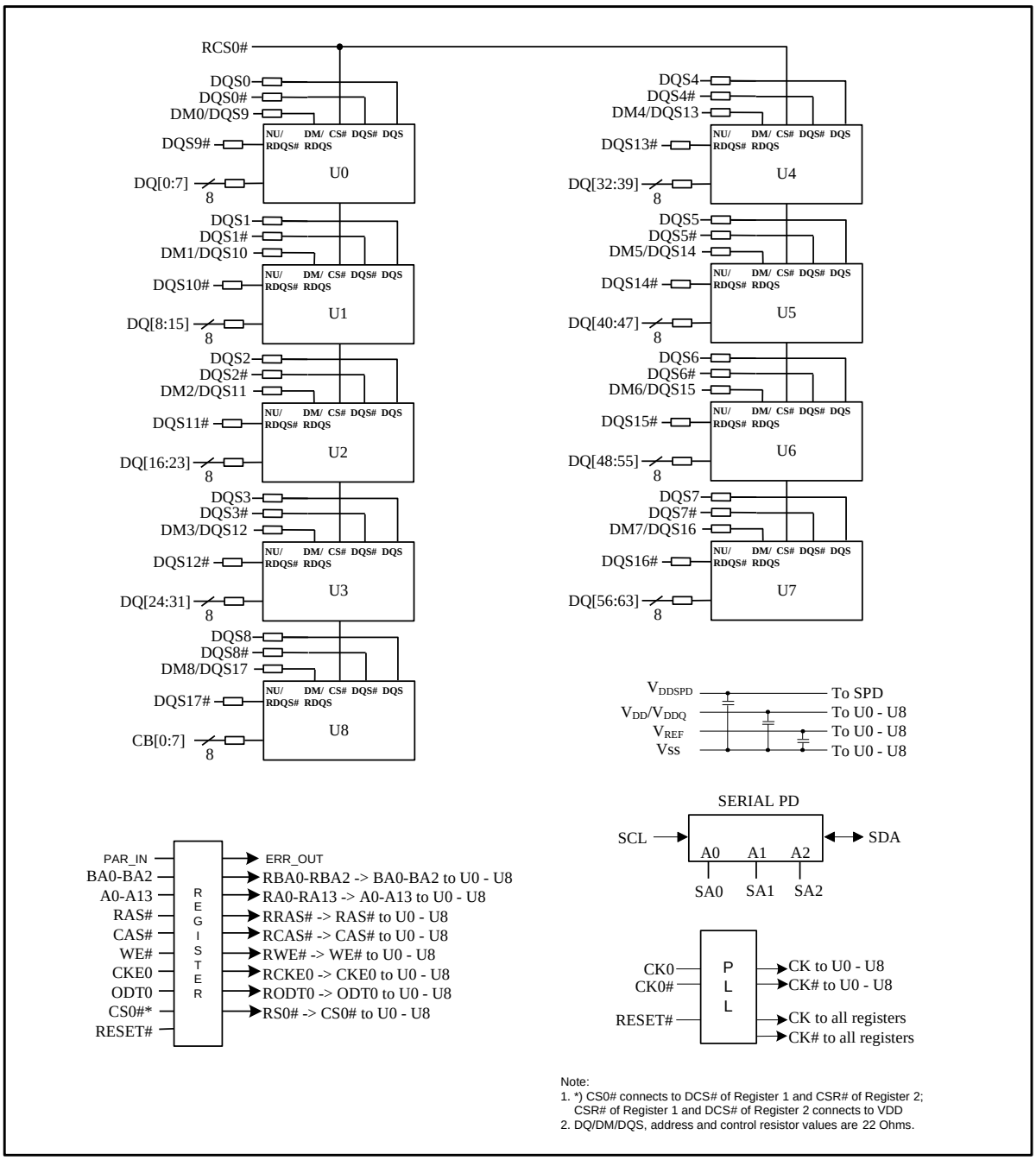
Pin Locations:



240-pin DIMM

Functional Block Diagram:

One Rank 64M x 72 (512MB), 128M x 72 (1GB), and 256M x 72 (2GB) DDR2 Registered SDRAM DIMM (x8 organization)



Absolute Maximum Ratings:

Exposure to stresses greater than these absolute maximum rating conditions for extended periods may affect reliability of the module.

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	-1.0	2.3	V
$V_{DD}Q$	$V_{DD}Q$ supply voltage relative to V_{SS}	-0.5	2.3	V
$V_{DD}L$	$V_{DD}L$ supply voltage relative to V_{SS}	-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5	2.3	V
T_{STG}	Storage temperature	-55	+100	°C
T_{OPR}	Operating Temperature (Ambient)	0	+70	°C
T_{CASE}	DRAM Component Case Temperature	0	+95	°C
I_{IL}	Input Leakage Current; Any input $0V \leq V_{IN} \leq 0.95V$	-5	5	µA
I_{OL}	Output Leakage Current; $0V \leq V_{OUT} \leq V_{DD}Q$; DQS and ODT are disabled	-5	5	µA

DC Operating Conditions:

Parameter	Symbol	Min	Nom	Max	Units	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.9	V	1
$V_{DD}L$ Supply Voltage	$V_{DD}L$	1.7	1.8	1.9	V	4
I/O Supply Voltage	$V_{DD}Q$	1.7	1.8	1.9	V	4
I/O Reference Voltage	V_{REF}	0.49 x $V_{DD}Q$	0.50 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	2
I/O Termination Voltage (system)	V_{TT}	V_{REF} - 40	V_{REF}	V_{REF} + 40	mV	3

NOTE:
1. V_{DD} and $V_{DD}Q$ must keep track of each other. $V_{DD}Q$ cannot exceed the value of V_{DD}
2. V_{REF} is expected to equal $V_{DD}Q/2$ of the transmitting device and to track variations in the DC level of the same
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}
4. $V_{DD}Q$ must tracks V_{DD}; and $V_{DD}L$ tracks V_{DD}

Electrical Characteristics and AC Timings:

V_{DD} = +1.8V ± 0.1V, $V_{DD}Q$ = +1.8V ± 0.1V, V_{REF} = V_{SS}, f =100MHz, 0°C≤T_{CASE} ≤+85°C, V_{OUT} (DC) = $V_{DD}Q/2$

Parameter	Symbol		-5 DDR2-400		-3.75 DDR2-533		-3 DDR2-667		-2.5 DDR2-800		Units
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
DQ output access time from *CK*/$\overline{CK}$	tAC		-600	+600	-500	+500	-450	+450	-400	+400	ps
DQS output access time from *CK*/$\overline{CK}$	tDQSCK		-500	+500	-450	+450	-400	+400	-350	+350	ps
CK high-level width	tCH		0.45	0.55	0.45	0.55	0.48	0.52	0.48	0.52	tCK
CK low-level width	tCL		0.45	0.55	0.45	0.55	0.48	0.52	0.48	0.52	tCK
CK half period	tHP		MIN (tCH, tCL)	-	MIN (tCH, tCL)	-	MIN (tCH, tCL)	-	min (tCH, tCL)	-	ps
Clock cycle time	tCK	CL=3	5,000	8,000	5,000	8,000	5,000	8,000	5,000	8,000	ps
		CL=4	5,000	8,000	3,750	8,000	3,750	8,000	3,750	8,000	ps
		CL=5	-	-	-	-	3,000	8,000	2,500	8,000	ps
		CL=6	-	-	-	-	-	-	2,500	8,000	ps
DQ and DM input hold time	tDH		275	-	225	-	175	-	125	-	ps
DQ and DM input setup time	tDS		150	-	100	-	100	-	50	-	ps
Control & Address input pulse width for each input	tIPW		0.6	-	0.6	-	0.6	-	0.6	-	tCK
DQ and DM input pulse width for each input	tDIPW		0.35	-	0.35	-	0.35	-	0.35	-	tCK
Data-out high-impedance time from *CK*/$\overline{CK}$	tHZ		-	tACmax	-	tACmax	-	tACmax	X		ps
Data-out low-impedance time from *CK*/$\overline{CK}$	tLZ		tACmin	tACmax	tACmin	tACmax	tACmin	tACmax	tACmin	tACmax	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ		-	350	-	300	-	240	x	200	ps
Data hold skew factor	tQHS		-	450	-	400	-	340	-	300	ps
Data output hold time from DQS	tQH		tHP-tQHS	-	tHP-tQHS	-		tHP-tQHS	tHP-tQHS	-	ps
Write command to 1st DQS latching transition	tDQSS		WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	tCK
DQS input low/high pulse width	tDQSL/H		0.35	-	0.35	-	0.35	-	0.35	-	tCK
DQS falling edge to CK setup time	tDSS		0.2	-	0.2	-	0.2	-	0.2	-	tCK
DQS falling edge hold time from CK	tDSH		0.2	-	0.2	-	0.2	-	0.2	-	tCK
Mode register set command cycle time	tMRD		2	-	2	-	2	-	2	-	tCK
Write preamble setup time	tWPRES		0	-	0	-	0	-	0	-	ps
Write preamble	tWPRE		0.25	-	0.25	-	0.35	-	0.35	-	tCK
Write postamble	tWPST		0.40	0.60	0.40	0.60	0.4	0.6	0.40	0.60	tCK
Read preamble	tRPRE		0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read postamble	tRPST		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Active to Precharge command	tRAS		45	70,000	45	70,000	45	70,000	45	70,000	ns
Active to Active command period	tRC		55	-	60	-	60	-	57.5/60	-	ns
Refresh to Refresh command interval	tRFC		105	-	105	-	105	-	105	-	ns
Active to Read/Write delay	tRCD		15	-	15	-	15	-	12.5/15	-	ns
Precharge command period	tRP		15	-	15		-	15	12.5/15	-	ns

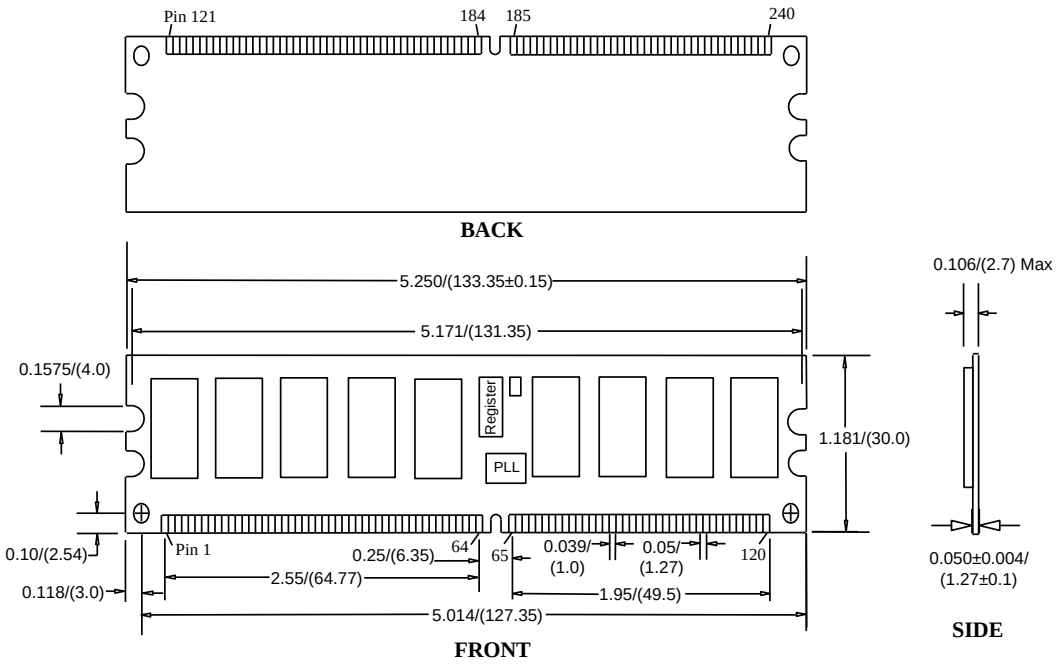
V_{DD} = +1.8V ± 0.1V, $V_{DD}Q$ = +1.8V ± 0.1V, V_{REF} = V_{SS}, f =100MHz, 0°C≤T_{CASE} ≤+85°C, V_{OUT} (DC) = $V_{DD}Q/2$

Parameter	Symbol	-5 DDR2-400		-3.75 DDR2-533		-3 DDR2-667		-2.5 DDR2-800		Units
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Active bank A to Active bank B command	tRRD	7.5	-	7.5	-	7.5	-	7.5	-	ns
$\overline{CAS}$ A to $\overline{CAS}$ B command period	tCCD	2		2		2	-	2	-	tCK
Write recovery time	tWR	15	-	15	-	15	-	15	-	ns
Auto Precharge write recovery + Precharge time	tDAL	WR+tRP	-	WR+tRP	-	WR+tRP	-	WR+tRP	-	tCK
Internal Write to Read command delay	tWTR	10	-	7.5	-	7.5	-	7.5	-	ns
Internal Read to Precharge command delay	tRTP	7.5	-	7.5	-	7.5	-	7.5	-	ns
Exit precharge power down to any non-Read command	tXP	2	-	2	-	2	-	2	-	tCK
Exit Self-Refresh to Read command	tXSRD	200	-	200	-	200	-	200	-	tCK
Exit Self-Refresh to non-Read command	tXSNR	tRFC+10	-	tRFC+10	-	tRFC+10	-	tRFC + 10	-	ns
CKE minimum high and low pulse width	tCKE	3	-	3	-	3	-	3	-	tCK
Average periodic refresh interval	tREFI	-	7.8	-	7.8	7.8	-	7.8	-	µs
OCD drive mode output delay	tOIT	0	12	0	12	0	12	0	12	ns
CKE low to *CK*, $\overline{CK}$ uncertainty	tDELAY	tIS+tCK +tIH	-	tIS+tCK +tIH	-	-	tIS+tCK +tIH	tIS+tCK +tIH	-	ns

Note: These parameters are applicable for all 3 chip manufacturers, Micron, Hynix, and Samsung.

Physical Dimensions – Standard:

1.181" Height DDR2 Registered DIMM
One physical rank, 9 components x8 organised



Note:
1. Dimensions are in inches/(mm)
2. Outline dimensions and tolerances are in accordance with the JEDEC standard

Ordering Guide:

DDR2-400, 533, 667, 800MHz, One-Rank x8, Registered ECC DIMM

WD2RE512X809
WD2RE01GX809
WD2RE02GX809

$$x - yyyy(j) - ZZZ$$

Naming Guide:

***x:* Profile**

(Blank)	= Std. (1.18")
V	= VLP. (0.72")

***yyyy:* Speed**

400C	= DDR2-400@CL3
533E	= DDR2-533@CL4
667G	= DDR2-667@CL5
800G	= DDR2-800@CL5
800I	= DDR2-800@CL6

***ZZZ:* DRAM/Die/Register**

(Blank)	= Std.		
C	= Hynix	A = A die	E = E die
P	= Samsung	B = B die	F = F die
H	= Micron	C = C die	G = G die
		D = D die	Q = Q die
I	= Inphi		
D	= IDT		

(Call for additional DRAM options and latest die-revision)

Configuration/Availability:

Density	PT #	Profile		Speed		DRAM/Die
512MB	WD2RE512X809	(Std), V	-	400C, 533E, 667G, 800G/I	-	*ZZZ*
1-GB	WD2RE01GX809	(Std), V		400C, 533E, 667G, 800G/I		
2-GB	WD2RE02GX809	(Std), V		400C, 533E, 667G, 800G/I		

Example: WD2RE01GX809-400C-QB
1GB DDR2-400 REG/ECC Infineon B-Die using 128Mx8 Config

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Revision History:

Revision 1.0 (December 2004)
- Initial Release

Revision 1.1 (August 2005)
- ROHS version
- Added DRAM Case temperature T_{CASE}

Revision 1.2 (Sept 2007)
- Added 800MHz speed grade

Revision 1.3 (Jan 2010)
- 1GB row address mapping updated

Revision 1.4 (Nov 2013)
- Updated the Ordering Guide

Revision 1.5 (Mar 2014)
- Updated the Ordering Guide