250 MHz, General Purpose Voltage Feedback Op Amps

AD8047/AD8048

FEATURES

Wide Bandwidth	AD8047, G = +1	AD8048, G = +2
Small Signal	250 MHz	260 MHz
Large Signal (2 V p-p)	130 MHz	160 MHz

5.8 mA Typical Supply Current
Low Distortion, (SFDR) Low Noise
- **–66 dBc Typ @ 5 MHz**
- **–54 dBc Typ @ 20 MHz**
- **5.2 nV/$\sqrt{Hz}$ (AD8047), 3.8 nV/$\sqrt{Hz}$ (AD8048) Noise**

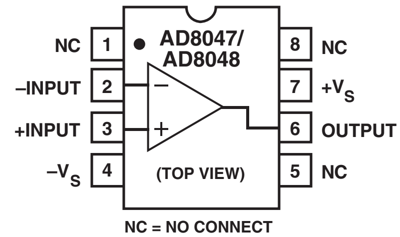
Drives 50 pF Capacitive Load
High Speed
- **Slew Rate 750 V/µs (AD8047), 1000 V/µs (AD8048)**
- **Settling 30 ns to 0.01%, 2 V Step**

±3 V to ±6 V Supply Operation

APPLICATIONS

Low Power ADC Input Driver
Differential Amplifiers
IF/RF Amplifiers
Pulse Amplifiers
Professional Video
DAC Current to Voltage Conversion
Baseband and Video Communications
Pin Diode Receivers
Active Filters/Integrators

FUNCTIONAL BLOCK DIAGRAM
8-Pin Plastic PDIP (N) and SOIC (R) Packages



PRODUCT DESCRIPTION

The AD8047 and AD8048 are very high speed and wide bandwidth amplifiers. The AD8047 is unity gain stable. The AD8048 is stable at gains of two or greater. The AD8047 and AD8048, which utilize a voltage feedback architecture, meet the requirements of many applications that previously depended on current feedback amplifiers.

A proprietary circuit has produced an amplifier that combines many of the best characteristics of both current feedback and voltage feedback amplifiers. For the power (6.6 mA max), the AD8047 and AD8048 exhibit fast and accurate pulse response (30 ns to 0.01%) as well as extremely wide small signal and large signal bandwidth and low distortion. The AD8047 achieves –54 dBc distortion at 20 MHz, 250 MHz small signal, and 130 MHz large signal bandwidths.

The AD8047 and AD8048's low distortion and cap load drive make the AD8047/AD8048 ideal for buffering high speed ADCs. They are suitable for 12-bit/10 MSPS or 8-bit/60 MSPS ADCs. Additionally, the balanced high impedance inputs of the voltage feedback architecture allow maximum flexibility when designing active filters.

The AD8047 and AD8048 are offered in industrial (–40°C to +85°C) temperature ranges and are available in 8-lead PDIP and SOIC packages.

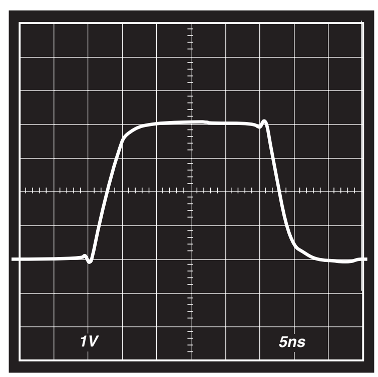


Figure 1. AD8047 Large Signal Transient Response, V_O = 4 V p-p, G = +1

REV. A

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AD8047/AD8048–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V, $R_{LOAD} = 100\ \Omega$, $A_V = 1$ (AD8047), $A_V = 2$ (AD8048), unless otherwise noted.)

Parameter	Conditions	AD8047A Min	AD8047A Typ	AD8047A Max	AD8048A Min	AD8048A Typ	AD8048A Max	Unit
DYNAMIC PERFORMANCE								
Bandwidth (–3 dB)								
Small Signal	$V_{OUT} \le 0.4$ V p-p	170	250		180	260		MHz
Large Signal[1]	$V_{OUT} = 2$ V p-p	100	130		135	160		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT} = 300$ mV p-p AD8047, $R_F = 0\ \Omega$; AD8048, $R_F = 200\ \Omega$		35			50		MHz
Slew Rate, Average +/–	$V_{OUT} = 4$ V Step	475	750		740	1000		V/µs
Rise/Fall Time	$V_{OUT} = 0.5$ V Step		1.1			1.2		ns
	$V_{OUT} = 4$ V Step		4.3			3.2		ns
Settling Time								
To 0.1%	$V_{OUT} = 2$ V Step		13			13		ns
To 0.01%	$V_{OUT} = 2$ V Step		30			30		ns
HARMONIC/NOISE PERFORMANCE								
Second Harmonic Distortion	2 V p-p; 20 MHz		–54			–48		dBc
	$R_L = 1$ kΩ		–64			–60		dBc
Third Harmonic Distortion	2 V p-p; 20 MHz		–60			–56		dBc
	$R_L = 1$ kΩ		–61			–65		dBc
Input Voltage Noise	f = 100 kHz		5.2			3.8		$nV/\sqrt{Hz}$
Input Current Noise	f = 100 kHz		1.0			1.0		$pA/\sqrt{Hz}$
Average Equivalent Integrated Input Noise Voltage	0.1 MHz to 10 MHz		16			11		µV rms
Differential Gain Error (3.58 MHz)	$R_L = 150\ \Omega$, G = +2		0.02			0.01		%
Differential Phase Error (3.58 MHz)	$R_L = 150\ \Omega$, G = +2		0.03			0.02		Degree
DC PERFORMANCE[2], $R_L = 150\ \Omega$								
Input Offset Voltage[3]			1	3		1	3	mV
	T_{MIN} to T_{MAX}			4			4	mV
Offset Voltage Drift			±5			±5		µV/°C
Input Bias Current			1	3.5		1	3.5	µA
	T_{MIN} to T_{MAX}			6.5			6.5	µA
Input Offset Current			0.5	2		0.5	2	µA
	T_{MIN} to T_{MAX}			3			3	µA
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5$ V	74	80		74	80		dB
Open-Loop Gain	$V_{OUT} = \pm 2.5$ V	58	62		65	68		dB
	T_{MIN} to T_{MAX}	54			56			dB
INPUT CHARACTERISTICS								
Input Resistance			500			500		kΩ
Input Capacitance			1.5			1.5		pF
Input Common-Mode Voltage Range			±3.4			±3.4		V
OUTPUT CHARACTERISTICS								
Output Voltage Range, $R_L = 150\ \Omega$		±2.8	±3.0		±2.8	±3.0		V
Output Current			50			50		mA
Output Resistance			0.2			0.2		Ω
Short-Circuit Current			130			130		mA
POWER SUPPLY								
Operating Range		±3.0	±5.0	±6.0	±3.0	±5.0	±6.0	V
Quiescent Current			5.8	6.6		5.9	6.6	mA
	T_{MIN} to T_{MAX}			7.5			7.5	mA
Power Supply Rejection Ratio		72	78		72	78		dB

NOTES
[1]See Absolute Maximum Ratings and Theory of Operation sections.
[2]Measured at $A_V = 50$.
[3]Measured with respect to the inverting input.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

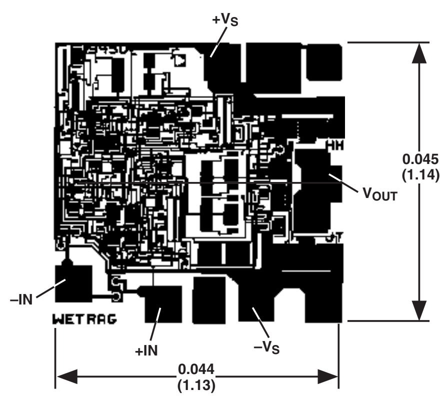
Supply Voltage, $(+V_S) - (-V_S)$ . . . . 12.6 V
Voltage Swing × Bandwidth Product
  AD8047 . . . . 180 V-MHz
  AD8048 . . . . 250 V-MHz
Internal Power Dissipation[2]
  Plastic Package (N) . . . . 1.3 W
  Small Outline Package (R) . . . . 0.9 W
Input Voltage (Common Mode) . . . . $\pm V_S$
Differential Input Voltage . . . . ±1.2 V
Output Short-Circuit Duration . . . . Observe Power Derating Curves
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . 300°C

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Specification is for device in free air: 8-Lead PDIP Package, θ_{JA} = 90°C/W; 8-Lead SOIC Package, θ_{JA} = 140°C/W

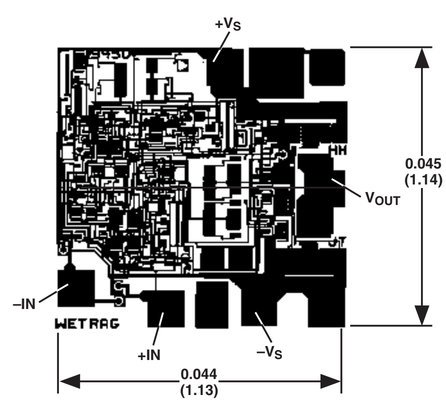
METALLIZATION PHOTOS

Dimensions shown in inches and (mm)
Connect Substrate to $-V_S$.

AD8047



AD8048



MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by these devices is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8047 and AD8048 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

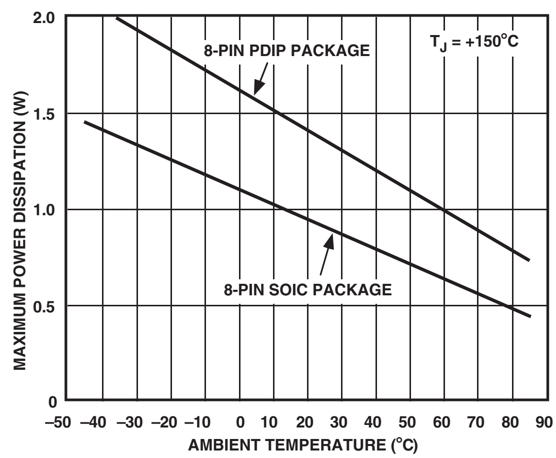


Figure 2. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

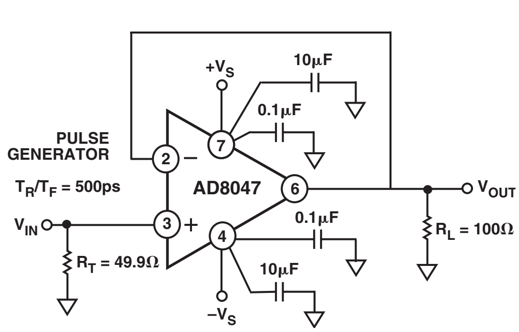
Model	Temperature Range	Package Description	Package Option*
AD8047AN	–40°C to +85°C	PDIP	N-8
AD8047AR	–40°C to +85°C	SOIC	R-8
AD8047AR-REEL	–40°C to +85°C	SOIC	R-8
AD8047AR-REEL7	–40°C to +85°C	SOIC	R-8
AD8048AN	–40°C to +85°C	PDIP	N-8
AD8048AR	–40°C to +85°C	SOIC	R-8
AD8048AR-REEL	–40°C to +85°C	SOIC	R-8
AD8048AR-REEL7	–40°C to +85°C	SOIC	R-8

*N = PDIP, R= SOIC

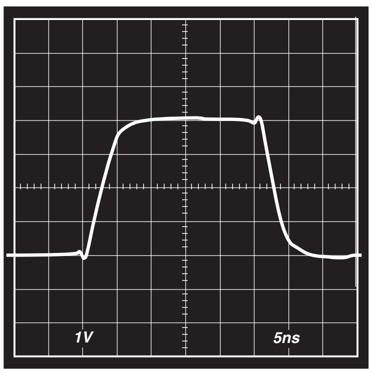
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8047/AD8048 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

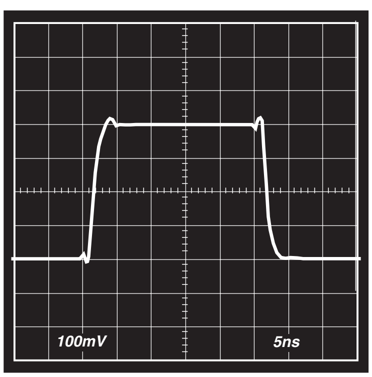
AD8047/AD8048–Typical Performance Characteristics



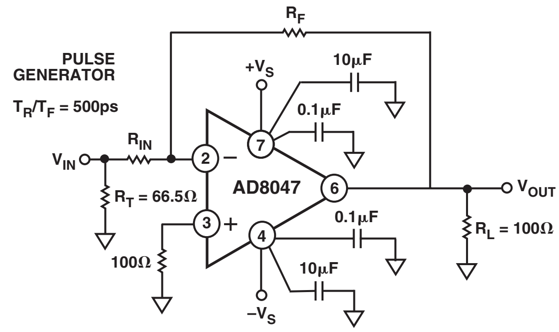
TPC 1. AD8047 Noninverting Configuration, G = +1



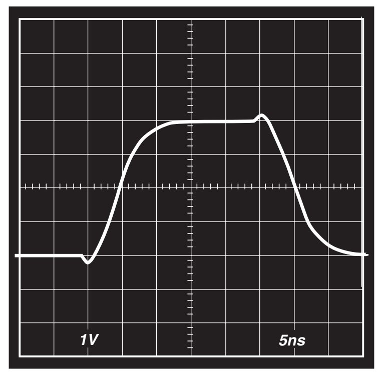
TPC 2. AD8047 Large Signal Transient Response; V_O = 4 V p-p, G = +1



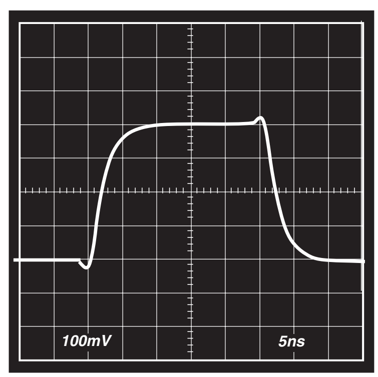
TPC 3. AD8047 Small Signal Transient Response; V_O = 400 mV p-p, G = +1



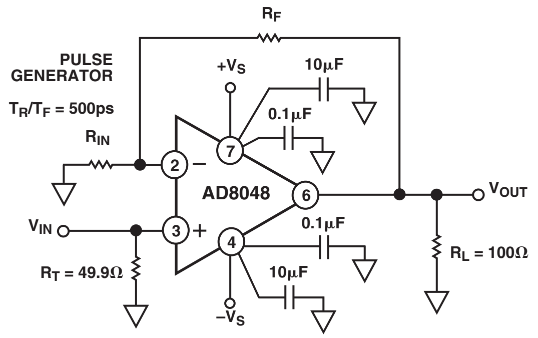
TPC 4. AD8047 Inverting Configuration, G = –1



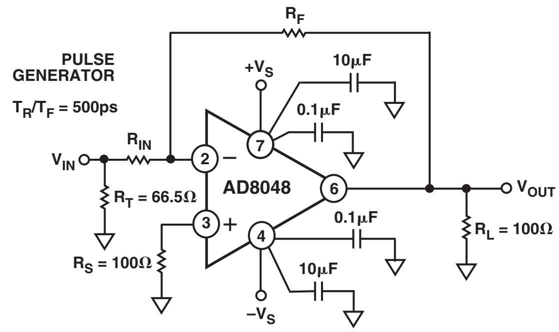
TPC 5. AD8047 Large Signal Transient Response; V_O = 4 V p-p, G = –1, $R_F = R_{IN}$ = 200 Ω



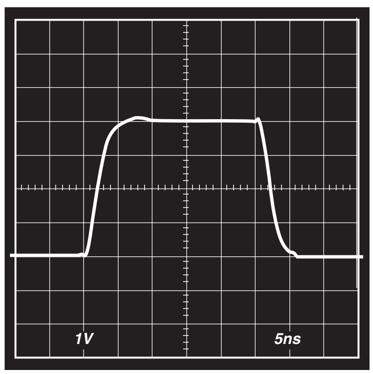
TPC 6. AD8047 Small Signal Transient Response; V_O = 400 mV p-p, G = –1, $R_F = R_{IN}$ = 200 Ω



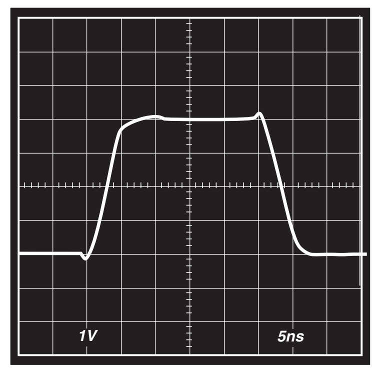
TPC 7. AD8048 Noninverting Configuration, G = +2



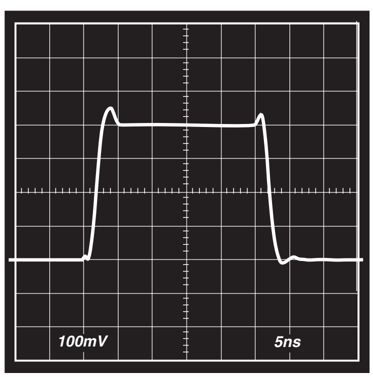
TPC 10. AD8048 Inverting Configuration, G= –1



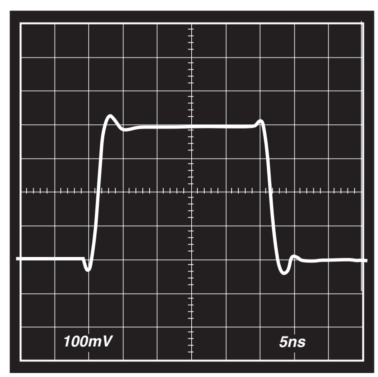
TPC 8. AD8048 Large Signal Transient Response; V_O = 4 V p-p, G = +2, $R_F = R_{IN}$ = 200 Ω



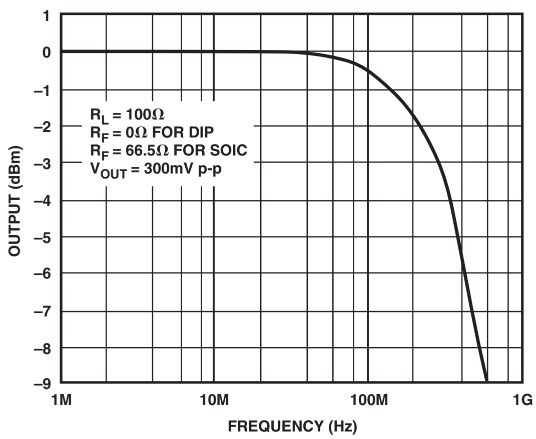
TPC 11. AD8048 Large Signal Transient Response; V_O = 4 V p-p, G = –1, $R_F = R_{IN}$ = 200 Ω



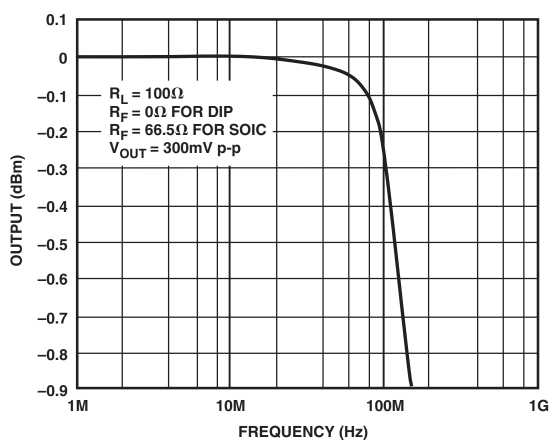
TPC 9. AD8048 Small Signal Transient Response; V_O = 400 mV p-p, G = +2, $R_F = R_{IN}$ = 200 Ω



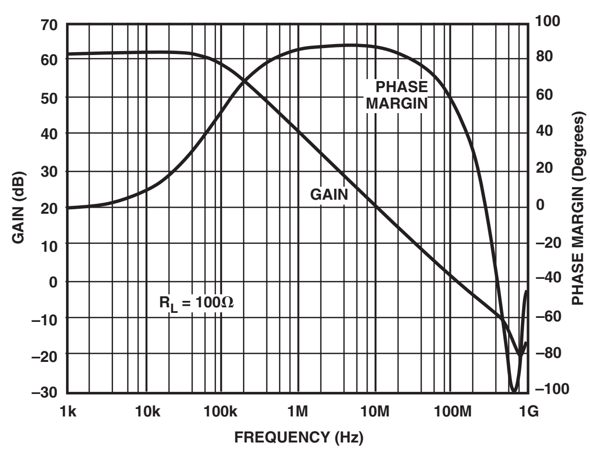
TPC 12. AD8048 Small Signal Transient Response; V_O = 400 mV p-p, G = –1, $R_F = R_{IN}$ = 200 Ω



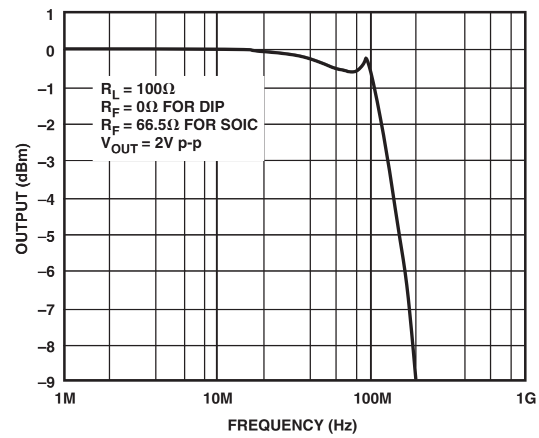
TPC 13. AD8047 Small Signal Frequency Response, G = +1



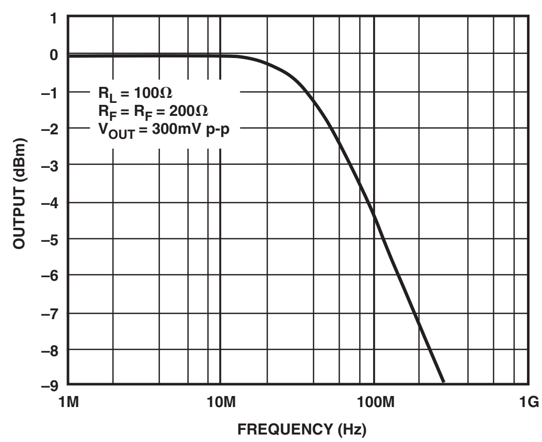
TPC 14. AD8047 0.1 dB Flatness, G = +1



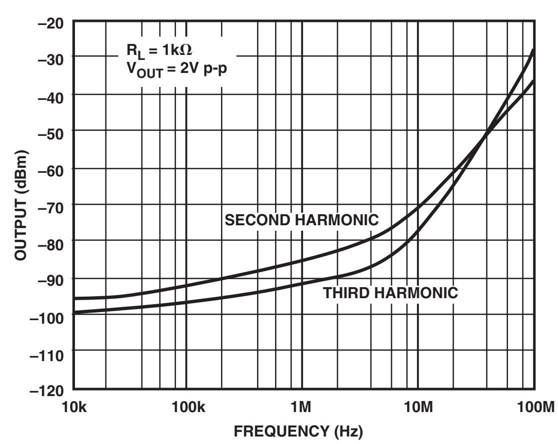
TPC 15. AD8047 Open-Loop Gain and Phase Margin vs. Frequency



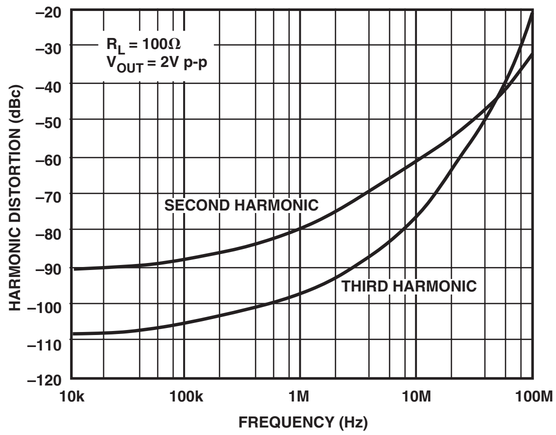
TPC 16. AD8047 Large Signal Frequency Response, G = +1



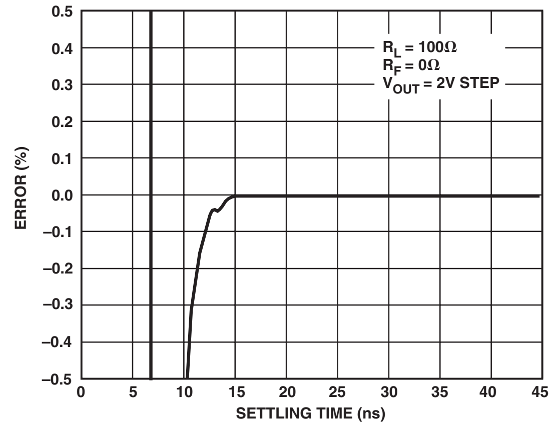
TPC 17. AD8047 Small Signal Frequency Response, G = –1



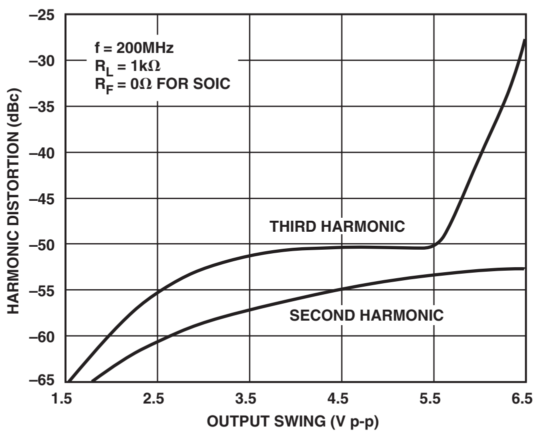
TPC 18. AD8047 Harmonic Distortion vs. Frequency, G = +1



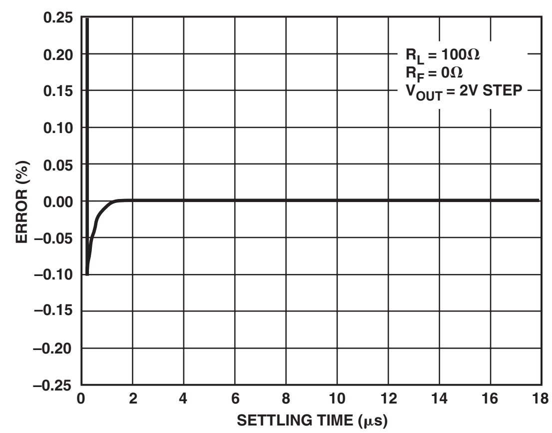
TPC 19. AD8047 Harmonic Distortion vs. Frequency, G = +1



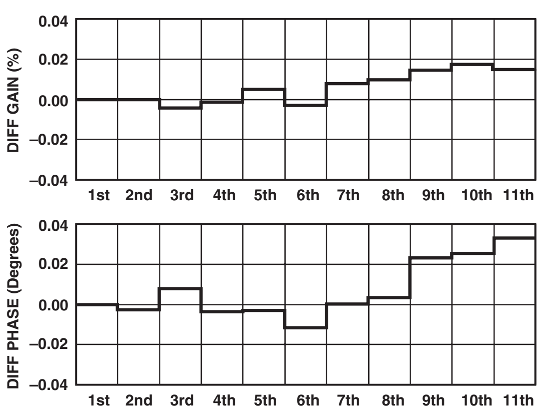
TPC 22. AD8047 Short-Term Settling Time, G = +1



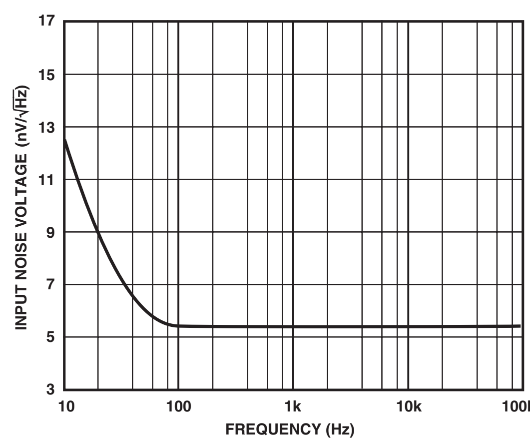
TPC 20. AD8047 Harmonic Distortion vs. Output Swing, G = +1



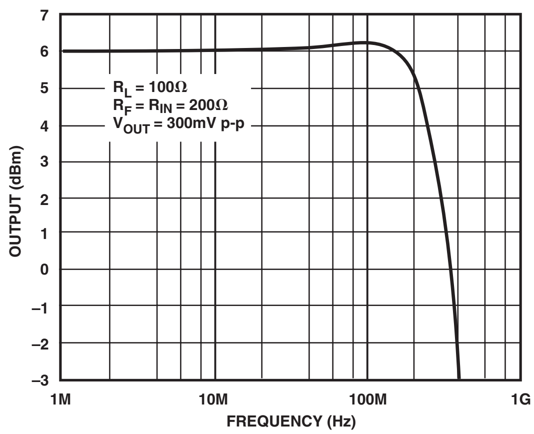
TPC 23. AD8047 Long-Term Settling Time, G = +1



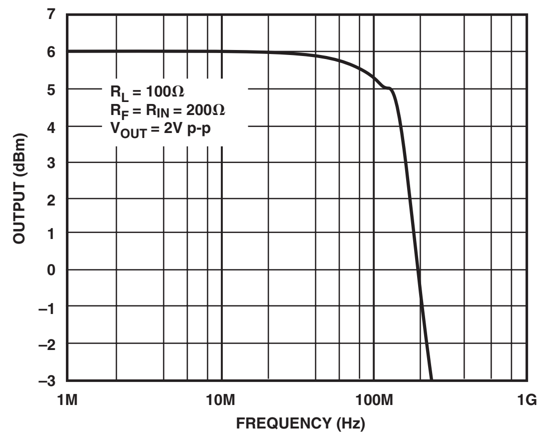
TPC 21. AD8047 Differential Gain and Phase Error, G = +2, $R_L = 150\ \Omega$, $R_F = 200\ \Omega$, $R_{IN} = 200\ \Omega$



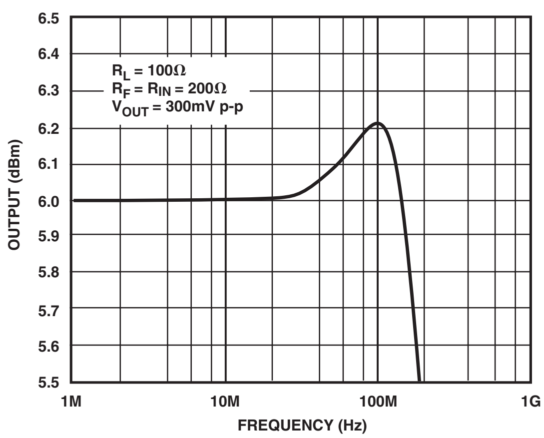
TPC 24. AD8047 Noise vs. Frequency



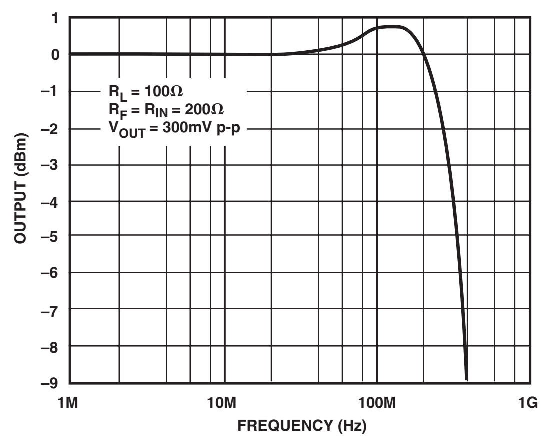
TPC 25. AD8048 Small Signal Frequency Response, G = +2



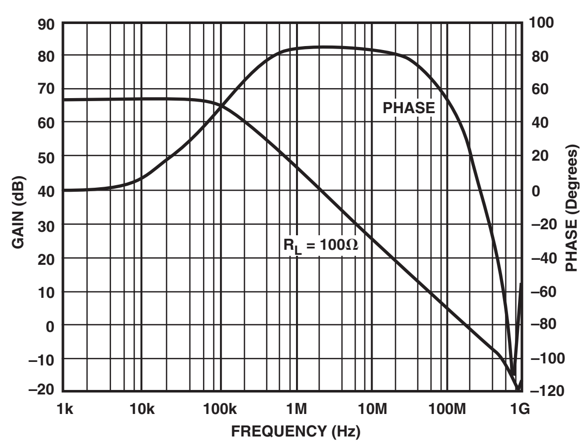
TPC 28. AD8048 Large Signal Frequency Response, G = +2



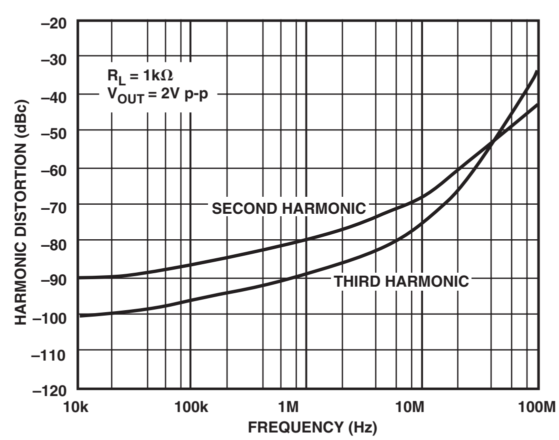
TPC 26. AD8048 0.1 dB Flatness, G = +2



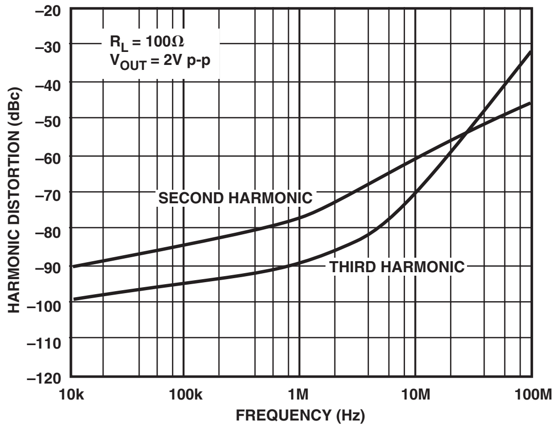
TPC 29. AD8048 Small Signal Frequency Response, G = –1



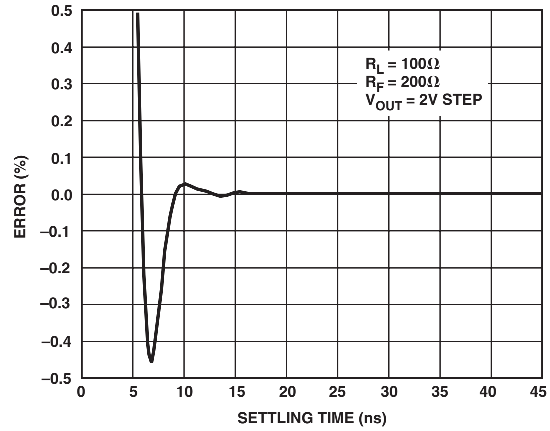
TPC 27. AD8048 Open-Loop Gain and Phase Margin vs. Frequency



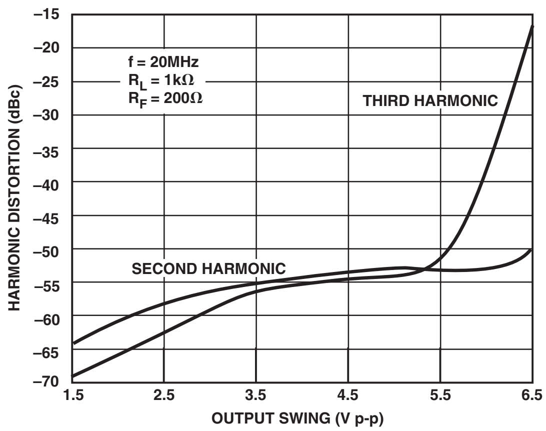
TPC 30. AD8048 Harmonic Distortion vs. Frequency, G = +2



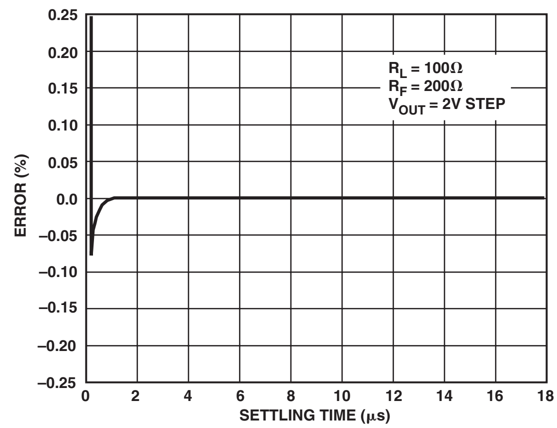
TPC 31. AD8048 Harmonic Distortion vs. Frequency, G = +2



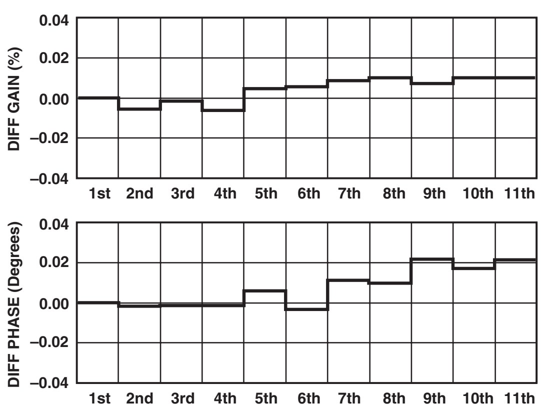
TPC 34. AD8048 Short-Term Settling Time, G = +2



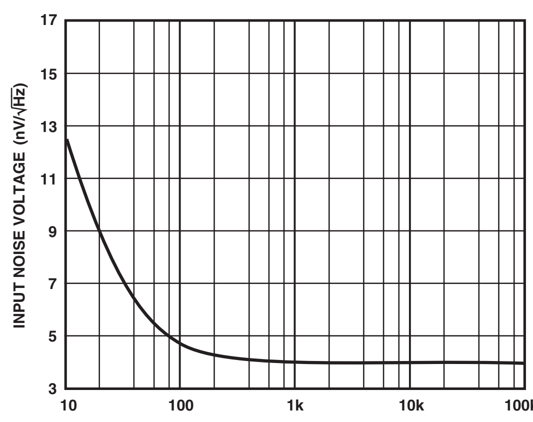
TPC 32. AD8048 Harmonic Distortion vs. Output Swing, G = +2



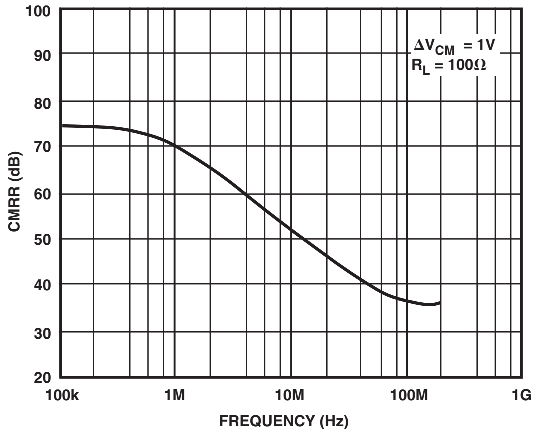
TPC 35. AD8048 Long-Term Settling Time 2 V Step, G = +2



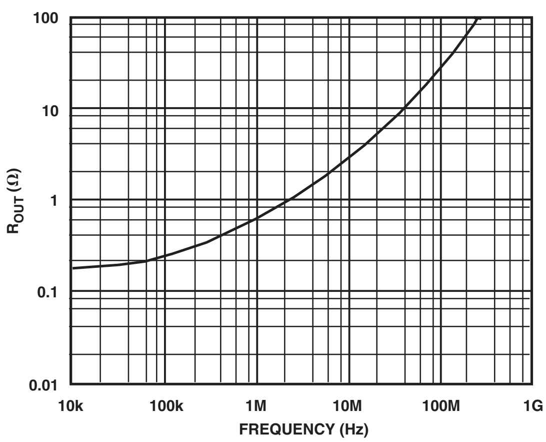
TPC 33. AD8048 Differential Gain and Phase Error, G = +2, R_L = 150 Ω, R_F = 200 Ω, R_{IN} = 200 Ω



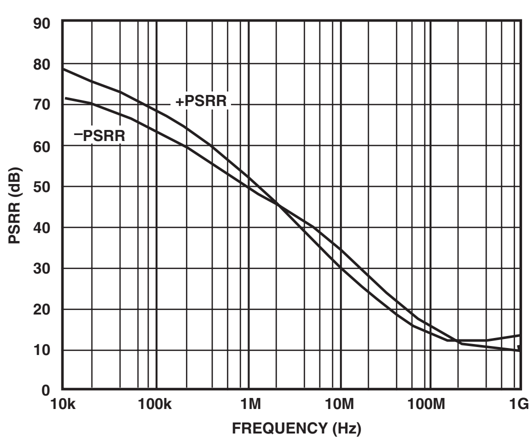
TPC 36. AD8048 Noise vs. Frequency



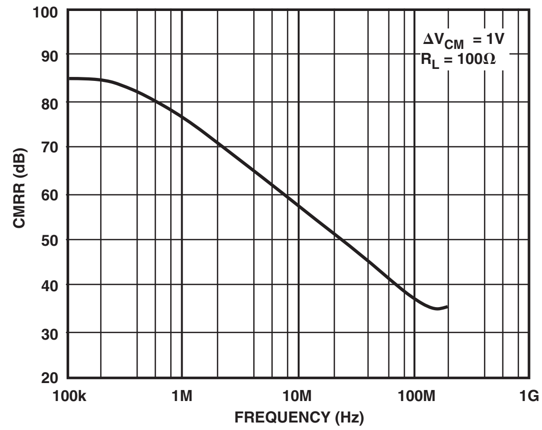
TPC 37. AD8047 CMRR vs. Frequency



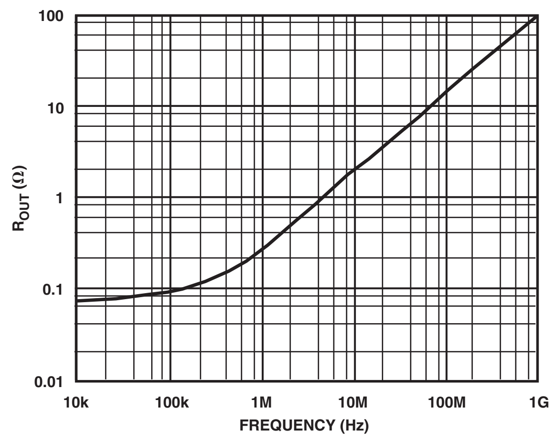
TPC 38. AD8047 Output Resistance vs. Frequency, G = +1



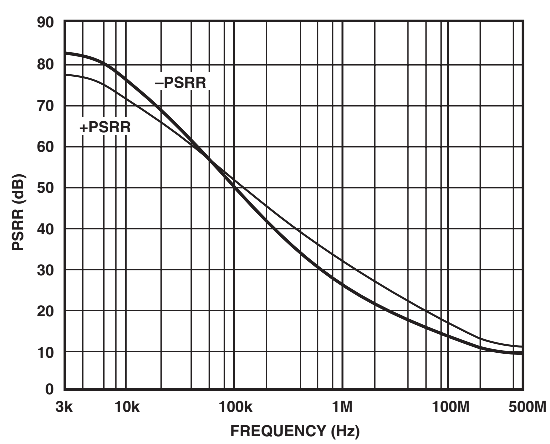
TPC 39. AD8047 PSRR vs. Frequency



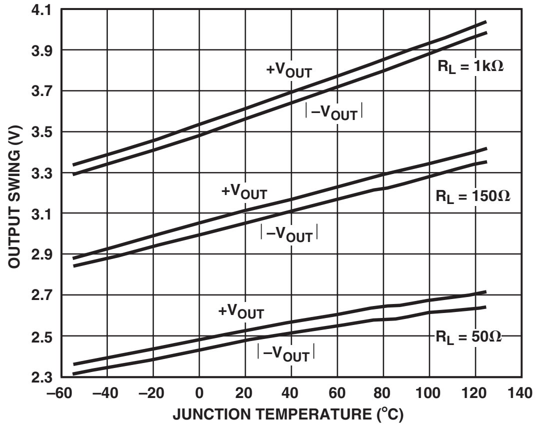
TPC 40. AD8048 CMRR vs. Frequency



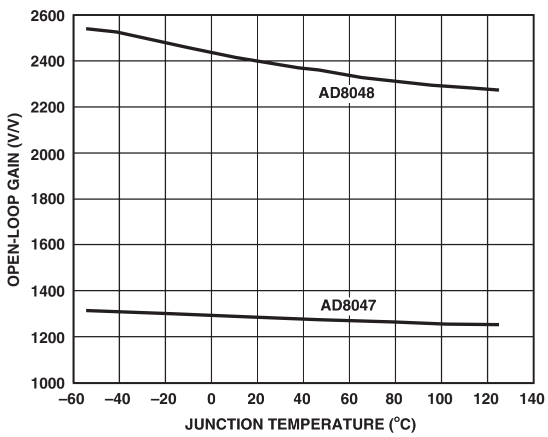
TPC 41. AD8048 Output Resistance vs. Frequency, G = +2



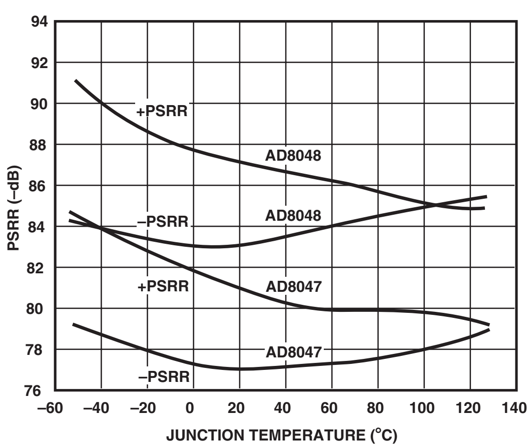
TPC 42. AD8048 PSRR vs. Frequency, G = +2



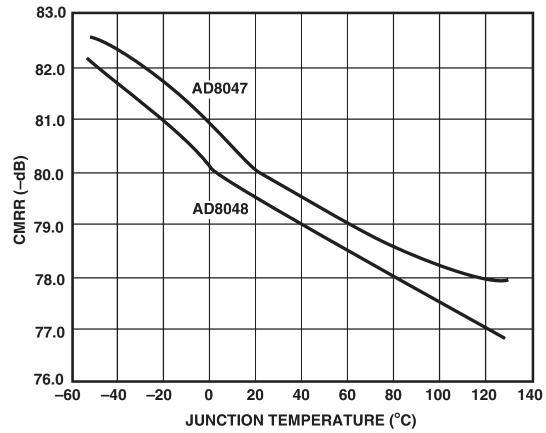
TPC 43. AD8047/AD8048 Output Swing vs. Temperature



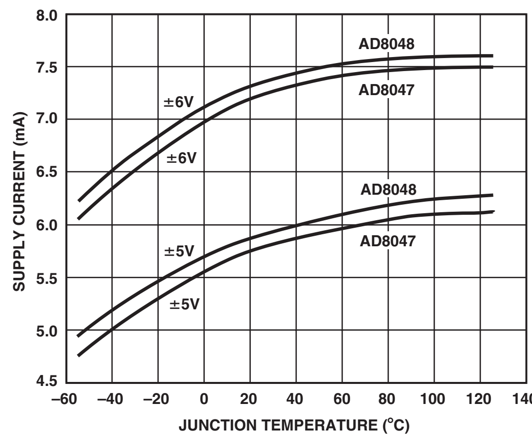
TPC 44. AD8047/AD8048 Open-Loop Gain vs. Temperature



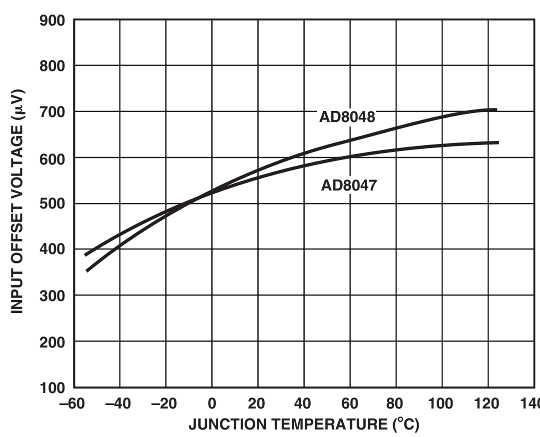
TPC 45. AD8047/AD8048 PSRR vs. Temperature



TPC 46. AD8047/AD8048 CMRR vs. Temperature



TPC 47. AD8047/AD8048 Supply Current vs. Temperature



TPC 48. AD8047/AD8048 Input Offset Voltage vs. Temperature

THEORY OF OPERATION

General

The AD8047 and AD8048 are wide bandwidth, voltage feedback amplifiers. Since their open-loop frequency response follows the conventional 6 dB/octave roll-off, their gain bandwidth product is basically constant. Increasing their closed-loop gain results in a corresponding decrease in small signal bandwidth. This can be observed by noting the bandwidth specification between the AD8047 (gain of 1) and AD8048 (gain of 2).

Feedback Resistor Choice

The value of the feedback resistor is critical for optimum performance on the AD8047 and AD8048. For maximum flatness at a gain of 2, R_F and R_G should be set to 200 Ω for the AD8048. When the AD8047 is configured as a unity gain follower, R_F should be set to 0 Ω (no feedback resistor should be used) for the plastic DIP and 66.5 Ω for the SOIC.

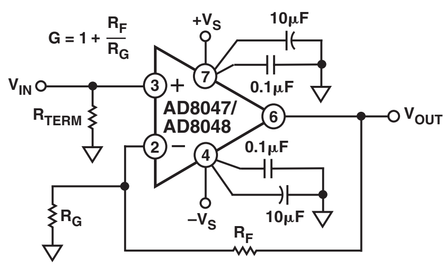


Figure 3. Noninverting Operation

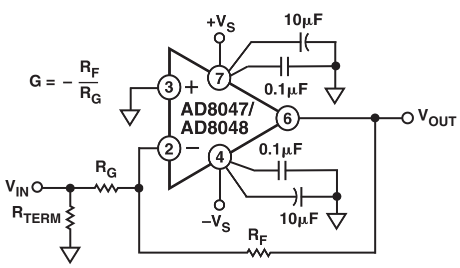


Figure 4. Inverting Operation

When the AD8047 is used in the transimpedance (I to V) mode, such as in photodiode detection, the values of R_F and diode capacitance (C_I) are usually known. Generally, the value of R_F selected will be in the kΩ range, and a shunt capacitor (C_F) across R_F will be required to maintain good amplifier stability. The value of C_F required to maintain optimal flatness (<1 dB peaking) and settling time can be estimated as

$$C_F \cong \left[(2\ \omega_O C_I R_F - 1)/\omega_O^{\ 2}\ R_F^{\ 2} \right]^{1/2}$$

where ω_O is equal to the unity gain bandwidth product of the amplifier in rad/sec, and C_I is the equivalent total input capacitance at the inverting input. Typically, $\omega_O = 800 \times 10^6$ rad/sec (see Open-Loop Frequency Response curve, TPC 15).

As an example, choosing R_F = 10 kΩ and C_I = 5 pF requires C_F to be 1.1 pF (Note: C_I includes both source and parasitic circuit capacitance). The bandwidth of the amplifier can be estimated using the C_F calculated as

$$f_{3\,dB} \cong \frac{1.6}{2\pi R_F C_F}$$

For general voltage gain applications, the amplifier bandwidth can be closely estimated as

$$f_{3\,dB} \cong \frac{\omega_O}{2\pi\left[1+\left(\dfrac{R_F}{R_G}\right)\right]}$$

This estimation loses accuracy for gains of +2/–1 or lower due to the amplifier's damping factor. For these low gain cases, the bandwidth will actually extend beyond the calculated value (see Closed-Loop BW plots, TPCs 13 and 25).

As a general rule, capacitor C_F will not be required if

$$(R_F \| R_G) \times C_I \le \frac{NG}{4\ \omega_O}$$

where NG is the Noise Gain ($1 + R_F/R_G$) of the circuit. For most voltage gain applications, this should be the case.

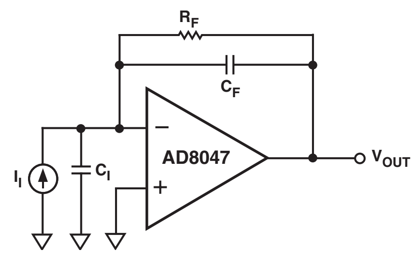


Figure 5. Transimpedance Configuration

Pulse Response

Unlike a traditional voltage feedback amplifier, where the slew speed is dictated by its front end dc quiescent current and gain bandwidth product, the AD8047 and AD8048 provide on demand current that increases proportionally to the input step signal amplitude. This results in slew rates (1000 V/µs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (1.0 pA/$\sqrt{\text{Hz}}$), gives the AD8047 and AD8048 the best attributes of both voltage and current feedback amplifiers.

Large Signal Performance

The outstanding large signal operation of the AD8047 and AD8048 is due to a unique, proprietary design architecture. In order to maintain this level of performance, the maximum 180 V-MHz product must be observed (e.g., @ 100 MHz, $V_O \le 1.8$ V p-p) on the AD8047 and the 250 V-MHz product must be observed on the AD8048.

Power Supply Bypassing

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 µF) will be required to provide the best settling time and lowest distortion. A parallel combination of at least 4.7 µF, and between 0.1 µF and 0.01 µF, is recommended. Some brands of electrolytic capacitors will require a small series damping resistor ≈4.7 Ω for optimum results.

Driving Capacitive Loads

The AD8047/AD8048 have excellent cap load drive capability for high speed op amps, as shown in Figures 7 and 9. However, when driving cap loads greater than 25 pF, the best frequency response is obtained by the addition of a small series resistance.

It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

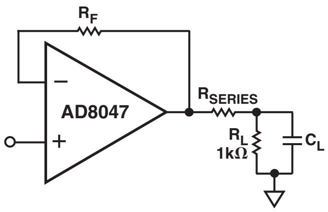


Figure 6. Driving Capacitive Loads

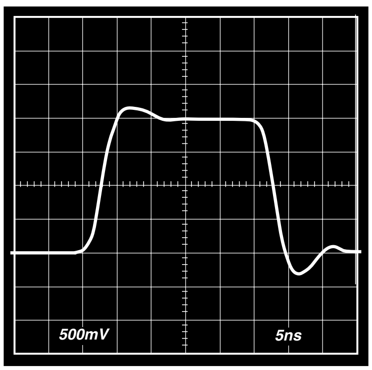


Figure 7. AD8047 Large Signal Transient Response; V_O = 2 V p-p, G = +1, R_F = 0 Ω, R_{SERIES} = 0 Ω, C_L = 27 pF

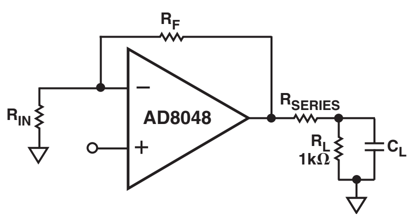


Figure 8. Driving Capacitive Loads

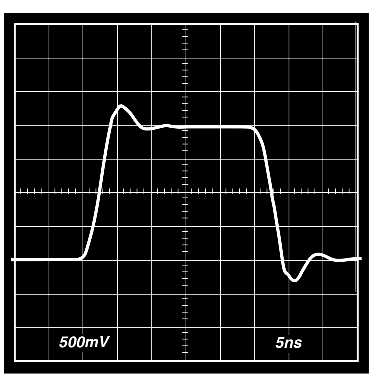


Figure 9. AD8048 Large Signal Transient Response; V_O = 2 V p-p, G = +2, R_F = R_{IN} = 200 Ω, R_{SERIES} = 0 Ω, C_L = 27 pF

APPLICATIONS

The AD8047 and AD8048 are voltage feedback amplifiers well suited for such applications as photodetectors, active filters, and log amplifiers. The devices' wide bandwidth (260 MHz), phase margin (65°), low noise current (1.0 pA/√Hz), and slew rate (1000 V/µs) give higher performance capabilities to these applications over previous voltage feedback designs.

With a settling time of 30 ns to 0.01% and 13 ns to 0.1%, the devices are an excellent choice for DAC I/V conversion. The same characteristics along with low harmonic distortion make them a good choice for ADC buffering/amplification. With superb linearity at relatively high signal frequencies, the AD8047 and AD8048 are ideal drivers for ADCs up to 12 bits.

Operation as a Video Line Driver

The AD8047 and AD8048 have been designed to offer outstanding performance as video line drivers. The important specifications of differential gain (0.01%) and differential phase (0.02°) meet the most exacting HDTV demands for driving video loads.

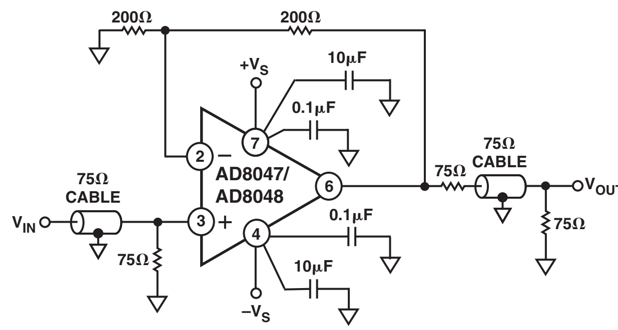


Figure 10. Video Line Driver

Active Filters

The wide bandwidth and low distortion of the AD8047 and AD8048 are ideal for the realization of higher bandwidth active filters. These characteristics, while being more common in many current feedback op amps, are offered in the AD8047 and AD8048 in a voltage feedback configuration. Many active filter configurations are not realizable with current feedback amplifiers.

A multiple feedback active filter requires a voltage feedback amplifier and is more demanding of op amp performance than other active filter configurations such as the Sallen-Key. In general, the amplifier should have a bandwidth that is at least 10 times the bandwidth of the filter if problems due to phase shift of the amplifier are to be avoided.

Figure 11 is an example of a 20 MHz low-pass multiple feedback active filter using an AD8048.

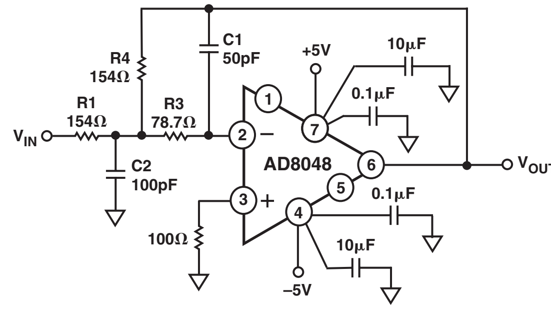


Figure 11. Active Filter Circuit

Choose

F_O = Cutoff Frequency = 20 MHz
α = Damping Ratio = 1/Q = 2
H = Absolute Value of Circuit Gain = $\left|\frac{-R4}{R1}\right| = 1$

Then,

$$k = 2\pi \ F_O \ C1$$

$$C2 = \frac{4\,C1\,(H+1)}{\alpha^2}$$

$$R1 = \frac{\alpha}{2\,HK}$$

$$R3 = \frac{\alpha}{2\,K\,(H+1)}$$

$$R4 = H(R1)$$

A/D Converter Driver

As A/D converters move toward higher speeds with higher resolutions, there becomes a need for high performance drivers that will not degrade the analog signal to the converter. It is desirable from a system's standpoint that the A/D be the element in the signal chain that ultimately limits overall distortion. This places new demands on the amplifiers used to drive fast, high resolution A/Ds.

With high bandwidth, low distortion, and fast settling time, the AD8047 and AD8048 make high performance A/D drivers for advanced converters. Figure 12 is an example of an AD8047 used as an input driver for an AD872A, a 12-bit, 10 MSPS A/D converter.

Layout Considerations

The specified high speed performance of the AD8047 and AD8048 requires careful attention to board layout and component selection. Proper RF design techniques and low-pass parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for the supply bypassing (see Figure 12). One end should be connected to the ground plane and the other within 1/8 inch of each power pin. An additional large (0.47 µF to 10 µF) tantalum electrolytic capacitor should be connected in parallel, though not necessarily so close, to the supply current for fast, large signal changes at the output.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

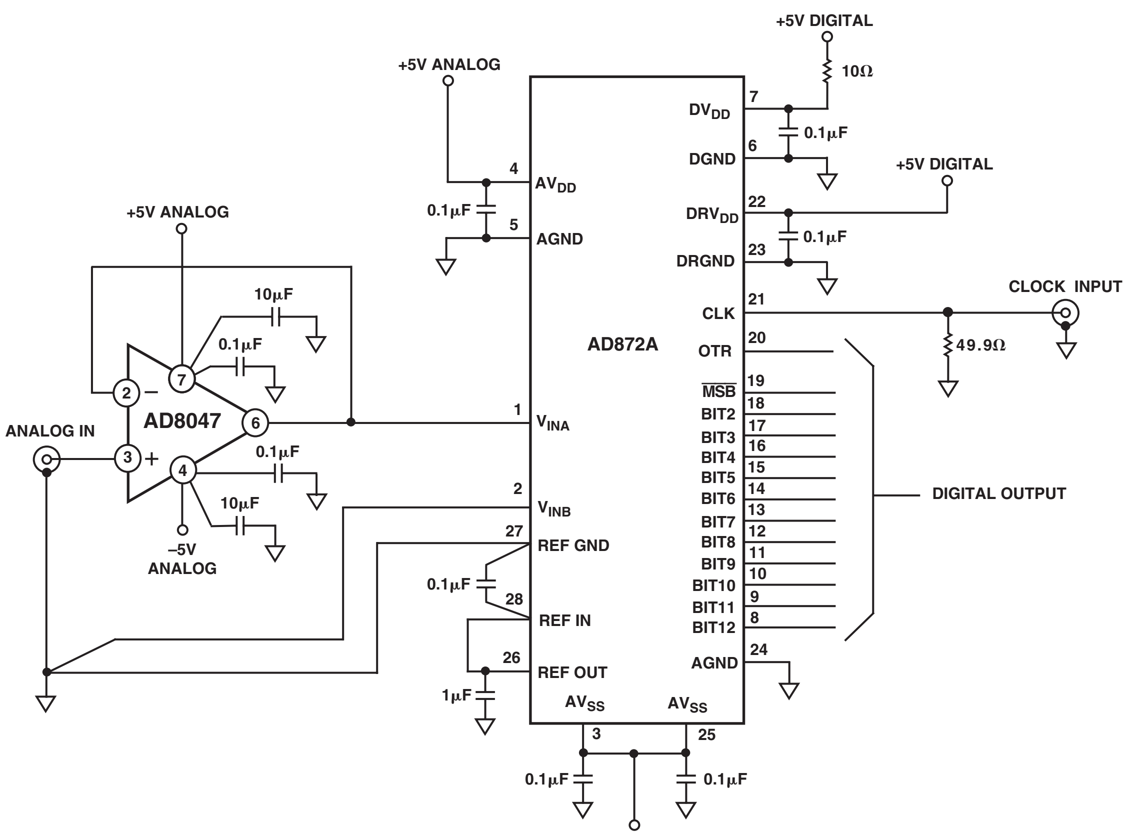
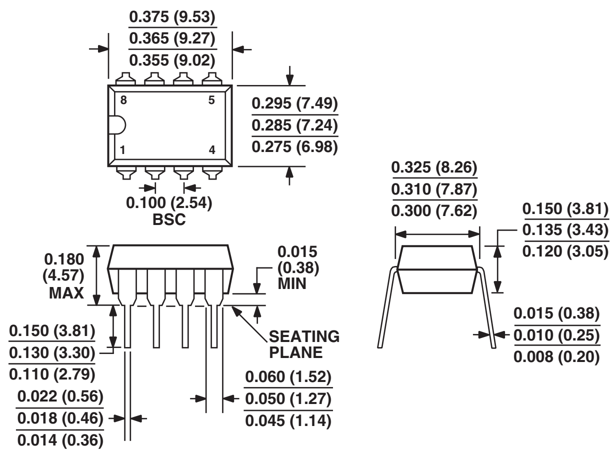


Figure 12. AD8047 Used as Driver for an AD872A, a 12-Bit, 10 MSPS A/D Converter

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP] (N-8)

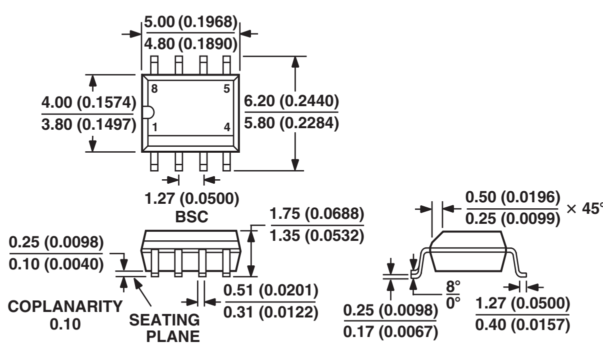
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC] (R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
7/03—Data Sheet changed from REV. 0 to REV. A.	
Renumbered Figures	Universal
Deleted Evaluation Board Information	Universal
Updated ORDERING GUIDE	3
Updated OUTLINE DIMENSIONS	15

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