DisplayPort VIP Output Board

Evaluation Board User Guide

FPGA-EB-02015-1.0

March 2018

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DP	DisplayPort
I^2C	Inter-Integrated Circuit
LDO	Low Dropout
LED	Light-emitting Diode
LVDS	Low-Voltage Differential Signaling
mDP	Mini DisplayPort
VIP	Video Interface Platform

1. Introduction

This document describes the Lattice Semiconductor DisplayPort® VIP Output Board. This board is designed to work with the Lattice Video Interface Platform (VIP) board interconnect system.

This user guide includes descriptions of board components, schematics, and bill of materials.

Key features of the DisplayPort VIP Output Board include:

- Integrated Texas Instruments SN75DP130 DisplayPort 1:1 Redriver
- Mini DisplayPort (mDP) connector
- Two 60-pin Rugged High-Speed Headers

Figure 1.1 shows the top view of the DisplayPort VIP Output Board and its key components. Figure 1.2 shows the bottom view of the board.

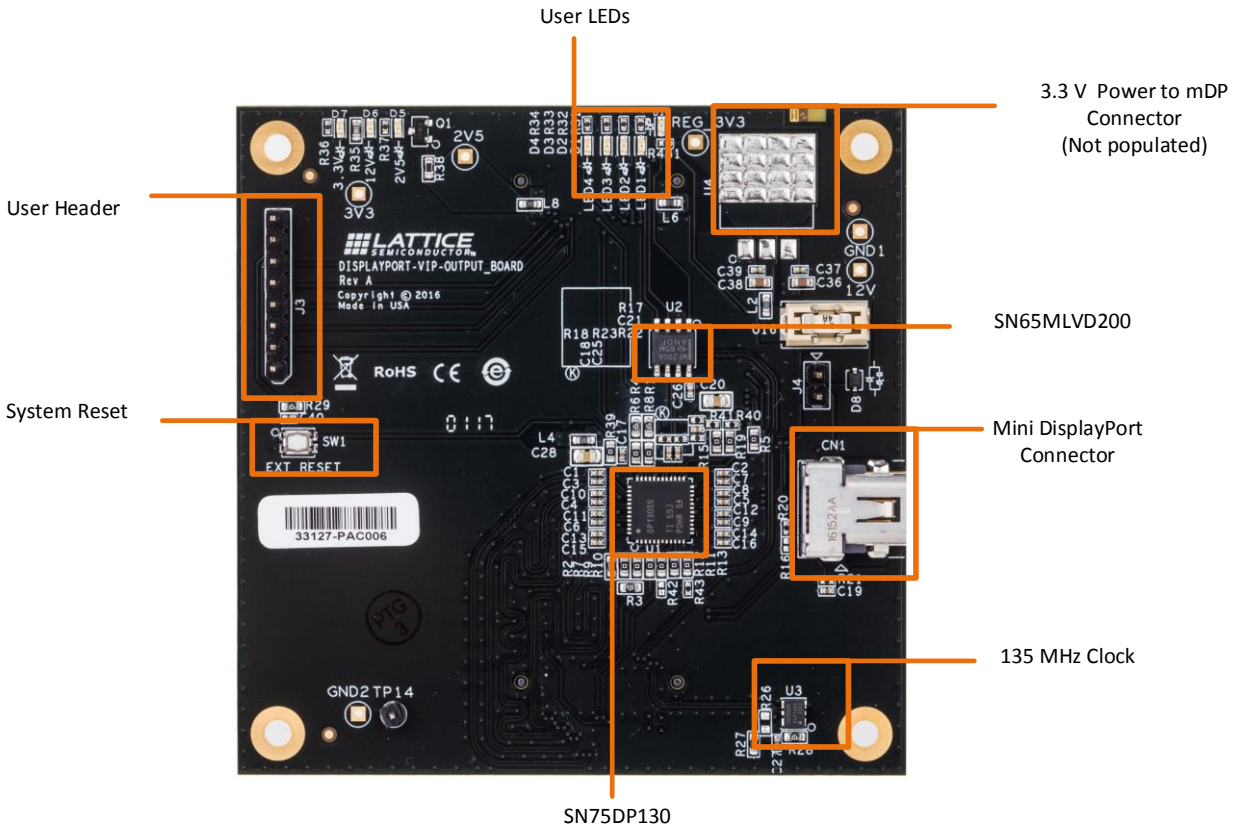


Figure 1.1. Top View of DisplayPort VIP Output Board

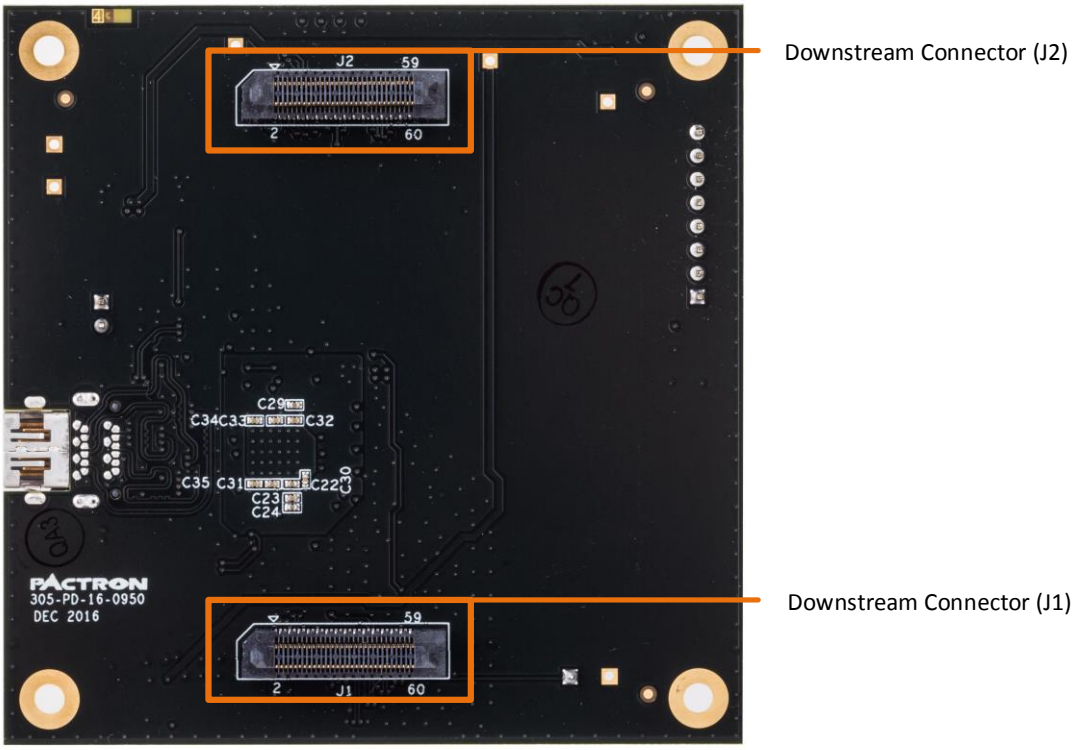


Figure 1.2. Bottom View of DisplayPort VIP Output Board

1.1. Further Information

The following references provide detailed information on the DisplayPort VIP Output Board:

- Appendix A. DisplayPort VIP Output Board Schematics
- Appendix B. DisplayPort VIP Output Board Bill of Materials
- For more information on boards and kits available for the VIP (Video Interface Platform) system visit www.latticesemi.com/boards
- For details on the Texas Instruments SN75DP130, visit the Texas Instruments website at www.ti.com

2. Functional Description

The DisplayPort VIP Output board receives up to 4-lanes of DisplayPort from the upstream processor board through connector J1. The DisplayPort Main Link, Control and Aux Channel are sent through the TI DisplayPort re-driver, which regenerates the DisplayPort high-speed digital link to the mini DisplayPort connector.

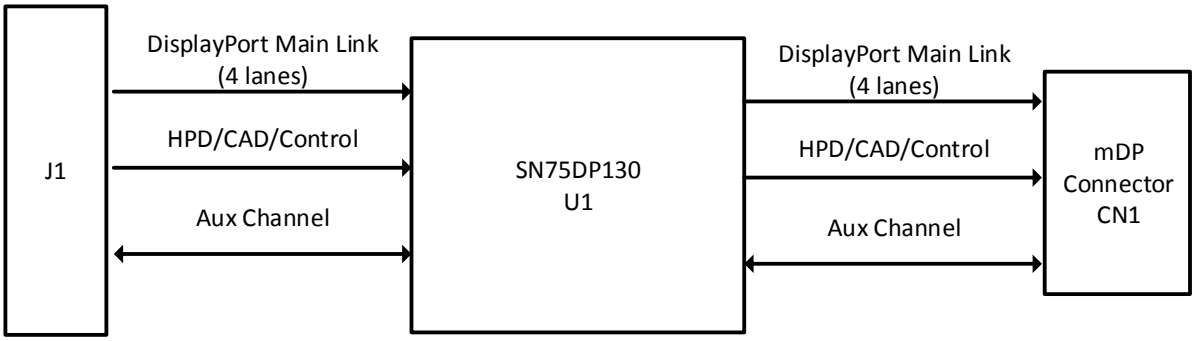


Figure 2.1 Functional Block Diagram

2.1. Switches

The push button switch, SW1, controls the reset signal RESET. Pressing SW1 provides logic 0 to the SN75DP130 RSTN pin. RESET is connected to GSRN on connecter J1, allowing SW1 to control the reset signal for other connected boards.

2.2. DisplayPort Interface

The mini DisplayPort connector, CN1, connects the DisplayPort VIP Output Board to a DisplayPort sink. If PWR Out is required on Pin 20, the user must populate the 3.3 V Low Dropout (LDO) regulator, U4, and short jumper J4.

2.3. LVDS Translator

The SN65MLV200 LVDS Driver/Receiver, U2, can be used to translate the LVDS AUX Channel to single ended I/O. This can be used if the upstream processor board is unable to receive LVDS. The single ended I/O are routed to connector J2.

2.4. Clock Interface

The 135 MHz LVDS clock, U3, can be used as a reference clock for the upstream processor board. This clock is routed to connector J1.

3. High-Speed Headers

The two 60-pin high-speed headers, connectors J1 and J2, are used to connect to an upstream host processor board.

Table 3.1. Connector J1

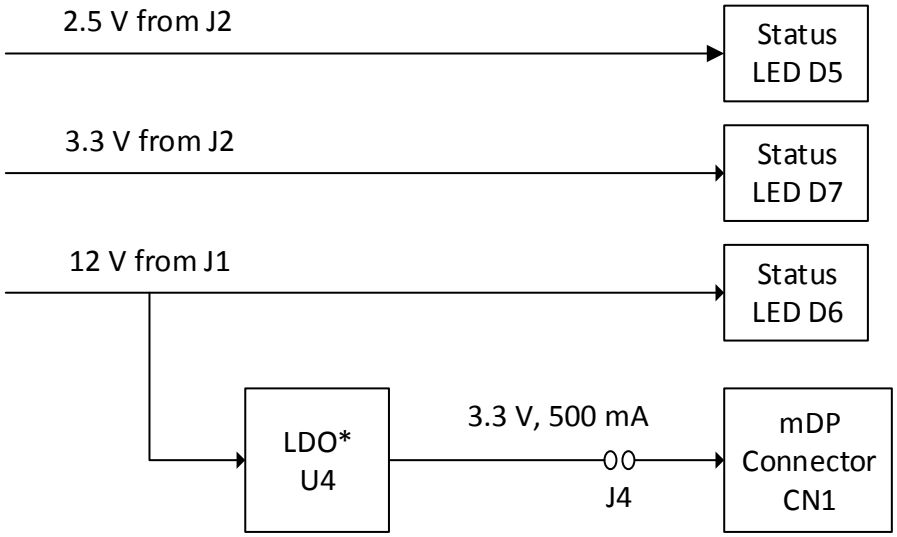
J1 Connector Pin	Signal Name	SN75DP130 pin	Description
1	GND	—	—
2	12V	—	—
3	CLK135_P	—	135 MHz LVDS Clock
4	12V	—	—
5	CLK135_N	—	135 MHz LVDS Clock
6	12V	—	—
7	GND	—	—
8	12V	—	—
9	AUX_P	AUX_SRCp	DisplayPort Auxiliary Data Channel
11	AUX_N	AUX_SRCn	DisplayPort Auxiliary Data Channel
13	GND	—	—
14	GND	—	—
19	GND	—	—
20	GND	—	—
26	GND	—	—
28	RESET	RSTN	Global System Reset
30	HPD_SRC	HPD_SRC	Hot Plug Detect
32	CAD_SRC	CAD_SRC	DP Cable Adapter Detect
34	GND	—	—
36	TXP0_D0CH0	IN0p	DisplayPort Main Link Lane 0
38	TXN0_D0CH0	IN0n	DisplayPort Main Link Lane 0
40	GND	—	—
41	SCL_CTL	SCL_CTL	I2C Interface to SN75DP130
42	TXP0_D0CH1	IN1p	DisplayPort Main Link Lane 1
43	SDA_CTL	SDA_CTL	I2C Interface to SN75DP130
44	TXN0_D0CH1	IN1n	DisplayPort Main Link Lane 1
46	GND	—	—
48	TXP0_D1CH0	IN2p	DisplayPort Main Link Lane 2
50	TXN0_D1CH0	IN2n	DisplayPort Main Link Lane 2
52	GND	—	—
54	TXP0_D1CH1	IN3p	DisplayPort Main Link Lane 3
55	GND	—	—
56	TXN0_D1CH1	IN3n	DisplayPort Main Link Lane 3
58	GND	—	—
60	TP14	—	—
10, 12, 15, 16, 17, 18, 21, 22, 23, 24, 25, 27, 29, 31, 33, 35, 37, 39, 45, 47, 49, 51, 53, 57, 59	Not Connected	—	—

Table 3.2. Connector J2

J1 Connector Pin	Signal Name	SN75DP130 pin	Description
1	3.3V	—	—
2	3.3V	—	—
3	3.3V	—	—
4	3.3V	—	—
7	AUX_EN	—	Aux Channel Translator Enable
8	LED1	—	User LED
9	AUX_OUT	—	Aux Channel single ended Out
10	LED2	—	User LED
11	AUX_IN	—	Aux Channel single ended In
12	LED3	—	User LED
13	EN	EN	SN75DP130 Enable
14	LED4	—	User LED
20	GND	—	—
21	GND	—	—
30	SDA_DDC	SDA_DDC	I2C Display Data Channel
32	SCL_DDC	SCL_DDC	I2C Display Data Channel
39	GND	—	—
40	GND	—	—
44	HEADER1	—	User I/O Header J3
46	HEADER2	—	User I/O Header J3
48	HEADER3	—	User I/O Header J3
50	HEADER4	—	User I/O Header J3
52	HEADER5	—	User I/O Header J3
53	GND	—	—
55	GND	—	—
56	GND	—	—
57	2.5V	—	—
58	2.5V	—	—
59	2.5V	—	—
60	2.5V	—	—
5, 6, 15, 16, 17, 18, 19, 22, 23, 24, 25, 26, 27, 28, 29, 31, 33, 34, 35, 36, 37, 38, 41, 42, 43, 45, 47, 49, 51, 54	Not Connected	—	—

4. Power Supply

Board power is supplied through connectors J1 and J2. Figure 4.1 shows the power distribution scheme. To provide power to the mini DisplayPort connector, install a 5.0 V to 3.3 V LDO at U4 and add shunt to jumper J4.



* Not Installed

Figure 4.1 Power Supply

5. User LEDs and Headers

Four discrete LEDs (light-emitting diodes) are available to the user. These are driven by the upstream processor board through connector J2.

Table 5.1 User LEDs

Signal	LED #	Connector J2 Pin	Color
LED1	D1	8	Green
LED2	D2	10	Green
LED3	D3	12	Green
LED4	D4	14	Green

An 8-pin 100-mil header, J3, is available to the user. There are five user connections routed to the upstream connector J2.

Table 5.2 User Header

Signal	Header J3 Pin	Connector J2 Pin
3V3	1	—
HEADER1	2	44
HEADER2	3	46
HEADER3	4	48
HEADER4	5	50
HEADER5	6	52
RESET	7	—
GND	8	—

6. Ordering Information

Please visit www.latticesemi.com/boards for the latest ordering information.

Table 6.1. Reference Part Number

Description	Ordering Part Number
DisplayPort VIP Output Board	DP-VIP-O-EVN

References

For more information, refer to

- Lattice Embedded Vision Development Kit User Guide (FPGA-UG-02015)
- ECP5 VIP Processing Board (FPGA-EB-02001)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Appendix A. DisplayPort VIP Output Board Schematics

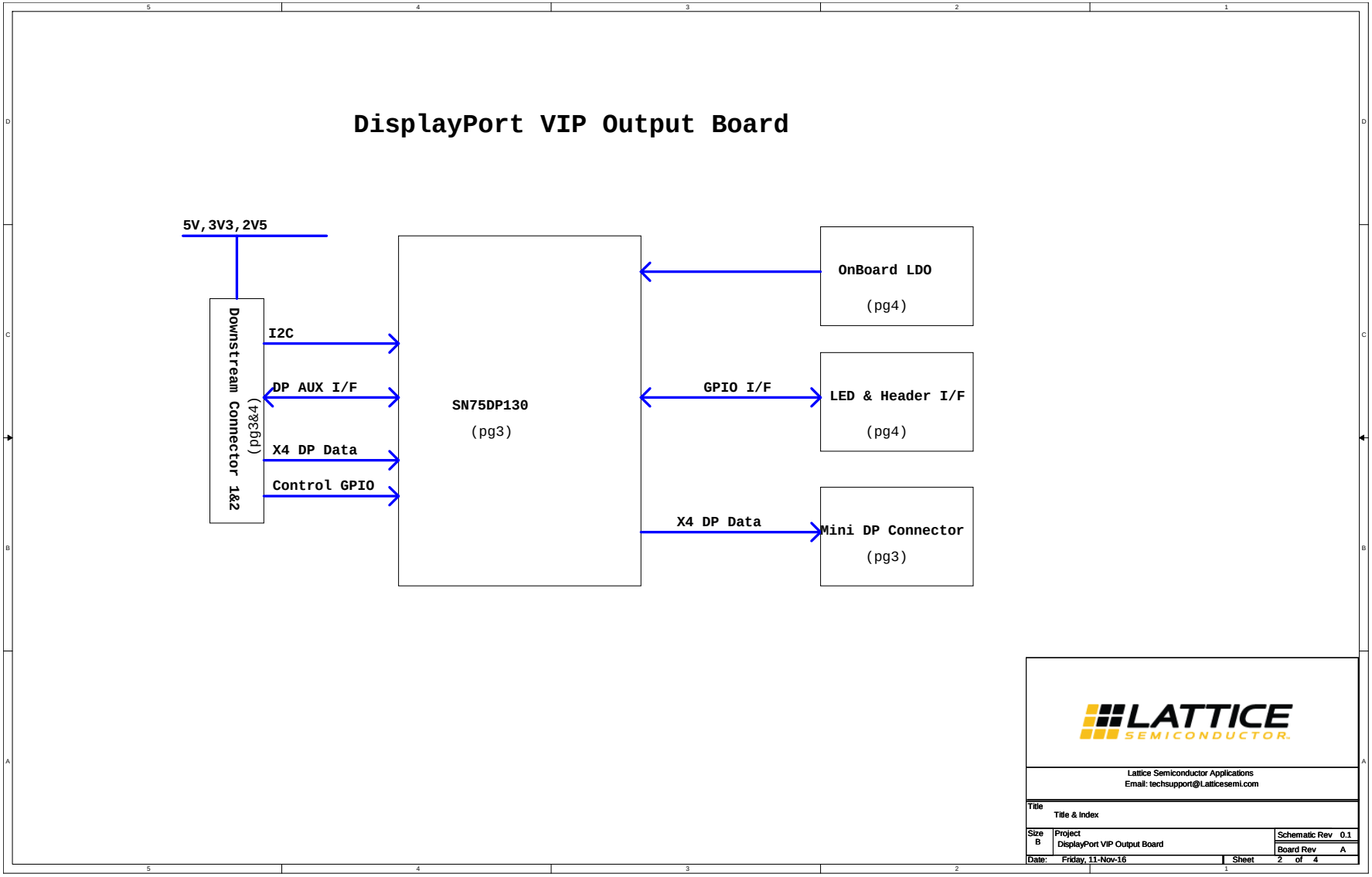


Figure A.1. Block Diagram

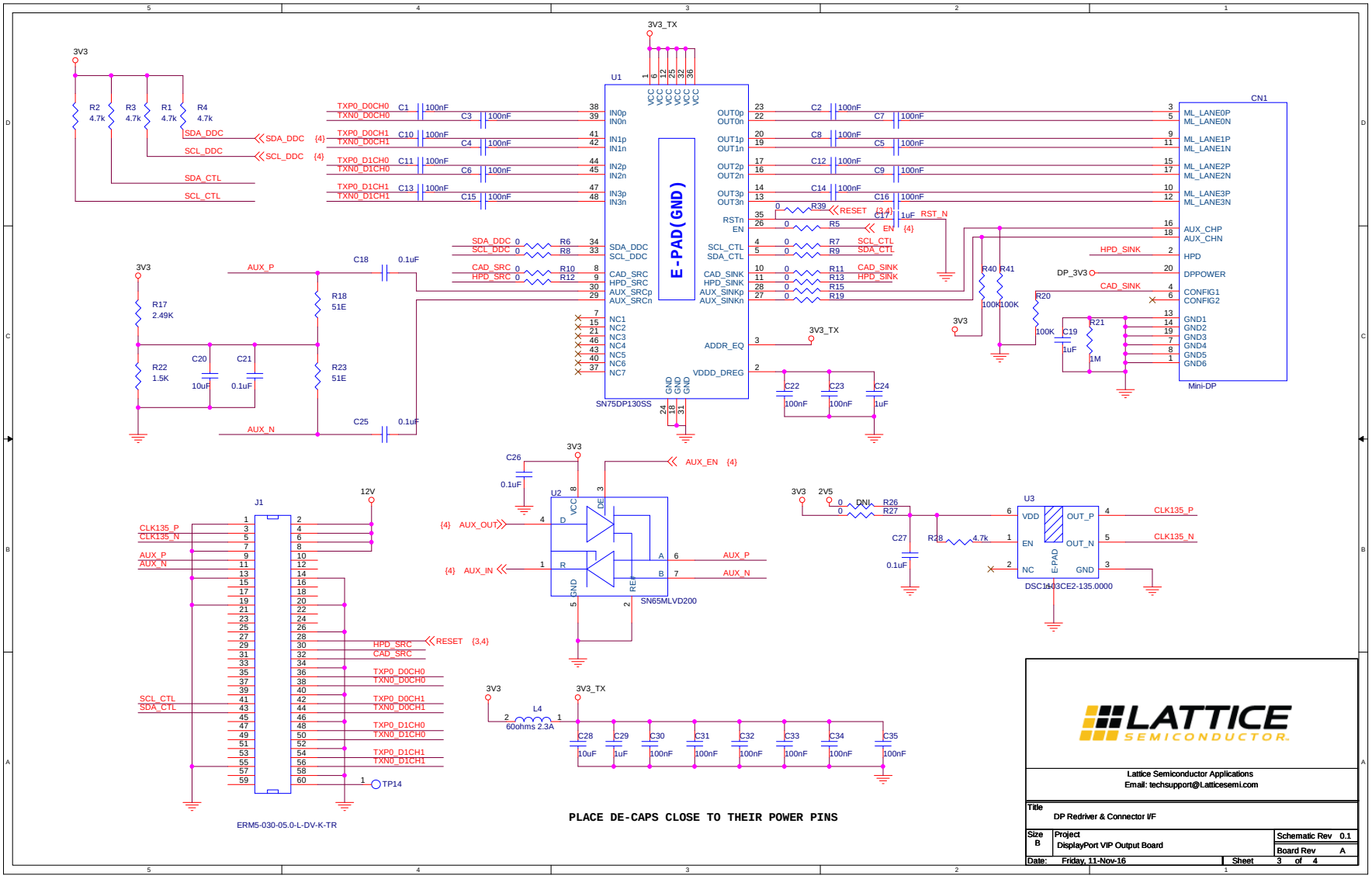


Figure A.2. DP Redriver and Connector I/F

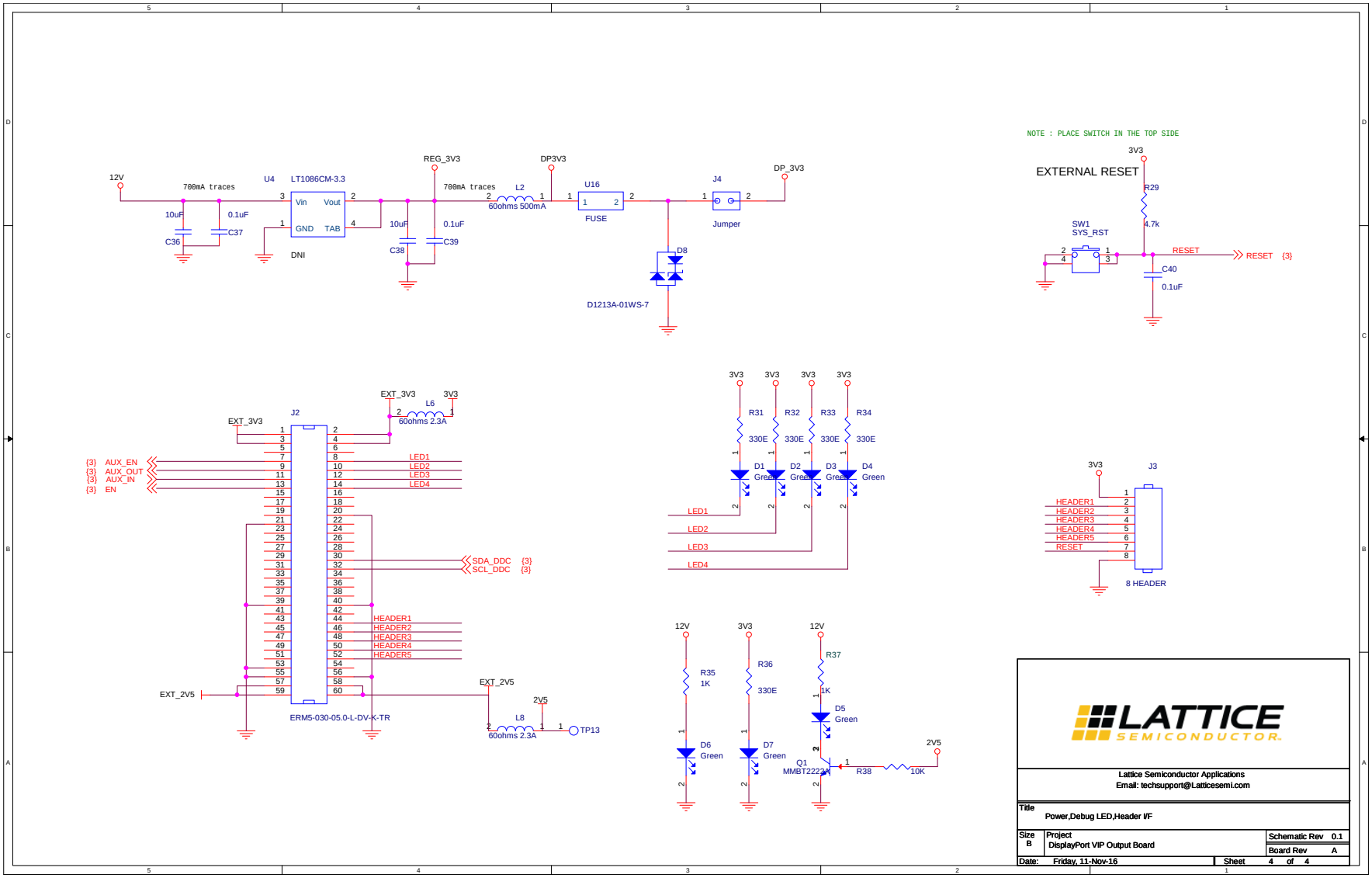


Figure A.3. Power, Debug LED, Header I/F

Appendix B. DisplayPort VIP Output Board Bill of Materials

Item	Reference	Qty	Value	Comments	Part Number	Manufacturer	Description
1	CN1	1	Mini-DP	—	2129320-3	TE Connectivity	MINI DISPLAYPORT REVERSE OFFSET
2	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11,C12,C13,C14, C15,C16	16	100 nF	—	885012205018	Wurth	CAP CER 0.1UF 10V X7R 0402
3	C17,C19,C24,C29	4	1 uF	—	GRM155R61A105KE15 D	Murata	CAP CER 1uf 10V 10% X5R 0402
4	C18,C21,C25,C26,C27	5	0.1 uF	—	GRM155R61A104KA01 D	Murata	CAP CER 0.1UF 10V X5R 0402
5	C20,C28	2	10 uF	—	GRM21BR61A106KE19L	Murata	CAP CER 10UF 10V X5R 0805
6	C22,C23,C30,C31,C32,C33, C34,C35	8	100 nF	—	GRM155R61A104KA01 D	Murata	CAP CER 0.1UF 10V X5R 0402
7	C36,C38	2	10 uF	—	C1608X5R1E106M080A C	TDK Corporation	CAP CER 10UF 25V X5R 0603
8	C37,C39	2	0.1 uF	—	CL05A104KA5NNNC	Samsung	CAP CER 0.1UF 25V X5R 0402
9	C40	1	0.1 uF	—	885012205037	Wurth	CAP CER 0.1UF 16V X7R 0402
10	D1,D2,D3,D4,D5,D6,D7	7	Green	—	LTST-C190KGKT	LITE-On INC	LED SUPER GREEN CLEAR 0603 SMD
11	D8	1	D1213A-01WS-7	—	D1213A-01WS-7	Diodes Incorporated	TVS DIODE 3.3VWM 10VC SOD323
12	J1,J2	2	ERM5-030-05.0-L-DV-K-TR	—	ERM5-030-050-L-DV-K-TR	Samtec Inc	Conn High Speed Edge Rate Terminal Strip HDR 60 POS 0.5mm Solder ST SMD T/R -
13	J3	1	8 HEADER	—	—	—	General purpose 100 Mils header
14	J4	1	Jumper	—	—	—	General purpose 100 mils 1x2 Header
15	L2	1	60 Ω 500 mA	—	MMZ1608Y600BTA00	TDK	FERRITE BEAD 60 OHM 0603 1LN

Item	Reference	Qty	Value	Comments	Part Number	Manufacturer	Description
16	L4,L6,L8	3	60 Ω 2.3 A	—	MPZ1608Y600BTA00	TDK	FERRITE BEAD 60 OHM 0603 1LN
17	Q1	1	MMBT2222A	—	MMBT2222A,215	NXP Semiconductor	TRANS NPN 40V 0.6A SOT23
18	R1,R2,R3,R4,R28,R29	6	4.7 k	—	CRCW06034K70FKEA	Vishay	RES SMD 4.7K OHM 1% 1/10W 0603
19	R5,R6,R7,R8,R9,R10,R11, R12,R13,R15,R19,R27,R39	13	0	—	RC0603JR-070RL	Yageo	RES SMD 0.0OHM JUMPER 1/10W 0603
20	R26	1	0	DNL	RC0603JR-070RL	Yageo	RES SMD 0.0OHM JUMPER 1/10W 0603
21	R17	1	2.49 K	—	ERA-2AEB2491X	Panasonic	RES SMD 2.49KOHM 0.1% 1/16W 0402
22	R18,R23	2	51E	—	ERJ-2GEJ510X	Panasonic	RES SMD 51 OHM 5% 1/10W 0402
23	R20,R40,R41	3	100 K	—	ERA-2AEB104X	Panasonic	RES SMD 100K OHM 0.1% 1/16W 0402
24	R21	1	1 M	—	ERJ-2GEJ105X	Panasonic	RES SMD 1M OHM 5% 1/10W 0402
25	R22	1	1.5 K	—	ERJ-2RKF1501X	Panasonic	RES SMD 1.5K OHM 1% 1/10W 0402
26	R31,R32,R33,R34,R36	5	330E	—	CRCW0402330RFKED	Vishay Dale	RES SMD 330 OHM 1% 1/16W 0402
27	R35	1	1 K	—	RC0603FR-071KL	Yageo	RES SMD 1K OHM 1% 1/10W 0603
28	R37	1	1 K	—	RMCF0402JT1K00	Stackpole Electronics Inc	RES SMD 1K OHM 5% 1/16W 0402
29	R38	1	10 K	—	ERJ-3EKF1002V	Panasonic	RES SMD 10K OHM 1% 1/10W 0603
30	SW1	1	SYS_RST	—	434153017835	Wurth	SWITCH TACTILE SPST-NO 0.05A 12V
31	TP13,TP14	2	TEST POINT	—	22-28-4020	Molex	Test Point 0.1"
32	U1	1	SN75DP130SS	—	SN75DP130SSRGZR	Texas Instruments	IC DISPLYPRT 1:1 REDRIVR 48VQFN
33	U2	1	SN65MLVD200	—	SN65MLVD200AD	Texas Instruments	IC LVDS LINE DVR/RCVR 8-SOIC

Item	Reference	Qty	Value	Comments	Part Number	Manufacturer	Description
34	U3	1	DSC1103CE2-135.0000	—	DSC1103CE2-135.0000	Microchip Technology Inc	Standard Clock Oscillators -20C - 70C 25 ppm 135.0000MHz
35	U4	1	LT1086CM-3.3	DNI	LT1086CM-3.3#TRPBF	Linear Tech	IC REG LDO 3.3V 1.5A D2PAK
36	U16	1	FUSE	—	0154004.DRT	Littelfuse Inc.	FUSE BRD MNT 4A 125VAC/VDC 2SMD
37	DISPLAYPORT-VIP-OUTPUT BOARD REV1 PCB	1	—	—	305-PD-16-0XXX	PACTRON	—

Revision History

Date	Version	Change Summary
March 2018	1.0	Initial release.

7th Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com