MT3332 GNSS Host-Based Solution Technical Brief

Version: 1.0
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Specifications are subject to change without notice.

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1 System Overview

1.1 General descriptions

MT3332 is a high-performance single-chip multi-GNSS solution which includes on-chip CMOS RF and digital baseband. It is able to achieve the industry's highest level of sensitivity, accuracy and Time-to-First-Fix (TTFF) with the lowest power consumption in a small-footprint lead-free package. Its small footprint and minimal BOM requirement provide significant reductions in the design, manufacturing and testing resource required for portable applications.

With built-in LNA to reach total receiver chain NF to 2.2 dB, you can eliminate antenna requirement and do not need external LNA. With its on-chip image-rejection mixer, the spec of external SAW filter is alleviated. With an on-chip automatic center frequency calibration band pass filter, an external filter is not required. The on-chip power management design allows MT3332 to be easily integrated into your system without extra voltage regulator. With both linear and a highly efficient switching type regulator embedded, MT3332 allows direct battery connection and does not need any external LDO, which gives customers plenty of choices for the application circuit.

Up to 12 multi-tone active interference cancellers (ISSCC2011 award) offer you more flexibility in system design. The integrated PLL with Voltage Controlled Oscillator (VCO) provides excellent phase noise performance and fast locking time. A real-time clock is also provided to accelerate acquisition at the system restart-up.

MT3332 acquires and tracks satellites in the shortest time even at indoor signal levels. MT3332 supports various location and navigation applications, including autonomous GPS, GLONASS, GALILEO, BEIDOU (after ICD released), SBAS ranging (WAAS, EGNOS, GAGAN, and MSAS), QZSS, DGPS (RTCM) and AGPS.

Through MT3332's excellent low-power consumption characteristic (acquisition 36 mW, track 26 mW), while using power sensitive devices, especially portable applications, you will not need to worry about the operating time anymore and can have more fun. Combined with many advanced features including AlwaysLocate™, HotStill™ and EPO™ function, MT3332 provides always-on position with minimal average power consumption. The great features provide you supreme experiences for portable applications such as DSC, cellular phone, PMP, and gaming devices.

1.2 Features

- Specifications
  - GPS/GLONASS/GALILEO/BEIDOU (after ICD released) receiver
  - Supports multi-GNSS incl. QZSS, SBAS ranging
  - Supports WAAS/EGNOS/MSAS/GAGAN
  - 12 multi-tone active interference cancellers (ISSCC2011 award)
  - RTCM ready
  - Indoor and outdoor multi-path detection and compensation
  - Supports FCC E911 compliance and A-GPS
  - Max. fixed update rate up to 5 Hz
- Advanced software features
  - AlwaysLocate™ advanced location awareness technology
  - EPO™/HotStill™ orbit prediction
- Reference oscillator
  - TCXO
    - Frequency: 16.368 MHz, 12.6 ~ 40.0 MHz
    - Frequency variation: ±2.5 ppm
  - Crystal
    - Frequency: 26 MHz, 12.6 ~ 40.0 MHz
    - Frequency accuracy: ±10 ppm
- RF configuration
  - SoC, integrated in single chip with CMOS process
- Pulse-per-second (PPS) GPS time reference
  - Adjustable duty cycle
  - Typical accuracy: ±10 ns
- Power scheme
  - A 1.8 volts SMPS build-in SOC
  - Direct lithium battery connection (2.8 ~ 4.3 volts)
  - Self build 1.1 volts RTC LDO, 1.1 volts core LDO, and 2.8 volts TCXO LDO
- Build-in reset controller
  - Does not need of external reset control IC
- Internal real-time clock (RTC)
  - 32.768 KHz ± 20 ppm crystal
  - 1.1 volts RTC clock output
  - Supports external pin to wake up MT3332
- Backup mode
  - A Force_On pin to ease backup mode application circuit.
- Serial interface
  - 3 UARTs
  - SPI
  - I2C
  - GPIO interface (up to 15 pins)
- NMEA
  - NMEA 0183 standard V3.01 and backward compliance
  - Supports 219 different data
- Superior sensitivities
  - Acquisition: -148 dBm (cold) / -163 dBm (hot)
  - Tracking: -165 dBm
- Ultra-low power consumption (GPS+GLONASS)

  - Acquisition: 36 mW
  - Tracking: 26 mW
  - AlwaysLocate™: 3.0 mW
- Package
  - VFBGA: 4.3 mm x 4.3 mm, 57 balls, 0.5 mm pitch
  - WLCSP: 2.7 mm x 2.7 mm, 48 ball, 0.4 mm pitch
  - QFN: 6mm x 6mm, 48 ball
- Slim hardware design
  - 52 mm^2 solution footprint with all software features inside
  - 9 passive external components
  - Single RF Front-End for multi-GNSS frequency bands
- Compatibility
  - Pin-to-pin compatible to MT3336

2 Pin Assignment and Descriptions

2.1 Pin assignment (top view)

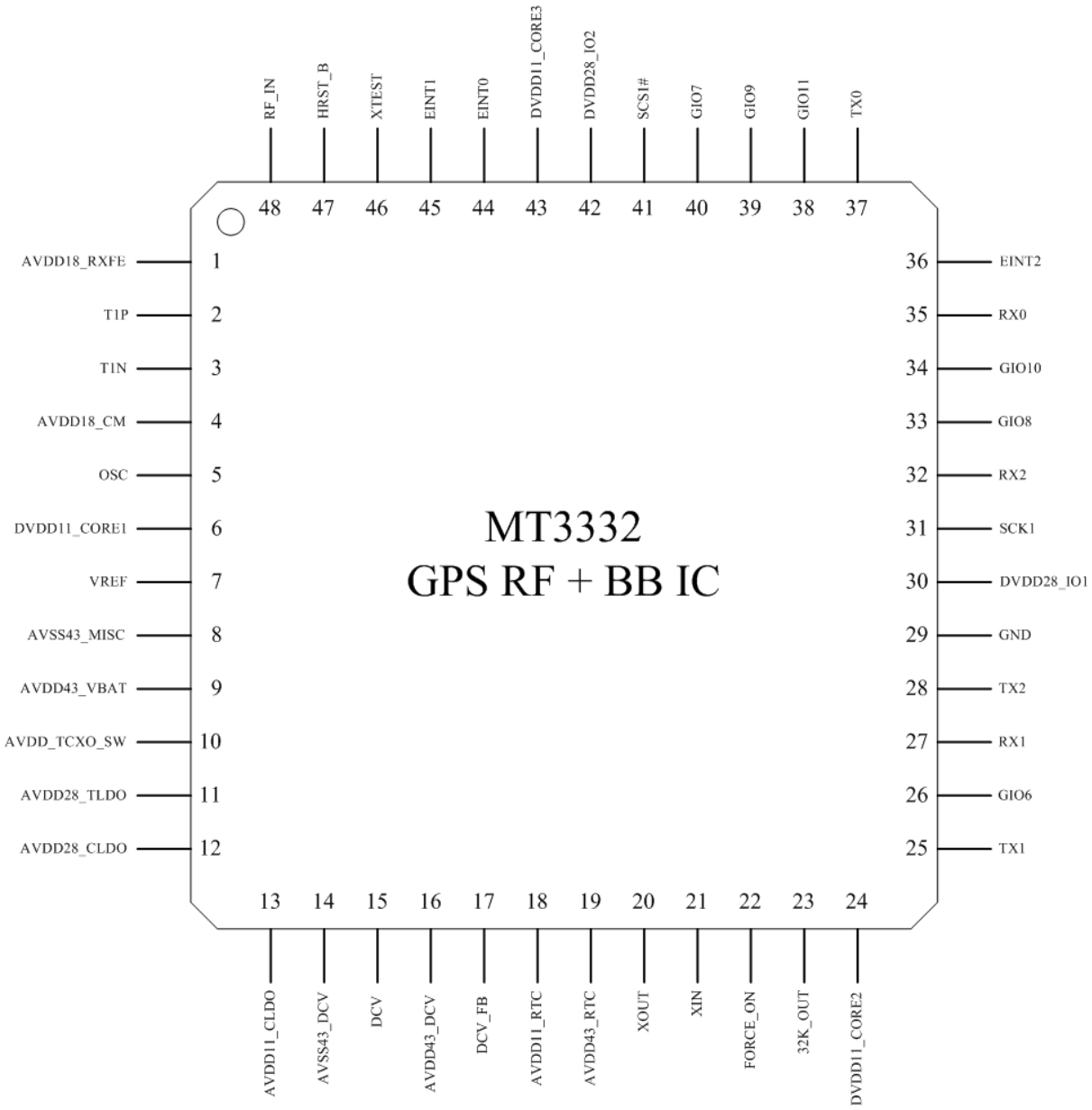


Figure 1 Pin assignment (top view)

2.2 Pin descriptions

Pin#	Symbol	Type	Description
System interface (2 pins)			
47	HRST_B	2.8V LVTTL input SMT	System reset. Active low Default: pull-up
46	XTEST	2.8V LVTTL input SMT	Test mode. *Must keep low in normal mode.* Default: pull-down
	BOPT0	2.8V LVTTL input 75K pull up, SMT	Bonding option 0 1 : AIO flash 0 : AIO ROM
	BOPT1	2.8V LVTTL input 75K pull up, SMT	Bonding option 1 1 : HOST mode 0 : AIO mode
Peripheral interface (8 pins)			
35	RX0/MM_I2CC/H_SPI_SI	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial input for UART 0 Default: pull-up Default: 8mA driving
37	TX0/MM_I2CD/H_SPI_SO	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 0 Default: pull-up Default: 8mA driving
27	RX1/H_SPI_SCK/CTS0/ MM_I2CC/CXO_TSENS/ GIO0	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial input for UART 1 Default: pull-up Default: 8mA driving
25	TX1/TXIND/RTS0/MM_I2CD/CXO_CS/GIO1	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 1 Default: pull-up Default: 8mA driving
32	RX2/SPI_SI/JDI/DBG_RX/BSI_CK/GIO2	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial input for UART 2 Default: pull-up Default: 8mA driving
28	TX2/SPI_SO/DBG_TX/GIO3	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 2 Default: pull-up Default: 8mA driving Strap pin tcxo_sw_sel 1'b0: AVDD_TCXO_SW output 1.8V 1'b1: AVDD_TCXO_SW output 2.8V

Pin#	Symbol	Type	Description
	SCK0	2.8V, LVTTL I/O PPU, PPD,SMT 2mA~16mA PDR	Synchronous serial interface (SPI) Default 75K pull down Default 8mA driving
	SCS0_	2.8V, LVTTL I/O PPU, PPD,SMT 2mA~16mA PDR	SPI slave select 0. Active low Default 75K pull up Default 8mA driving
	SIN0	2.8V, LVTTL I/O PPU, PPD,SMT 2mA~16mA PDR	Synchronous serial interface (SPI) Default 75K pull down Default 8mA driving
	SO0	2.8V, LVTTL I/O PPU, PPD,SMT 2mA~16mA PDR	Synchronous serial interface (SPI) Default 75K pull down Default 8mA driving
31	SCK1/SPI_SCK/GIO4	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	SPI clock output Default: pull-up Default: 8mA driving Strap pin clk_sel[0] Clk_sel[1:0] Mode 2'b00: XTAL mode 2'b01: External clock mode 2'b10: TCXO mode 2'b11: 16.368MHz TCXO mode
41	SCS1#/SPI_SCS#/BSI_DATA/SYNC_PULSE/GIO5	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	SPI slave selection 1 Default: pull-up Default: 8mA driving Strap pin clk_sel[1]
Debugging interface (6 pins)			
26	BSI_CK/MM_I2CC/ECLK/GIO6	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO6 Default: pull-down Default: 8mA driving
40	BSI_CS/MM_I2CD/DUTY_CYCLE/PPS/GIO7	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO7 Default: pull-down Default: 8mA driving
33	FRAME_SYNC/DBG_RX/GIO8	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO8. Default: pull-down Default: 8mA driving

Pin#	Symbol	Type	Description
39	PPS/DBG_TX/GIO9	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO9 Default: pull-up Default: 8mA driving Strap pin host_sel[0] Host_sel[1:0] Interface 2'b00: I2C (by request) 2'b01: Reserved 2'b10: SPI (by request) 2'b11: UART
34	CXO_CS/GIO10	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO10 Default: pull-up Default: 8mA driving Strap pin host_sel[1]
38	H_SPI_SCS#/CXO_TSENS/SYNC_PULSE/GIO11	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO11 Default: pull-up Default: 8mA driving
External system interface (3 pins)			
44	EINT0/MM_I2CC/BSI_CS/GIO12	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	External interrupt 0 Default: pull-down Default: 8mA driving
45	EINT1/MM_I2CD/PPS/BSI_DATA/GIO13	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	External interrupt 1 Default: pull-down Default: 8mA driving
36	EINT2/DBG_RX/PPS/GIO14	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	External interrupt 2 Default: pull-up Default: 8mA driving
D8	EINT3/DBG_TX/PPS	2.8V, LVTTL I/O PPU, PPD, SMT 2mA ~ 16mA PDR	External interrupt 3 Default: 75K pull-up Default: 8mA driving Shared with GIO15
RTC interface (6 pins)			
19	AVDD43_RTC	Analog power	RTC LDO input
18	AVDD11_RTC	Analog power	RTC LDO output
21	XIN	Analog input	RTC 32KHz XTAL input
20	XOUT	Analog output	RTC 32KHz XTAL output

Pin#	Symbol	Type	Description
23	32K_OUT/DR_IN	1.1V LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	RTC domain GPIO pin, can be programmed to be 32KHz clock output or DR wake-up signal input Default: pull-down Default: 16mA driving
22	FORCE_ON	1.1V LVTTL input PPU,PPD, SMT	Logic high to force power on this chip. Default: pull-up
RF & analog			
1	AVDD18_RXFE	RF power	1.8V supply for RF core circuits
2	T1P	Analog signal	RF testing signal
3	T1N	Analog signal	RF testing signal
A2/B2/ C2/D2	AVSS_RF	RF ground	RF ground pins
4	AVDD18_CM	RF power	1.8V supply for XTAL OSC, bandgap, thermal sensor and level shifter
5	OSC	Analog signal	Input for crystal oscillator or TCXO
48	RF_IN	RF signal	LNA RF Input pin
6	DVDD11_CORE1	Digital power	Digital 1.1V core power input
24	DVDD11_CORE2	Digital power	Digital 1.1V core power input
43	DVDD11_CORE3	Digital power	Digital 1.1V core power input
	DVSS11_CORE	Digital ground	Digital 1.1V core ground
30	DVDD28_IO1	Digital power	Digital 1.8/2.8V IO power input
42	DVDD28_IO2	Digital power	Digital 1.8/2.8V IO power input
29	GND	Digital ground	Digital ground
	DVSS28_IO	Digital ground	Digital 1.8/2.8V IO ground
	DVDD28_SF	Digital power	Digital 2.8V serial flash power input
	DVSS28_SF	Digital ground	Digital 2.8V serial flash ground
7	VREF	Analog	Bandgap output pin. Must add 1uF decoupling cap on EVB.
8	AVSS43_MISC	Analog ground	GND pin for buck controller, TCXO LDO and start-up block
9	AVDD43_VBAT	Analog power	TCXO LDO input pin. Always be powered by external source. UVLO will detect this PIN to check power status.
10	AVDD_TCXO_SW	Analog power	TCXO power switch output pin
11	AVDD28_TLDO	Analog power	TCXO LDO output pin
12	AVDD28_CLDO	Analog power	Core LDO input pin. Always powered by external source or SMPS
13	AVDD11_CLDO	Analog power	Core LDO output pin
	AVSS11_CLDO	Analog ground	GND pin for core LDO
14	AVSS43_DCV	SMPS	SMPS GND pin

Pin#	Symbol	Type	Description
15	DCV	SMPS	SMPS output pin
16	AVDD43_DCV	SMPS	SMPS input pin.
17	DCV_FB	SMPS	SMPS feedback pin

Notes:

PPU = Programmable pull-up
PPD = Programmable pull-down
PSR = Programmable slew rate
PDR = Programmable driving

3 Electrical Characteristics

3.1 DC characteristics

3.1.1 Absolute maximum ratings

Symbol	Parameter	Rating	Unit
AVDD43_DCV	SMPS power supply	-0.3 ~ 4.3	V
AVDD43_VBAT	2.8 volts TLDO power supply	-0.3 ~ 4.3	V
AVDD28_CLDO	1.1 volts CLDO power supply	-0.3 ~ 3.6	V
DVDD28_IO1 DVDD28_IO2	IO 2.8/1.8 volts power supply	-0.3 ~ 3.6	V
DVDD11_CORE1 DVDD11_CORE2 DVDD11_CORE3	Baseband 1.1 volts power supply	-0.3 ~ 1.21	V
AVDD43_RTC	RTC 1.1 volts LDO power supply	-0.3 ~ 4.3	V
AVDD18_RXFE	1.8 volts supply for RF core circuits	-0.3 ~ 3.6	V
AVDD18_CM		-0.3 ~ 3.6	V
T_{STG}	Storage temperature	-50 ~ +125	°C
T_A	Operating temperature	-45 ~ +85	°C

3.1.2 Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD43_DCV	SMPS power supply	2.8	3.3	4.3	V
AVDD43_VBAT	2.8 volts TLDO power supply	2.8	3.3	4.3	V
DVDD11_CORE	1.1 volts baseband core power	0.99	1.1	1.21	V
DVDD28_IO	2.8 volts digital I/O power	2.52	2.8	3.08	V
	1.8 volts digital I/O power	1.62	1.8	1.98	V
AVDD18_RXFE	1.35 volts supply for RF core circuits in bypass mode	1.3	1.35	1.98	V
	1.8 volts supply for RF core circuits in LDO mode	1.62	1.8	3.08	V
AVDD18_CM	1.35 volts supply for common RF block in bypass mode	1.3	1.35	1.98	V
	1.8V volts supply for common RF block in LDO mode	1.62	1.8	3.08	V
T_A	Operating temperature	-40	25	85	˚C

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_j	Commercial junction operating temperature	0	25	115	˚C
	Industry junction operating temperature	-40	25	125	˚C

3.1.3 General DC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
I_{IL}	Input low current	No pull-up or down	-1	1	uA
I_{IH}	Input high current	No pull-up or down	-1	1	uA
I_{OZ}	Tri-state leakage current		-10	10	uA

3.1.4 DC electrical characteristics for 2.8 volts operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		2.52	2.8	3.08	V
V_{IL}	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
V_{OL}	Output low voltage	VDDIO = min I_{OL} = -2 mA	-	-	0.15*VDDIO	V
V_{OH}	Output high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	40	85	190	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 2.8 V	40	85	190	KΩ

3.1.5 DC electrical characteristics for 1.8 volts operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		1.62	1.8	1.98	V
V_{IL}	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OL}	Output low voltage	VDDIO = min I_{OL} = -2 mA	-	-	0.15*VDDIO	V
V_{OH}	Output high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	70	150	320	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 1.8 V	70	150	320	KΩ

3.1.6 DC electrical characteristics for 1.1 volts operation (for FORCE_ON and 32K_OUT)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		0.99	1.1	1.21	V
V_{IL}	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
V_{OL}	Output low voltage	VDDIO = min I_{OL} = -2 mA	-	-	0.15*VDDIO	V
V_{OH}	Output high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	130		560	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 1.1 V	130		560	KΩ

3.2 Analog related characteristics

3.2.1 SMPS DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_DCV	SMPS input supply voltage	2.8	3.3	4.3	V	
DCV	SMPS output	1.74	1.84	1.94	V	
I_{cc}	SMPS output current	-	-	100	mA	
ΔV_PWM	Ripple of PWM mode	-	-	40	mV	With L=1uH, C=4.7uF
ΔV_PFM	Ripple of PFM mode	-	-	90	mV	With L=1uH, C=4.7uF

3.2.2 TCXO LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_VBAT	TCXO LDO input supply voltage	2.8	3.3	4.3	V	Will change to bypass mode under 3.1 volts
AVDD28_TLDO	TCXO LDO output	2.71	2.8	2.89	V	
I_{cc}	LDO output current	-	-	50	mA	Not include external devices
	PSRR-30 KHz	35	-	-	dB	Co = 1 uF, ESR = 0.05, Iload = 25 mA
	Load regulation	-84	10	84	mV	

3.2.3 TCXO SWITCH DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD_TCXO_SW	TCXO switch output voltage @ TCXO switch input = AVDD28_TLDO	2.66	-	-	V	
AVDD_TCXO_SW	TCXO switch output voltage @ TCXO switch input = AVDD28_CLDO	1.71	-	-	V	
I_{max}	TCXO SWITCH current limit	-	-	30	mA	

3.2.4 1.1 volts core LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD28_CLDO	1.2 volts LDO input supply voltage	1.62	1.8	3.08	V	
AVDD11_CLDO	1.1 volts LDO output	1.05	1.12	1.2	V	
I_{cc}	LDO output current	-	-	50	mA	
	Load regulation	-	-	-	mV	

3.2.5 1.1 volts RTC LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_RTC	RTC LDO input supply voltage	2	4	4.3	V	
AVDD11_RTC	RTC LDO output	0.99	1.1	1.21	V	
I_{cc}	LDO output current	-	-	3	mA	
I_{leak}	Leakage current	2.2	10	-	uA	Including LDO and RTC domain circuit

3.2.6 32 KHz crystal oscillator (XOSC32)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD11_RTC	Analog power supply	0.99	-	1.21	V	
Dcyc	Duty cycle	-	50	-	%	

3.3 RF related characteristics

3.3.1 DC electrical characteristics for RF part

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{cc}(GPS+GLONASS)	Total supply current:	-	8.9	-	mA

3.3.2 RX chain (GPS+GLONASS mode)

Parameter	Condition	Min.	Typ.	Max.	Unit
RF input frequency		-	1575.4	-	MHz
LO frequency		-	1588.6	--	MHz
LO leakage	Measured at balun matching network input at LNA high gain	-	-70	-	dBm
Input return loss	Differential input and external matched to 50Ω source using balun matching network for all gain	-10	-	-	dB
Gain (Av) (integrated average over Fc+-4M)	High current mode with max PGA gain	80	76	70	dB
	Low current mode with max PGA gain	-	64	-	dB
PGA Gain range		-	24	-	dB
PGA Gain step		-	2	-	dB
NF (integrated average over Fc+-4M)	High current mode with max PGA gain	-	2.2	-	dB

3.3.3 Crystal oscillator (XO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{tcxo}	TCXO oscillation frequency	12.6	16.368	40	MHz
V_{tcxo}	TCXO output swing	0.8	1.2	-	Vpp

4 Interface Characteristics

4.1 RS-232 interface timing

Baudrate required (bps)	Programmed baudrate (bps)	Baudrate error (%)	Baudrate error (%) [3]
4,800	4,800.000	0.0000	0.002
9,600	9,600.000	0.0000	0.002
14,400	14,408.451	0.0587	0.0567
19,200	19,164.319	0.0587	0.0567
38,400	38,422.535	0.0587	0.0567
57,600	57,633.803	0.0587	0.0567
115,200	115,267.606	0.0587	0.0567
230,400	230,535.211	0.0587	0.0567
460,800	454,666.667	-1.3310	-1.3330
921,600	909,333.333	-1.3310	-1.3330

Notes:

1 UART baud-rate settings with UART_CLK frequency = 16.368 MHz (UART_CLK uses the reference clock of the system).

2 The baudrate error is optimized. Each baudrate needs to adjust counter to obtain the optimized error.

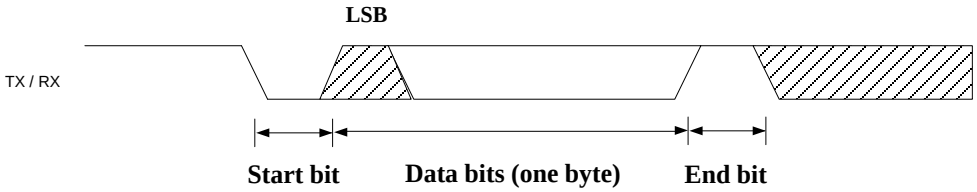


Figure 2 Timing diagram of RS-232 interface

1.1 SPI interface timing

Description	Symbol	Min.	Max.	Unit	Note
SCS# setup time	T1	0.5T	-	ns	1
SCS# hold time	T2	0.5T	-	ns	1
SO setup time	T3	0.5T – 3t	0.5T - 2t	ns	1, 2
SO hold time	T4	0.5T + 2t	0.5T + 3t	ns	1, 2

Description	Symbol	Min.	Max.	Unit	Note
SIN setup time	T5	3t	-	ns	1, 2
SIN hold time	T6	10	-	ns	1

Notes:

1 The condition of SPI clock cycle (T) is (SPI_IPLL/12) MHz ~ (rf_clk/1,020) MHz.

2 t indicates the period of SPI controller clock, which is SPI_IPLL clock or rf_clk.

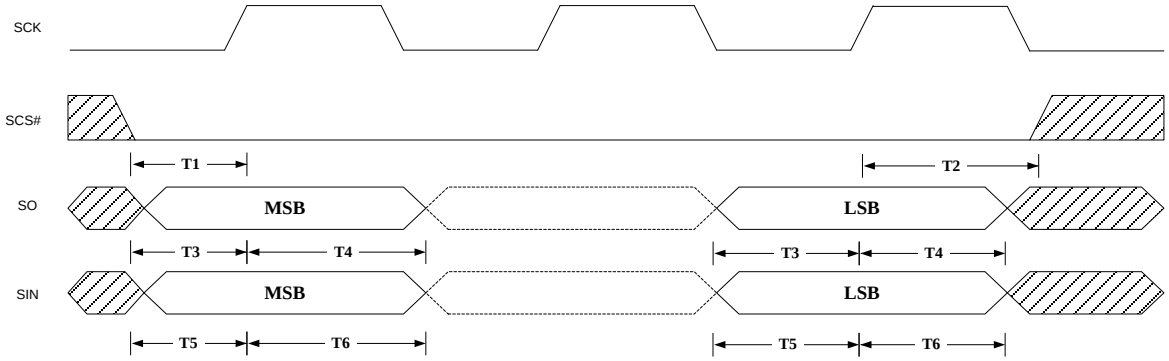


Figure 3 Timing diagram of SPI interface

1.2 I2C interface timing

Symbol	Period
T1	(MM_CNT_PHASE_VAL0+1)/TCXO_CLK
T2	(MM_CNT_PHASE_VAL1+1)/TCXO_CLK
T3	(MM_CNT_PHASE_VAL2+1)/TCXO_CLK
T4	(MM_CNT_PHASE_VAL3+1)/TCXO_CLK

Note: The condition of I2C clock cycle (I2C_CLK) is (TCXO_CLK/4) MHz ~ (TCXO_CLK/(MM_CNT+4)) MHz. The MM_CNT is sum of MM_CNT_PHASE_VAL0, MM_CNT_PHASE_VAL1, MM_CNT_PHASE_VAL2 and MM_CNT_PHASE_VAL3 in full speed mode.

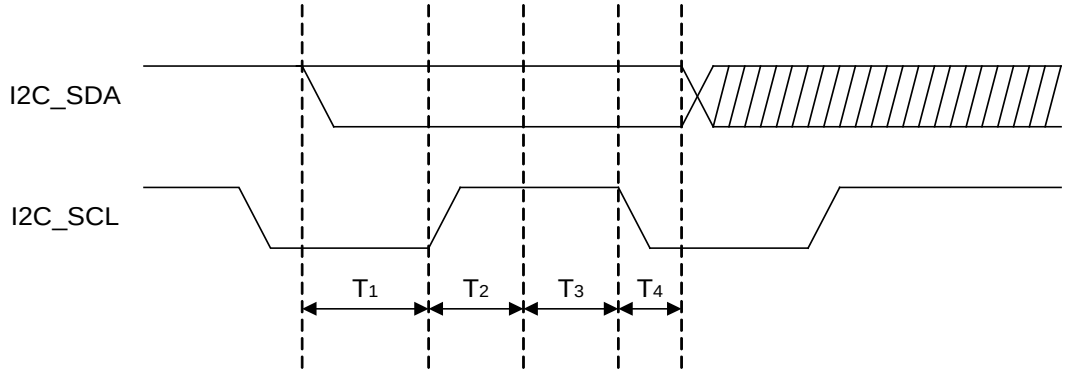


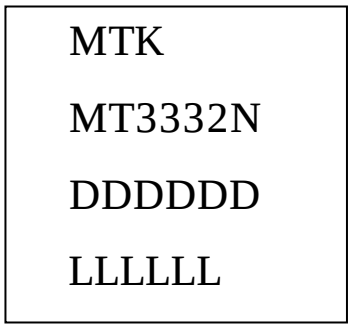
Figure 4 Timing diagram of HOST I2C interface

5 Package Description

5.1 Ordering information

Order #	Marking	Temp. range	Package
MT3332N		-40 ~ +85 °C	QFN

5.2 Top mark



N : QFN package
DDDDDD : Date code
LLLLLL : Lot number

5.3 Package dimensions

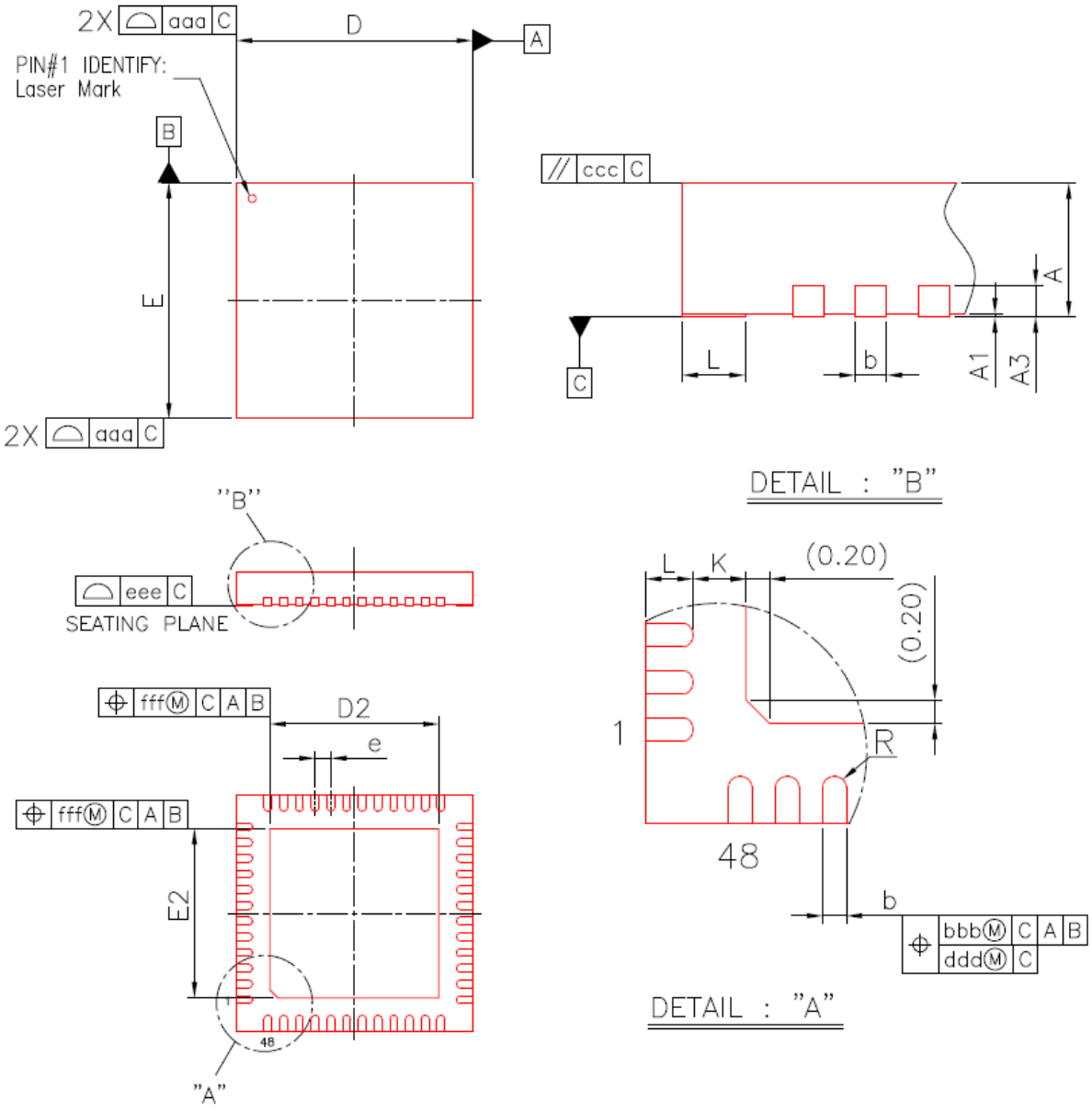


Figure 5 Packaging dimensions diagram

Exposed Pad Size							Internal Pad Size					
L/F	Dimension in mm			Dimension in inch			Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
D2/E2	4.15	4.30	4.45	0.163	0.169	0.175	4.45	4.60	4.75	0.175	0.181	0.187

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 6 Packaging dimensions tables

ESD CAUTION

MT3332 is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT3332 is with built-in ESD protection circuitry, please handle with care to avoid permanent malfunction or performance degradation.

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