DDR2 SDRAM SODIMM

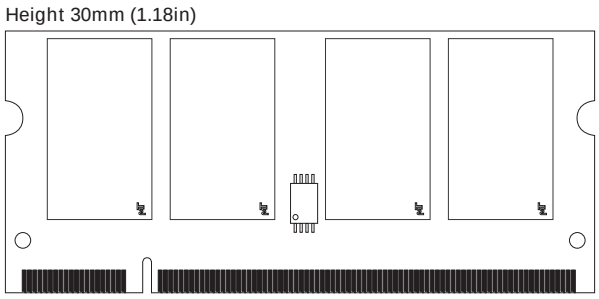
MT8HTF3264H(I) – 256MB
MT8HTF6464H(I) – 512MB
MT8HTF12864H(I) – 1GB

For component data sheets, refer to Micron's Web site: www.micron.com/products/dram/ddr2

Features

- 200-pin, small outline, dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- 256MB (32 Meg x 64), 512MB (64 Meg x 64), 1GB (128 Meg x 64)
- V_{DD} = $V_{DD}Q$ = +1.8V
- V_{DDSPD} = +1.7V to +3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Single rank

Figure 1: 200-pin SODIMM (MO-224 R/C "B")



Options — Marking

- Operating temperature
- Commercial (0°C ≤ T_C ≤ +85°C)
- Industrial (–40°C ≤ T_C ≤ +95°C)[1,2] — I
- Package
  - 200-pin SODIMM (Pb-free) — Y
- Frequency/CAS latency[3]
  - 2.5ns @ CL = 5 (DDR2-800)[4] — -80E
  - 2.5ns @ CL = 6 (DDR2-800)[4] — -800
  - 3ns @ CL = 5 (DDR2-667) — -667
  - 3.75ns @ CL = 4 (DDR2-533) — -53E
  - 5.0ns @ CL = 3 (DDR2-400) — -40E
- PCB Height
  - 30mm (1.18in)

Notes: 1. Industrial temperatures apply to DRAM only.
2. Contact Micron for product availability.
3. CL = CAS (READ) latency
4. Not available in 256MB density

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	533	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 2: Addressing

	256MB	512MB	1GB
Refresh count	8K	8K	8K
Row address	8K A[12:0]	16K A[13:0]	16K A[13:0]
Device bank address	4 BA[1:0]	4 BA[1:0]	8 BA[2:0]
Device page size per bank	1KB	1KB	1KB
Device configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]	1K A[9:0]
Module rank address	1 S0#	1 S0#	1 S0#

Table 3: Part Numbers and Timing Parameters – 256MB Modules
Base device: MT47H32M8, 256Mb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT8HTF3264HY-667__	256MB	32 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT8HTF3264HY-53E__	256MB	32 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT8HTF3264HY-40E__	256MB	32 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 4: Part Numbers and Timing Parameters – 512MB Modules
Base device: MT47H64M8, 512Mb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT8HTF6464HY-80E__	512MB	64 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT8HTF6464HY-800__	512MB	64 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT8HTF6464HY-667__	512MB	64 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT8HTF6464HY-53E__	512MB	64 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT8HTF6464HY-40E__	512MB	64 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 5: Part Numbers and Timing Parameters – 1GB Modules
Base device: MT47H128M8, 1Gb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT8HTF12864HY-80E__	1GB	128 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT8HTF12864HY-800__	1GB	128 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT8HTF12864HY-667__	1GB	128 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT8HTF12864HY-53E__	1GB	128 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT8HTF12864HY-40E__	1GB	128 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes:
1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8HTF6464HY-667A3.
2. For the latest componentdata sheets, see Micron's Web site: www.micron.com/products/dram/ddr2

Module Pin Assignments and Descriptions

Table 6: Pin Assignments

200-Pin SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	DQS2	101	A1	151	DQ42
3	VSS	53	VSS	103	VDD	153	DQ43
5	DQ0	55	DQ18	105	A10/AP	155	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48
9	VSS	59	VSS	109	WE#	159	DQ49
11	DQS0#	61	DQ24	111	VDD	161	VSS
13	DQS0	63	DQ25	113	CAS#	163	NC
15	VSS	65	VSS	115	NC#	165	VSS
17	DQ2	67	DM3	117	VDD	167	DQS6#
19	DQ3	69	NC	119	NC	169	DQS6
21	VSS	71	VSS	121	VSS	171	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50
25	DQ9	75	DQ27	125	DQ33	175	DQ51
27	VSS	77	VSS	127	VSS	177	VSS
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56
31	DQS1	81	VDD	131	DQS4	181	DQ57
33	VSS	83	NC	133	VSS	183	VSS
35	DQ10	85	NC/BA2	135	DQ34	185	DM7
37	DQ11	87	VDD	137	DQ35	187	VSS
39	VSS	89	A12	139	VSS	189	DQ58
41	VSS	91	A9	141	DQ40	191	DQ59
43	DQ16	93	A8	143	DQ41	193	VSS
45	DQ17	95	VDD	145	VSS	195	SDA
47	VSS	97	A5	147	DM5	197	SCL
49	DQS2#	99	A3	149	VSS	199	VDDSPD

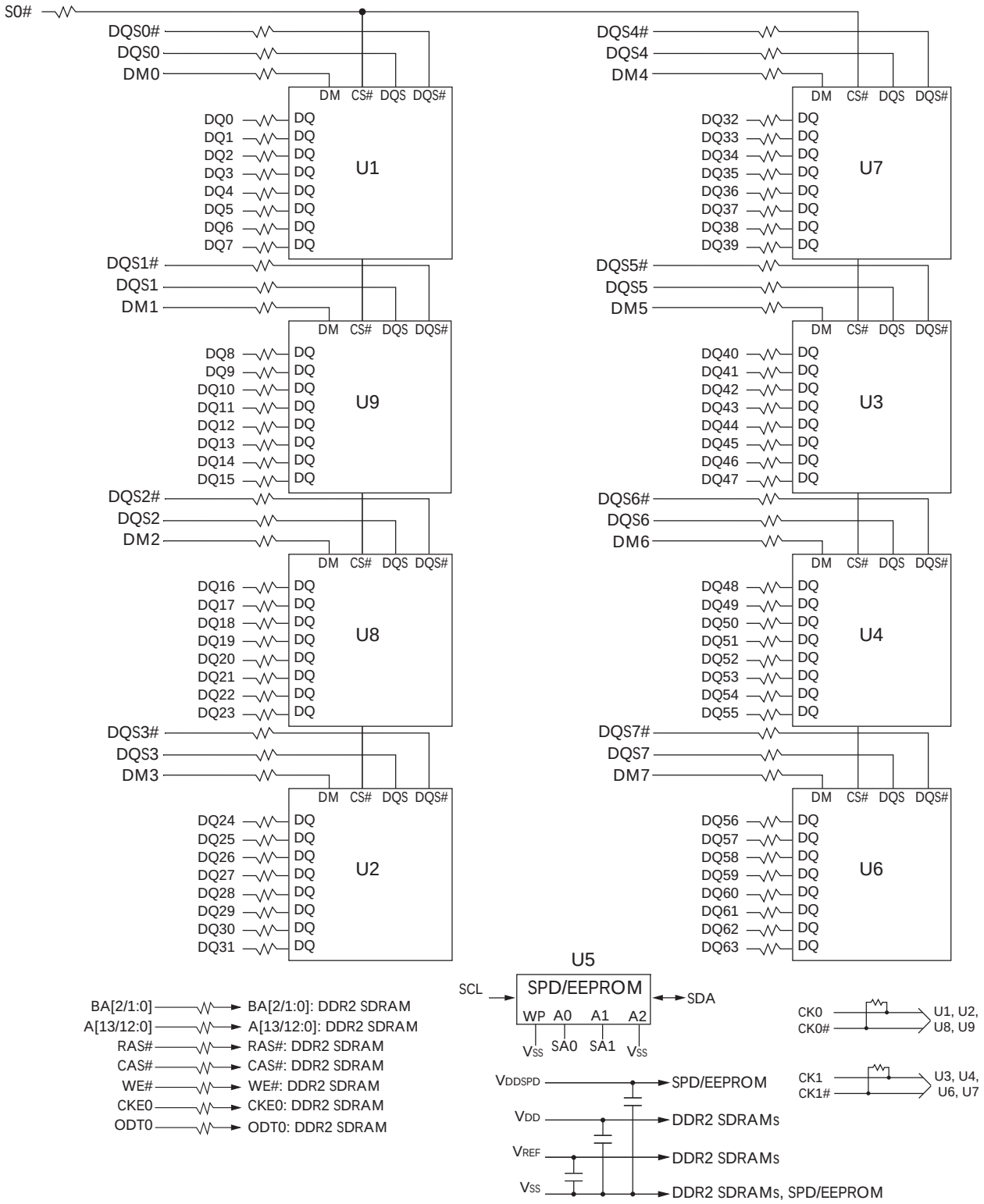
200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	VSS	52	DM2	102	A0	152	DQ46
4	DQ4	54	VSS	104	VDD	154	DQ47
6	DQ5	56	DQ22	106	BA1	156	VSS
8	VSS	58	DQ23	108	RAS#	158	DQ52
10	DM0	60	VSS	110	S0#	160	DQ53
12	VSS	62	DQ28	112	VDD	162	VSS
14	DQ6	64	DQ29	114	ODT0	164	CK1
16	DQ7	66	VSS	116	NC/A13	166	CK1#
18	VSS	68	DQS3#	118	VDD	168	VSS
20	DQ12	70	DQS3	120	NC	170	DM6
22	DQ13	72	VSS	122	VSS	172	VSS
24	VSS	74	DQ30	124	DQ36	174	DQ54
26	DM1	76	DQ31	126	DQ37	176	DQ55
28	VSS	78	VSS	128	VSS	178	VSS
30	CK0	80	NC	130	DM4	180	DQ60
32	CK0#	82	VDD	132	VSS	182	DQ61
34	VSS	84	NC	134	DQ38	184	VSS
36	DQ14	86	NC	136	DQ39	186	DQS7#
38	DQ15	88	VDD	138	VSS	188	DQS7
40	VSS	90	A11	140	DQ44	190	VSS
42	VSS	92	A7	142	DQ45	192	DQ62
44	DQ20	94	A6	144	VSS	194	DQ63
46	DQ21	96	VDD	146	DQS5#	196	VSS
48	VSS	98	A4	148	DQS5	198	SA0
50	NC	100	A2	150	VSS	200	SA1

Notes: 1. Pin 85 is NC for 256MB and 512MB, BA2 for 1GB.
2. Pin 116 is NC for 256MB, A13 for 512MB and 1GB.

Table 7: Pin Descriptions

Symbol	Type	Description
A[15:0]	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[2/1:0]) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. A[12:0] (512MB) and A[13:0] (1GB, 2GB). A[15:14] are connected for parity.
BA[2:0]	Input	**Bank address inputs:** BA[2/1:0] define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2/1:0] define which mode register (MR, EMR1, EMR2, and EMR3) is loaded during the LOAD MODE command. BA[1:0] (512MB, 1GB) and BA[2:0] (2GB).
CK[1:0] CK#[1:0]	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ, DQS, and DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM.
DM[8:0]	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of DQS. Although the DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODT0	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S0#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[1:0]	Input	**Serial address inputs:** These pins are used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** SCL is used to synchronize communication to and from the SPD EEPROM.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[8:0], DQS#[8:0]	I/O	**Data strobe:** DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module on the I^2C bus.
V_{DD}	Supply	**Power supply:** 1.8V ±0.1V. The component V_{DD} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**SPD EEPROM power supply:** +1.7V to +3.6V.
V_{REF}	Supply	**Reference voltage:** $V_{DD}/2$.
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Figure 2: Functional Block Diagram



General Description

The MT8HTF3264H, MT8HTF6464H, and MT8HTF12864H DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 256MB, 512MB, and 1GB memory modules organized in x64 configuration. DDR2 SDRAM modules use internally configured quad-bank (256Mb, 512Mb) or eight-bank (1Gb) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during reads and by the memory controller during writes. DQS is edge-aligned with data for reads and center-aligned with data for writes.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[1:0], which provide fourt unique DIMM/EEPROM addresses. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}		–1.0	+2.3	V
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}		–0.5	+2.3	V
V_{DDL}	V_{DDL} supply voltage relative to V_{SS}		–0.5	+2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+2.3	V
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤0.95V; (all other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE# S#, CKE, ODT	–40	+40	µA
		CK, CK#	–20	+20	
		DM	–5	+5	
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQs and ODT are disabled	DQ, DQS, DQS#	–5	+5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		–16	+16	µA
T_{CASE}	DDR2 SDRAM device operating temperature[1]	Commercial	0	+85	°C
		Industrial[2]	–40	+95	°C

Notes:
1. For further information, refer to technical note TN-00-08: Thermal Applications, available on Micron's Web site at www.micron.com/technotes.
2. Refresh rate must double when T_{CASE} exceeds 85°C.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 9.

Table 9: Module and Component Speed Grades
DDR2 components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-5E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

Table 10: DDR2 IDD Specifications and Conditions – 256MB

Values are for the MT47H32M8 DDR2 SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	720	640	600	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	800	720	680	mA
Precharge power-down current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	40	40	40	mA
Precharge quiet standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	320	280	200	mA
Precharge standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	320	280	240	mA
Active power-down current; All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	240	200	160	mA
	Slow PDN Exit MR[12] = 1		48	48	48	mA
Active standby current; All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	400	320	240	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,520	1,280	1,000	mA
Operating burst read current; All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,440	1,200	920	mA
Burst refresh current; ^{t}CK = ^{t}CK (IDD); Refresh the command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	1,440	1,360	1,320	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	40	40	40	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 conditions for detail		IDD7	2,080	1,920	1,840	mA

Table 11: DDR2 IDD Specifications and Conditions – 512MB

Values are for the MT47H64M8 DDR2 SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	800	720	640	640	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	920	840	760	720	mA
Precharge power-down current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	56	56	56	56	mA
Precharge quiet standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	400	360	320	280	mA
Precharge standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	440	400	360	320	mA
Active power-down current; All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	320	280	240	200	mA
	Slow PDN Exit MR[12] = 1		96	96	96	96	mA
Active standby current; All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	560	520	440	360	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1560	1360	1120	920	mA
Operating burst read current; All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1640	1440	1160	920	mA
Burst refresh current; ^{t}CK = ^{t}CK (IDD); Refresh the command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	1840	1440	1360	1320	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	56	56	56	56	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 conditions for detail		IDD7	2400	1920	1800	1760	mA

Table 12: DDR2 IDD Specifications and Conditions – 1GB (die revision A)
Values are for the MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	800	720	640	560	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	880	800	760	640	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	56	56	56	56	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	520	440	328	280	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	560	480	360	320	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	360	320	280	280	mA
	Slow PDN Exit MR[12] = 1		112	112	112	112	mA
Active standby current; All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	600	560	440	360	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1480	1280	1,040	880	mA
Operating burst read current; All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1520	1280	1040	880	mA
Burst refresh current; tCK = tCK (IDD); Refresh the command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2240	2080	2000	1760	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	56	56	56	56	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) - 1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 conditions for detail		IDD7	2680	2400	2320	2080	mA

Table 13: DDR2 IDD Specifications and Conditions – 1GB (die revision E)
Values are for the MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	720	680	560	560	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	880	800	760	720	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	56	56	56	56	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	400	320	320	280	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	400	320	320	280	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	320	240	240	240	mA
	Slow PDN Exit MR[12] = 1		80	80	80	80	mA
Active standby current; All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	480	440	360	320	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1280	1080	1000	840	mA
Operating burst read current; All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1280	1080	1000	840	mA
Burst refresh current; tCK = tCK (IDD); Refresh the command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	1880	1720	1680	1640	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	56	56	56	56	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) - 1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 conditions for detail		IDD7	2680	2240	2160	2080	mA

Serial Presence-Detect

Table 14: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.1	3.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3.0	µA
Standby current	I_{SB}	1.6	4.0	µA
Power supply current, READ: SCL clock frequency = 100 kHz	ICC_R	0.4	1.0	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	ICC_W	2.0	3.0	mA

Table 15: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA fall time	^tF	–	300	ns	2
SDA rise time	^tR	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tH:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SCL clock frequency	^fSCL	–	400	kHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

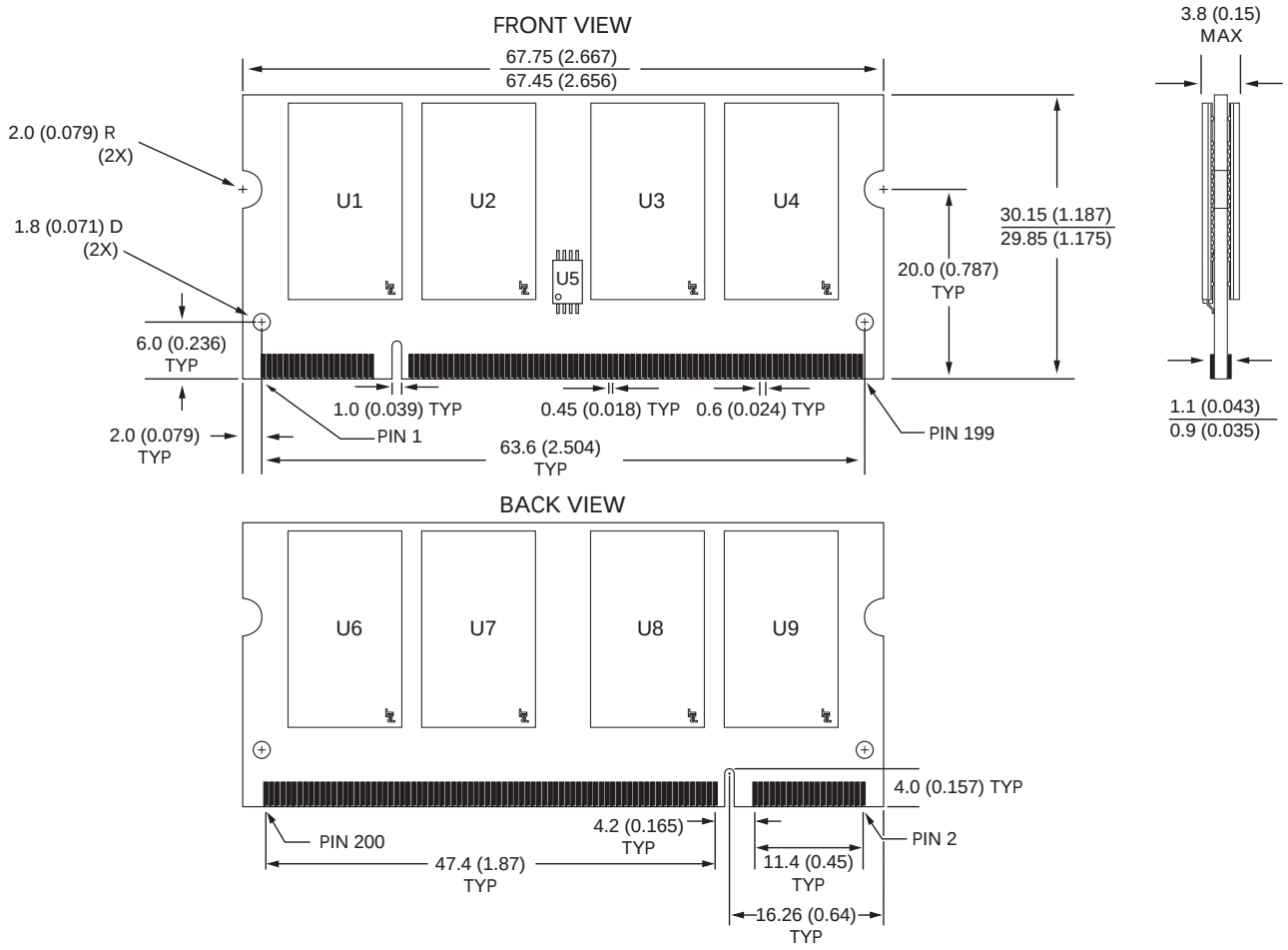
Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 3: 200-pin DDR2 SODIMM Module Dimensions



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

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