S-8206A Series

BATTERY PROTECTION IC FOR 1-CELL PACK (SECONDARY PROTECTION)

The S-8206A Series is used for secondary protection of lithium-ion / lithium polymer rechargeable batteries, and incorporates a high-accuracy voltage detection circuit and a delay circuit.

■ Features

- High-accuracy voltage detection circuit
  - Overcharge detection voltage: 3.500 V to 5.000 V (5 mV step) Accuracy ±20 mV
  - Overcharge release voltage: 3.100 V to 4.950 V*1 Accuracy ±50 mV
- Detection delay time is generated only by an internal circuit (external capacitors are unnecessary).
- Output logic is selectable: Active "H", active "L"
- Output form is selectable: CMOS output, Nch open-drain output
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  - During operation: 1.5 μA typ., 3.0 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected from a range of 0.05 V to 0.4 V in 50 mV step.)

■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Packages

- SNT-6A
- HSNT-6 (1212)

■ Block Diagram

1. CMOS output, active "H"

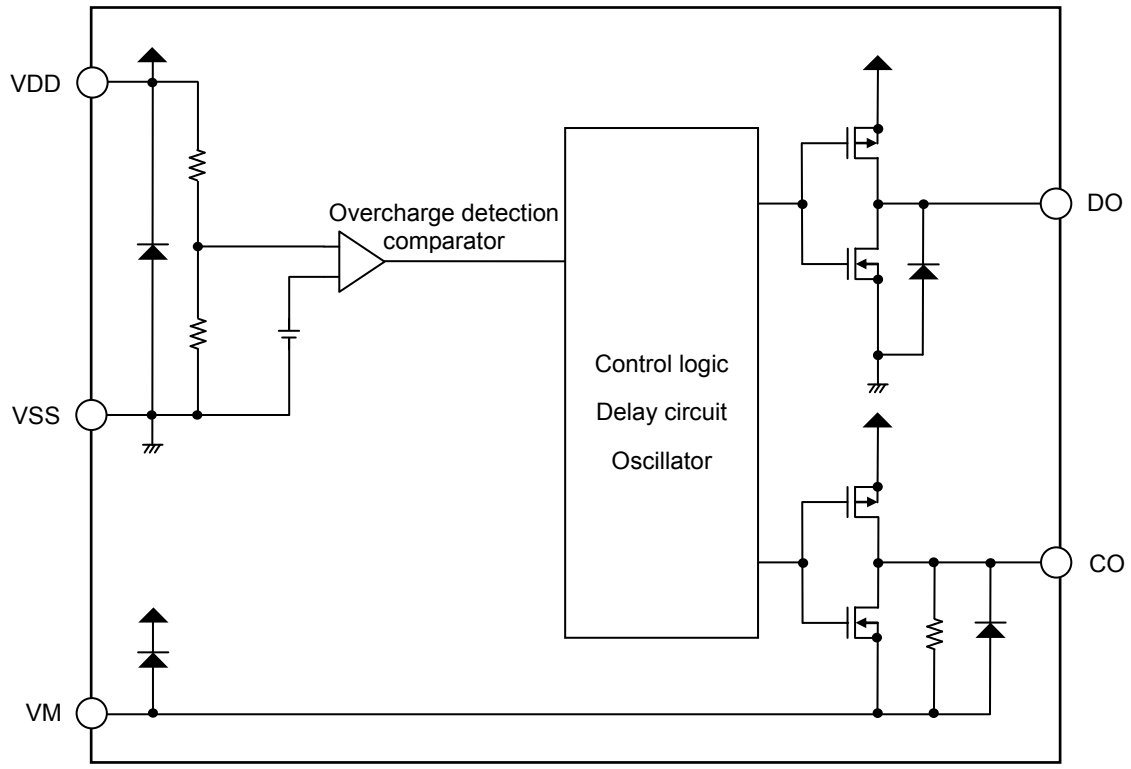


Figure 1

2. CMOS output, active "L"

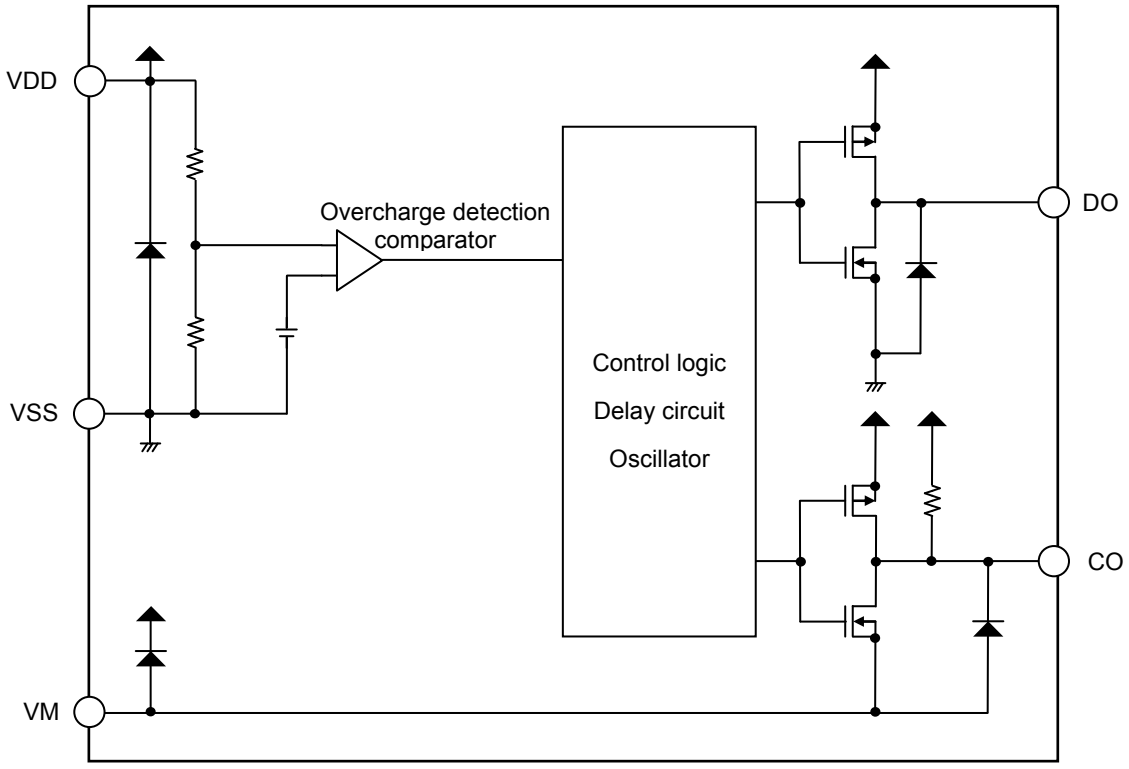


Figure 2

3. Nch open-drain output

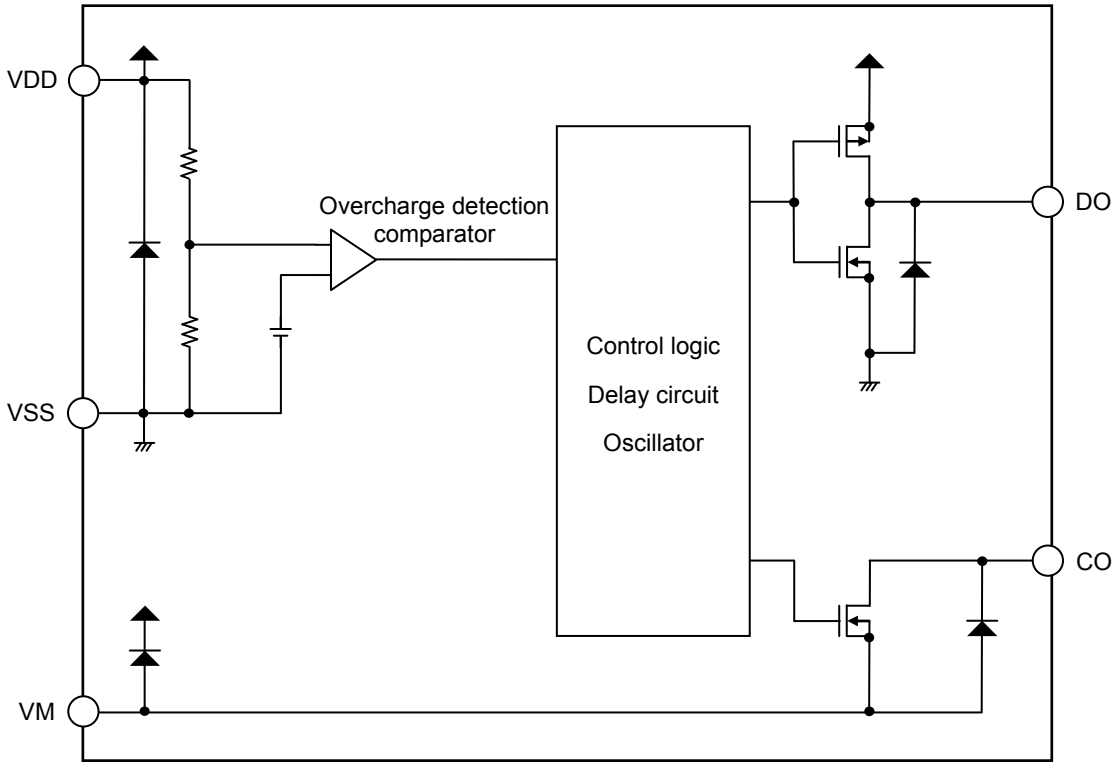


Figure 3

■ Product Name Structure

1. Product name

S-8206A xx - xxxx U

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications*1
I6T1: SNT-6A, Tape
A6T2: HSNT-6 (1212), Tape

Serial code*2
Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD
HSNT-6 (1212)	PM006-A-P-SD	PM006-A-C-SD	PM006-A-R-SD	PM006-A-L-SD

3. Product name list

3. 1 SNT-6A

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overcharge Detection Delay Time*1 [t_{CU}]	Output Logic*2	Output Form*3
S-8206AAA-I6T1U	4.500 V	4.150 V	2 s	Active "H"	CMOS output
S-8206AAB-I6T1U	4.550 V	4.200 V	2 s	Active "H"	CMOS output
S-8206AAC-I6T1U	4.150 V	4.000 V	2 s	Active "L"	CMOS output
S-8206AAD-I6T1U	4.250 V	4.100 V	2 s	Active "L"	CMOS output
S-8206AAE-I6T1U	4.150 V	4.000 V	2 s	Active "H"	Nch open-drain output
S-8206AAF-I6T1U	4.250 V	4.100 V	2 s	Active "H"	Nch open-drain output
S-8206AAG-I6T1U	4.450 V	4.150 V	2 s	Active "H"	CMOS output
S-8206AAH-I6T1U	4.400 V	4.100 V	2 s	Active "H"	CMOS output
S-8206AAI-I6T1U	4.350 V	4.050 V	2 s	Active "H"	CMOS output

***1.** Overcharge detection delay time 1 s / 2 s / 4 s is selectable.
***2.** Output logic active "H" / active "L" is selectable.
***3.** Output form CMOS output / Nch open-drain output is selectable.

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

3. 2 HSNT-6 (1212)

Table 3

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overcharge Detection Delay Time*1 [t_{CU}]	Output Logic*2	Output Form*3
S-8206AAA-A6T2U	4.500 V	4.150 V	2 s	Active "H"	CMOS output
S-8206AAB-A6T2U	4.550 V	4.200 V	2 s	Active "H"	CMOS output

***1.** Overcharge detection delay time 1 s / 2 s / 4 s is selectable.
***2.** Output logic active "H" / active "L" is selectable.
***3.** Output form CMOS output / Nch open-drain output is selectable.

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

■ Pin Configurations

1. SNT-6A

Top view

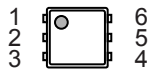


Figure 4

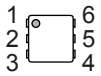
Table 4

Pin No.	Symbol	Description
1	NC*1	No connection
2	CO	Connection pin of charge control FET gate (CMOS output)
3	DO	Input pin for test signal
4	VSS	Input pin for negative power supply
5	VDD	Input pin for positive power supply
6	VM	Negative power supply pin for CO pin

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD pin or VSS pin.

2. HSNT-6 (1212)

Top view



Bottom view

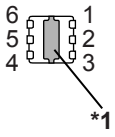


Figure 5

Table 5

Pin No.	Symbol	Description
1	NC*2	No connection
2	CO	Connection pin of charge control FET gate (CMOS output)
3	DO	Input pin for test signal
4	VSS	Input pin for negative power supply
5	VDD	Input pin for positive power supply
6	VM	Negative power supply pin for CO pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential open or VDD.
However, do not use it as the function of electrode.

***2.** The NC pin is electrically open.
The NC pin can be connected to VDD pin or VSS pin.

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item		Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin		V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 6	V
VM pin input voltage		V_{VM}	VM	V_{DD} − 28 to V_{DD} + 0.3	V
DO pin input voltage		V_{DO}	DO	V_{SS} − 0.3 to V_{DD} + 0.3	V
CO pin output voltage	CMOS output	V_{CO}	CO	V_{VM} − 0.3 to V_{DD} + 0.3	V
	Nch open-drain output			V_{VM} − 0.3 to V_{VM} + 28	V
Power dissipation	SNT-6A	P_D	−	400[*1]	mW
	HSNT-6 (1212)		−	480[*1]	mW
Operation ambient temperature		T_{opr}	−	−40 to +85	°C
Storage temperature		T_{stg}	−	−55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

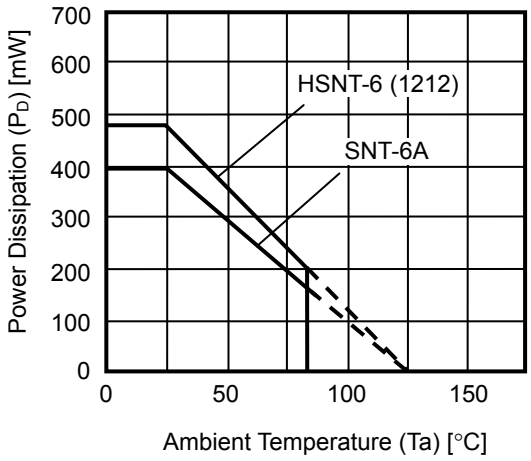


Figure 6 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Ta = +25°C

Table 7

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	$V_{CU}-0.020$	V_{CU}	$V_{CU}+0.020$	V	1
		Ta = –10°C to +60°C*1	$V_{CU}-0.025$	V_{CU}	$V_{CU}+0.025$	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	$V_{CL}-0.050$	V_{CL}	$V_{CL}+0.050$	V	1
		$V_{CL} = V_{CU}$	$V_{CL}-0.025$	V_{CL}	$V_{CL}+0.020$	V	1
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	–	1.5	–	6.0	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	1.5	3.0	μA	2
Output Resistance							
CO pin resistance "H" 1	R_{COH1}	CMOS output	5	10	20	kΩ	3
CO pin resistance "L" 1	R_{COL1}	–	5	10	20	kΩ	3
DO pin resistance "H"	R_{DOH}	–	5	10	20	kΩ	3
DO pin resistance "L"	R_{DOL}	–	5	10	20	kΩ	3
CO pin resistance "H" 2	R_{COH2}	CMOS output, active "L"	1	4	–	MΩ	3
CO pin resistance "L" 2	R_{COL2}	CMOS output, active "H"	1	4	–	MΩ	3
Output Current							
CO pin leakage current "L"	I_{COLL}	Nch open-drain output	–	–	0.1	μA	3
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.7$	t_{CU}	$t_{CU} \times 1.3$	–	4

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution 1. Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM}.
2. Set SW to ON and OFF in Nch open-drain output and CMOS output, respectively.

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

1. 1 Active "H"

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is gradually increased from the starting condition of V1 = 3.4 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL}.

1. 2 Active "L"

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = 3.4 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL}.

2. Current consumption during operation (Test circuit 2)

The current consumption during operation (I_{OPE}) is the current that flows through VDD pin (I_{DD}) under the set condition of V1 = 3.4 V.

3. CO pin resistance "H" 1 (CMOS output) (Test circuit 3)

3. 1 Active "H"

The CO pin resistance "H" 1 (R_{COH1}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 5.1 V, V2 = 4.7 V.

3. 2 Active "L"

The CO pin resistance "H" 1 (R_{COH1}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 3.0 V.

4. CO pin resistance "L" 1 (Test circuit 3)

4. 1 Active "H"

The CO pin resistance "L" 1 (R_{COL1}) is the resistance between VM pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 0.4 V.

4. 2 Active "L"

The CO pin resistance "L" 1 (R_{COL1}) is the resistance between VM pin and CO pin under the set conditions of V1 = 5.1 V, V2 = 0.4 V.

5. DO pin resistance "H" (Test circuit 3)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = 3.4 V, V3 = 3.0 V.

6. DO pin resistance "L" (Test circuit 3)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = 1.8 V, V3 = 0.4 V.

7. CO pin resistance "H" 2 (CMOS output, active "L") (Test circuit 3)

The CO pin resistance "H" 2 (R_{COH2}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 5.1 V, V2 = 0 V.

8. CO pin resistance "L" 2 (CMOS output, active "H") (Test circuit 3)

The CO pin resistance "L" 2 (R_{COL2}) is the resistance between VM pin and CO pin under the set conditions of V1 = 5.1 V, V2 = 5.1 V.

9. CO pin leakage current "L" (Nch open-drain output) (Test circuit 3)

9. 1 Active "H"

The CO pin leakage current "L" (I_{COLL}) is the current that flows through CO pin (I_{CO}) under the set conditions of V1 = 5.1 V, V2 = 28 V.

9. 2 Active "L"

The CO pin leakage current "L" (I_{COLL}) is the current that flows through CO pin (I_{CO}) under the set conditions of V1 = 3.4 V, V2 = 28 V.

10. Overcharge detection delay time (Test circuit 4)

10. 1 Active "H"

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "H" just after the voltage V1 increases and exceeds V_{CU} under the set condition of V1 = 3.4 V.

10. 2 Active "L"

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "L" just after the voltage V1 increases and exceeds V_{CU} under the set condition of V1 = 3.4 V.

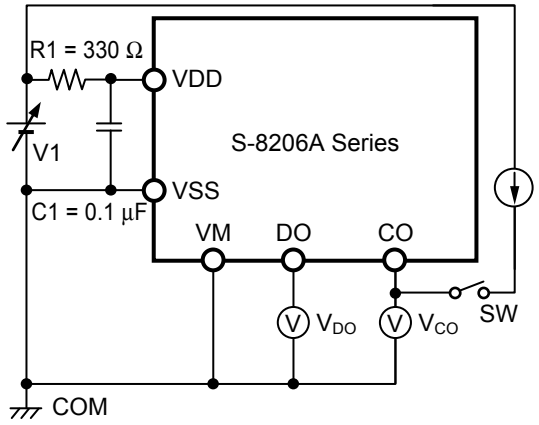


Figure 7 Test Circuit 1

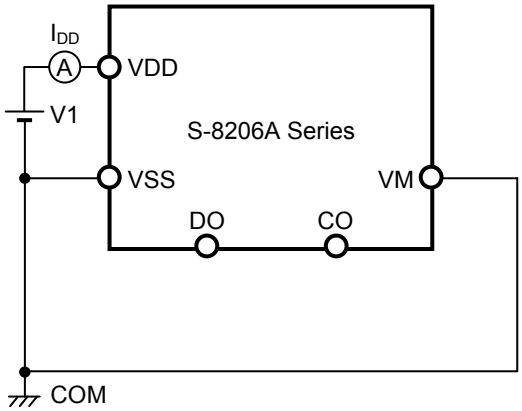


Figure 8 Test Circuit 2

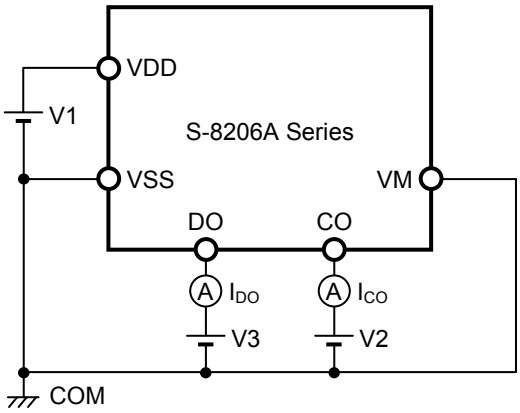


Figure 9 Test Circuit 3

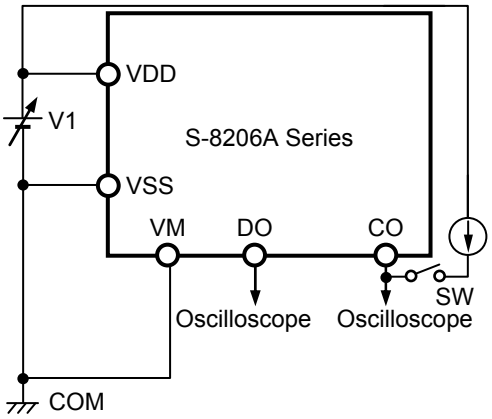


Figure 10 Test Circuit 4

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Example**".

1. Overcharge detection status

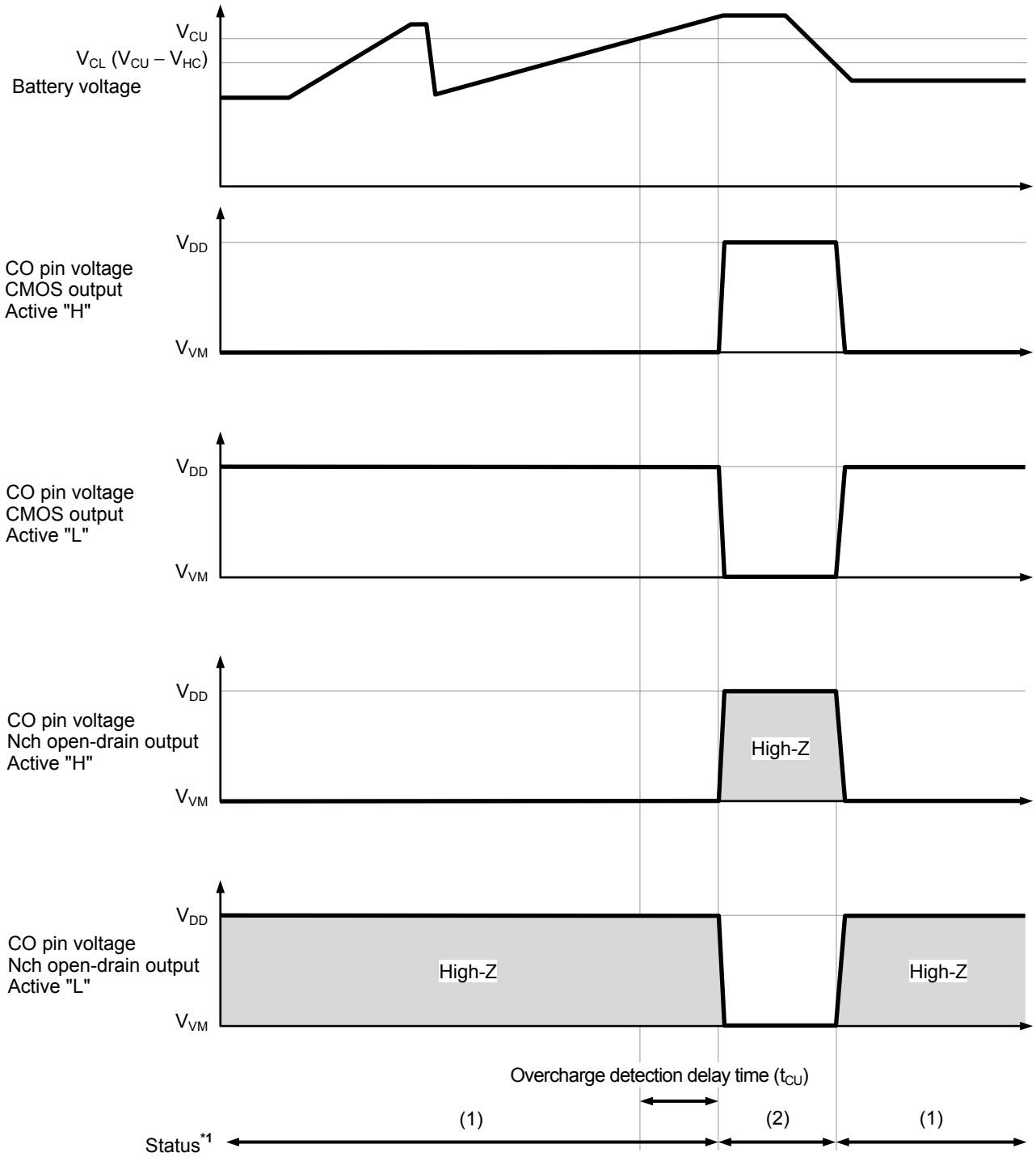
The S-8206A Series monitors the voltage of the battery connected between VDD pin and VSS pin to detect overcharge. When the battery voltage exceeds the overcharge detection voltage (V_{CU}) during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, the S-8206A Series outputs overcharge detection signal from the CO pin. This condition is called overcharge status. Connecting FET to the CO pin provides charge control and a second protection.

2. Test mode

t_{CU} can be shortened by forcibly setting the DO pin to V_{SS} level from external. When the DO pin is forcibly set to V_{SS} level from external, t_{CU} will be shortened to approximately 1/64.

■ Timing Charts

1. Overcharge detection



***1.** (1): Normal status
(2): Overcharge status

Figure 11

■ Battery Protection IC Connection Example

Figure 12 shows the connection example when CMOS output, active "H" product is used.

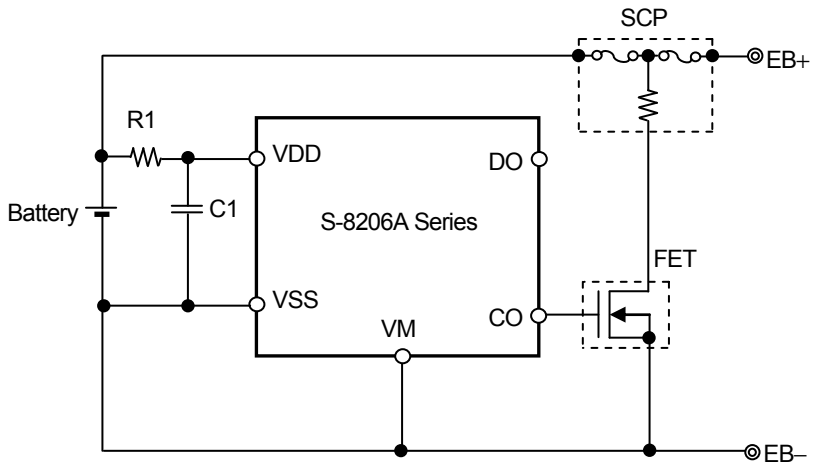


Figure 12

Table 8 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
FET	N-channel MOS FET	Charge control	–	–	–	–
R1	Resistor	ESD protection, For power fluctuation	150 Ω	330 Ω	1 kΩ	–
C1	Capacitor	For power fluctuation	0.068 μF	0.1 μF	1.0 μF	–

Caution 1. The above constants may be changed without notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

[For SCP, contact]
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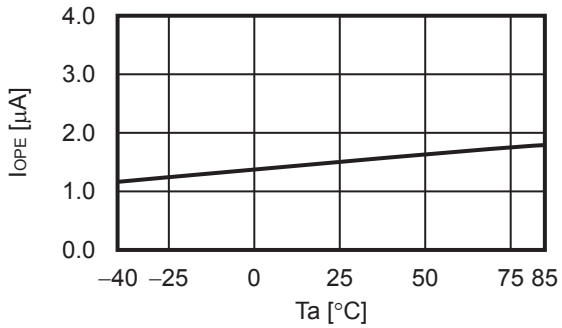
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII Semiconductor Corporation claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

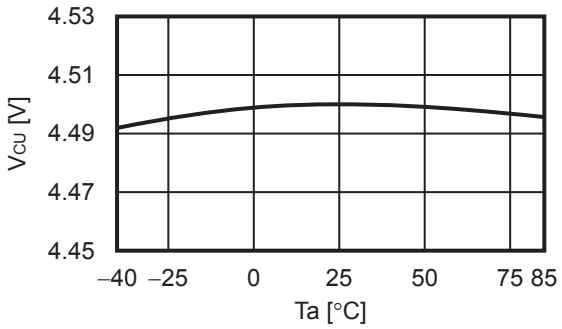
1. Current consumption

1. 1 I_{OPE} vs. Ta

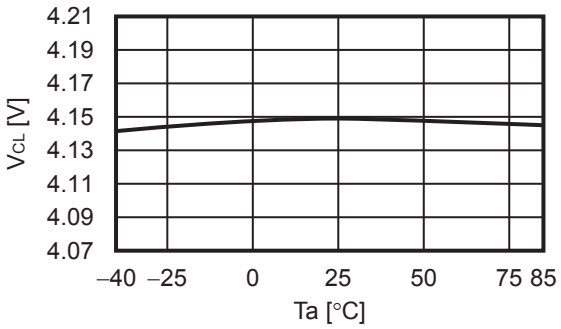


2. Detection voltage

2. 1 V_{CU} vs. Ta

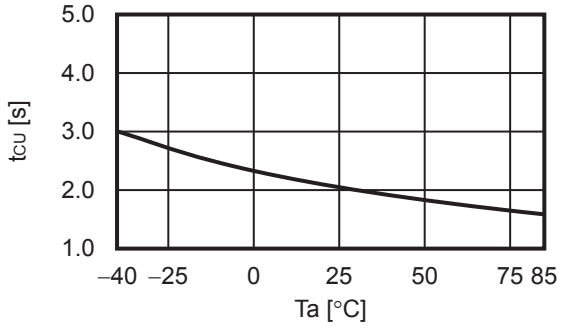


2. 2 V_{CL} vs. Ta



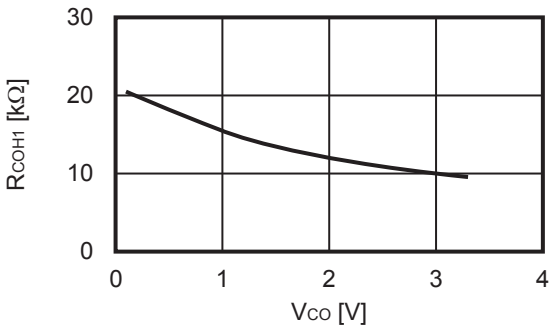
3. Delay time

3. 1 t_{CU} vs. Ta

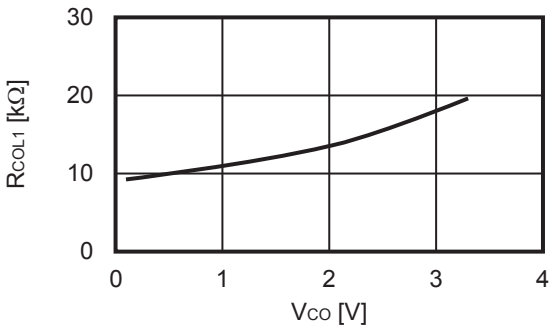


4. Output resistance

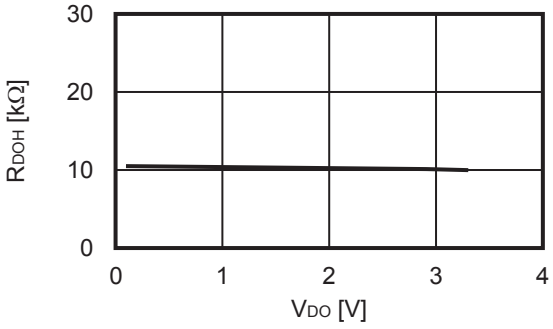
4. 1 R_{COH1} vs. V_{CO}



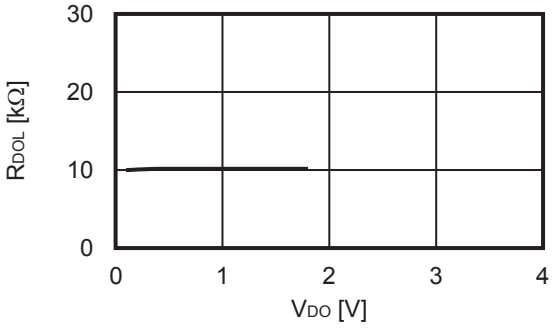
4. 2 R_{COL1} vs. V_{CO}



4. 3 R_{DOH} vs. V_{DO}



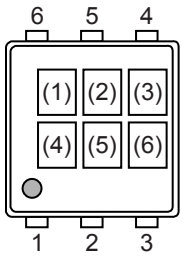
4. 4 R_{DOL} vs. V_{DO}



■ Marking Specifications

1. SNT-6A

Top view



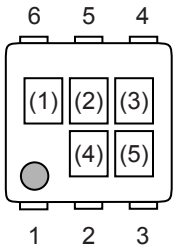
(1) to (3): Product code (refer to **Product name vs. Product code**)
(4) to (6): Lot number

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-8206AAA-I6T1U	J	N	A
S-8206AAB-I6T1U	J	N	B
S-8206AAC-I6T1U	J	N	C
S-8206AAD-I6T1U	J	N	D
S-8206AAE-I6T1U	J	N	E
S-8206AAF-I6T1U	J	N	F
S-8206AAG-I6T1U	J	N	G
S-8206AAH-I6T1U	J	N	H
S-8206AAI-I6T1U	J	N	I

2. HSNT-6 (1212)

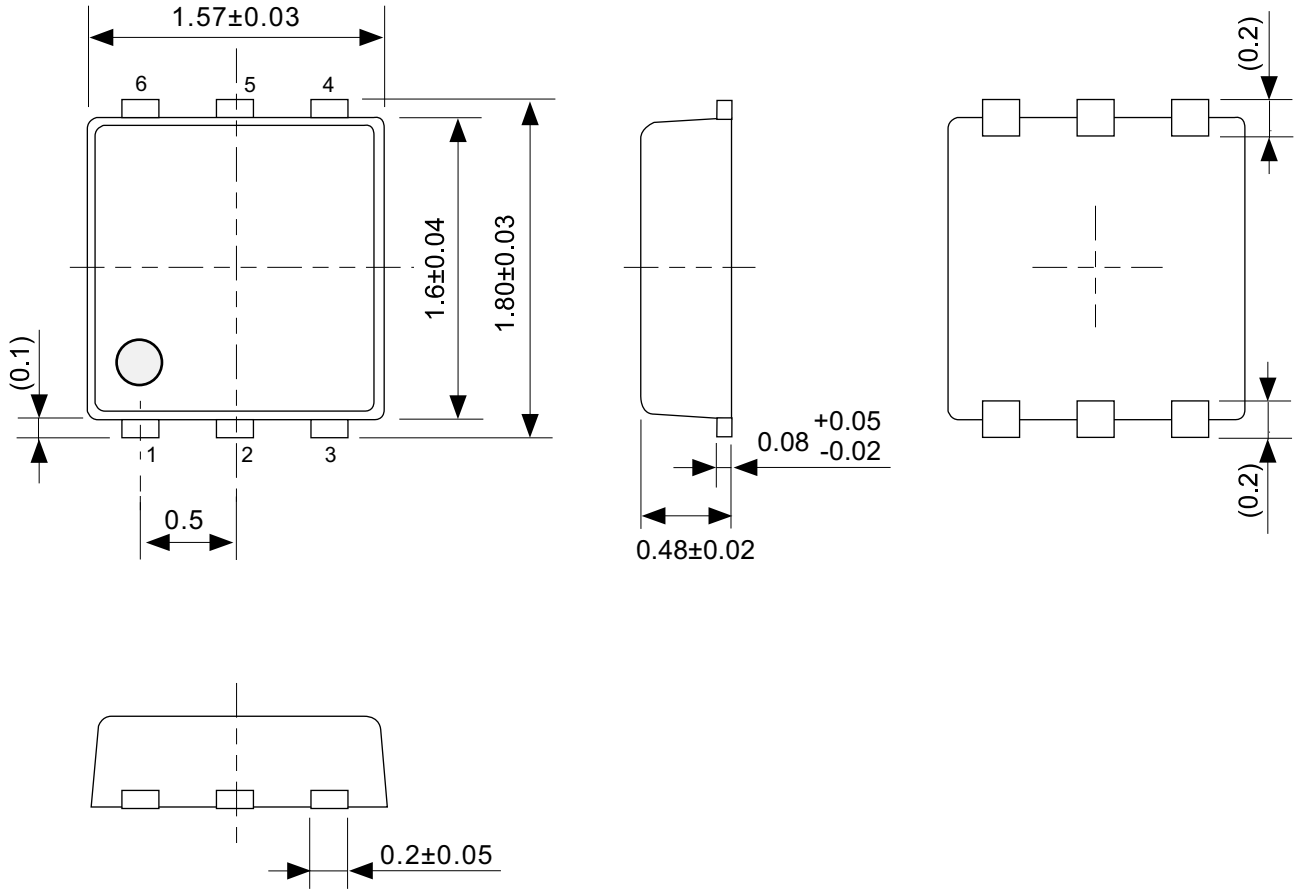
Top view



(1) to (3): Product code (refer to **Product name vs. Product code**)
(4), (5): Lot number

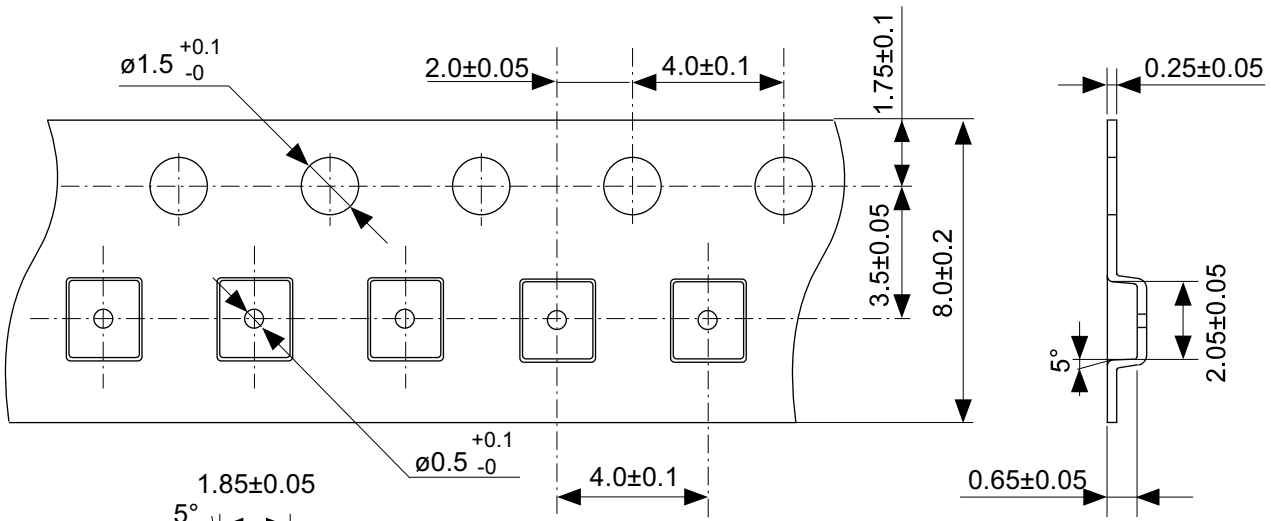
Product name vs. Product code

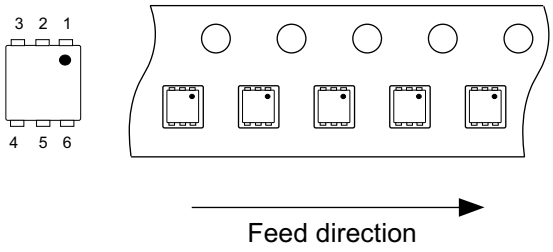
Product Name	Product Code		
	(1)	(2)	(3)
S-8206AAA-A6T2U	J	N	A
S-8206AAB-A6T2U	J	N	B



No. PG006-A-P-SD-2.1

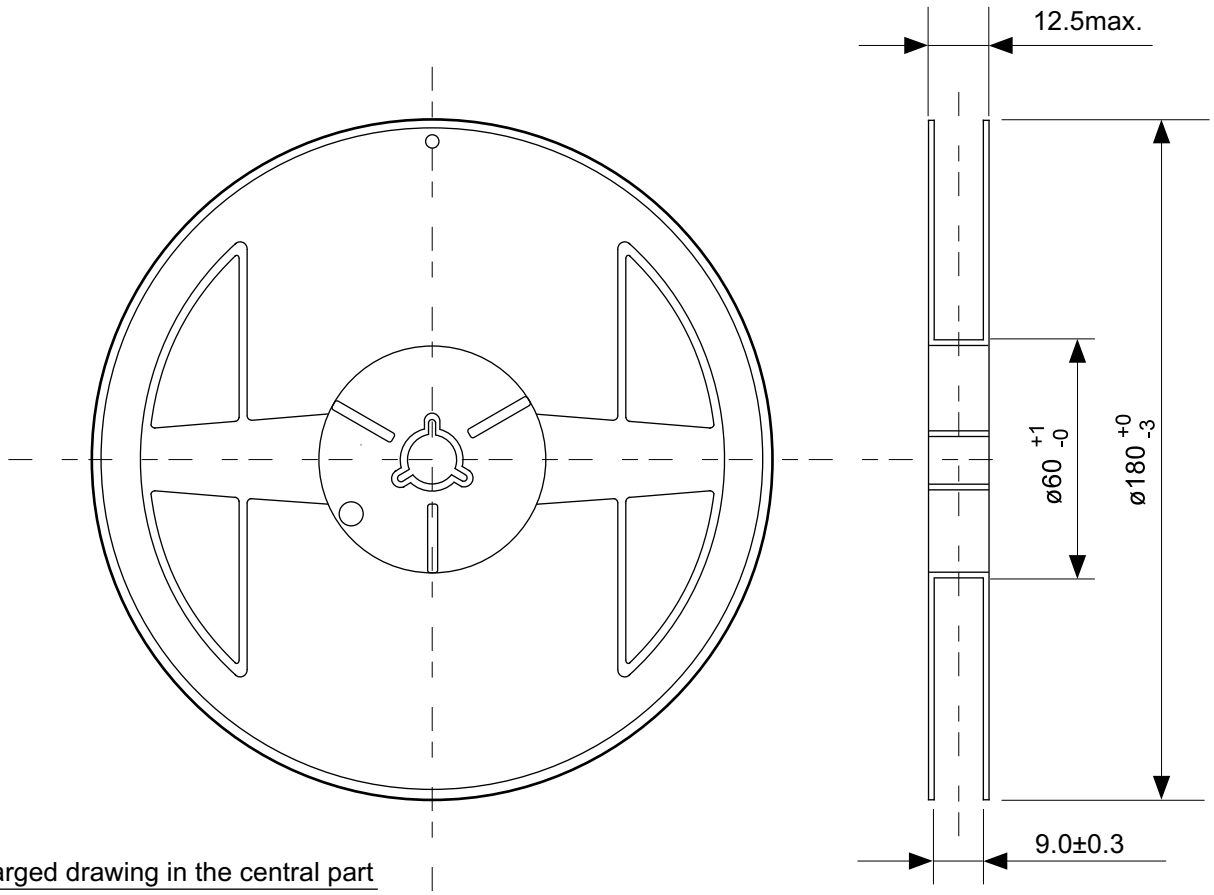
TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm
SII Semiconductor Corporation	



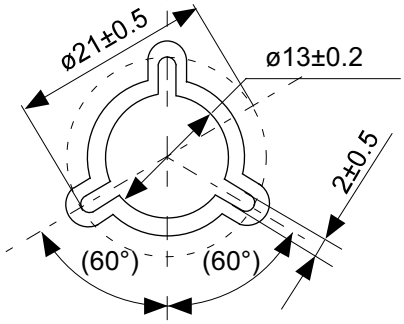


No. PG006-A-C-SD-1.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-1.0
ANGLE	
UNIT	mm
SII Semiconductor Corporation	

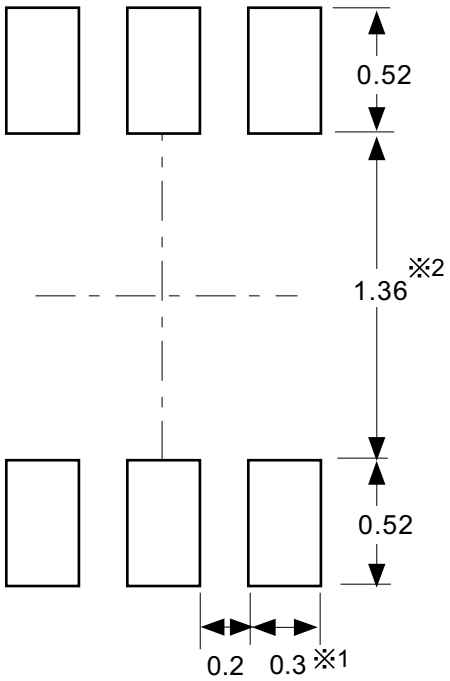


Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
SII Semiconductor Corporation			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝**SNT**パッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

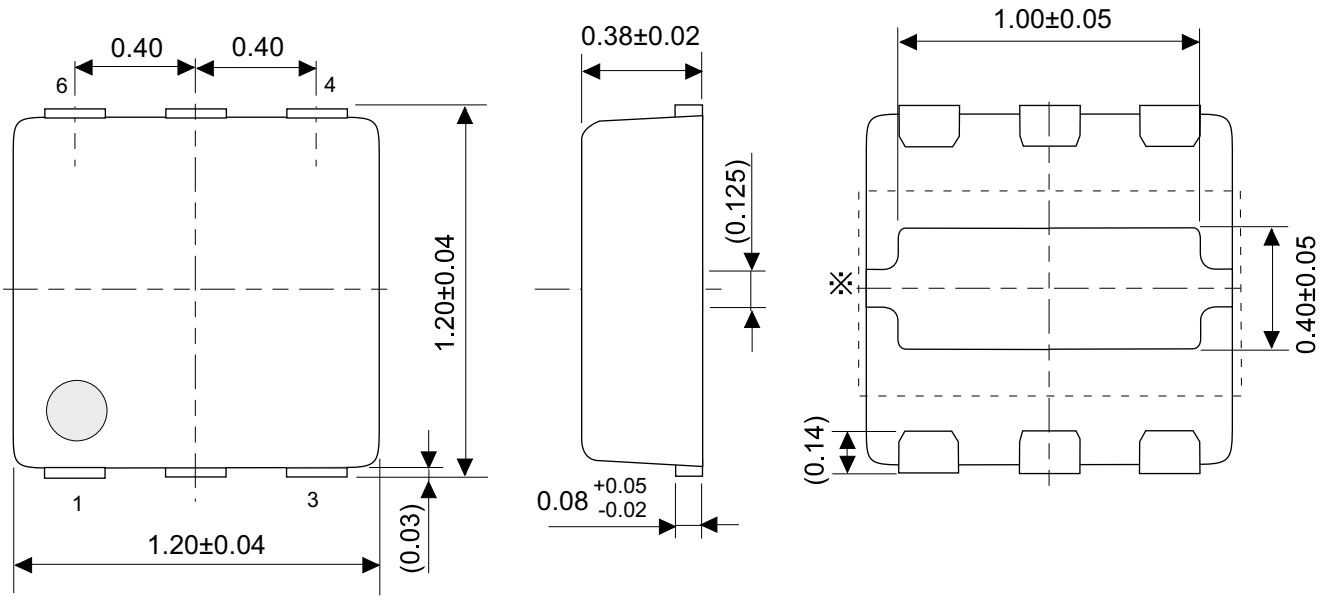
Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

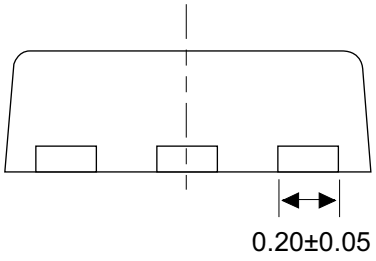
※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm
SII Semiconductor Corporation	

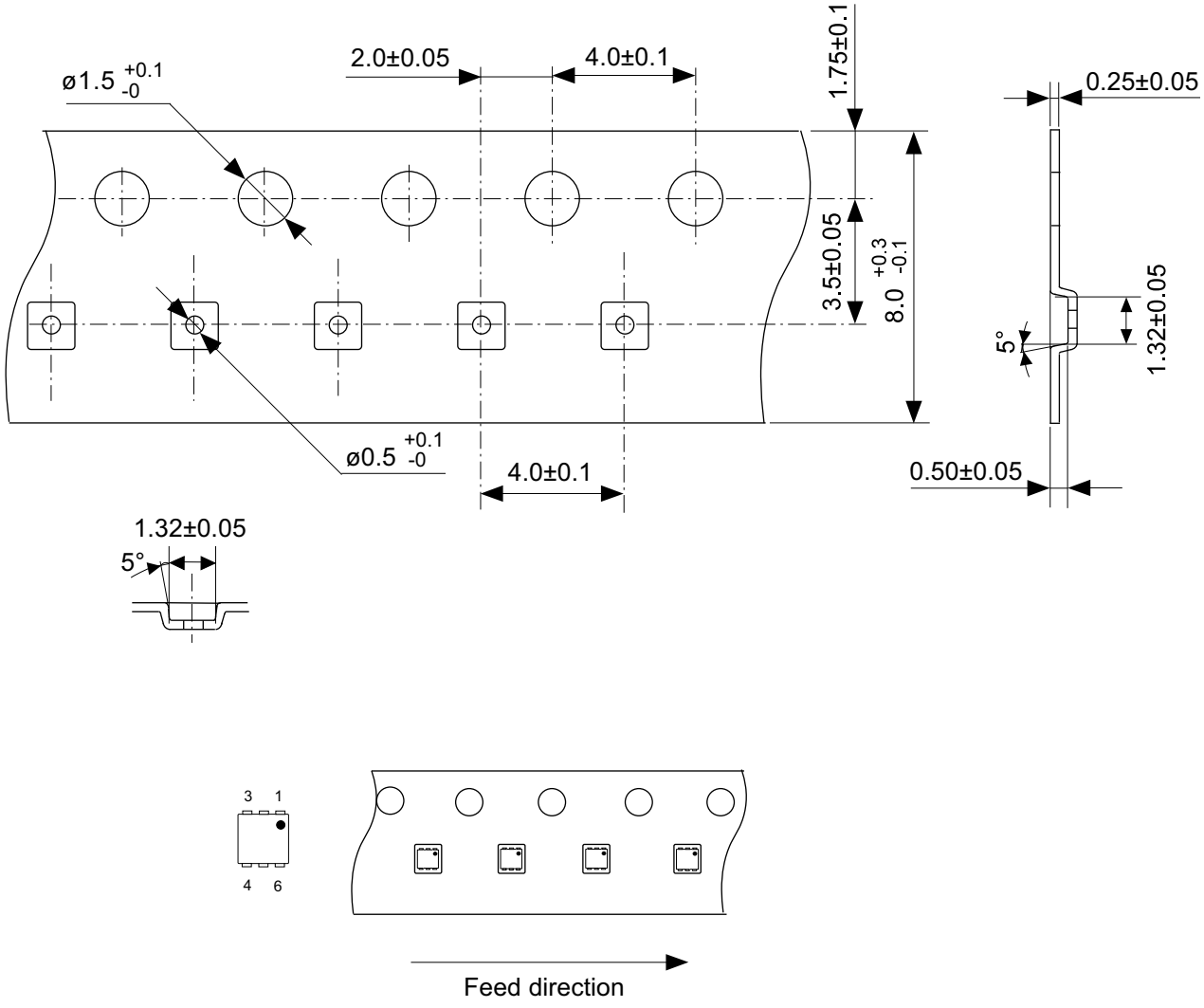




※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

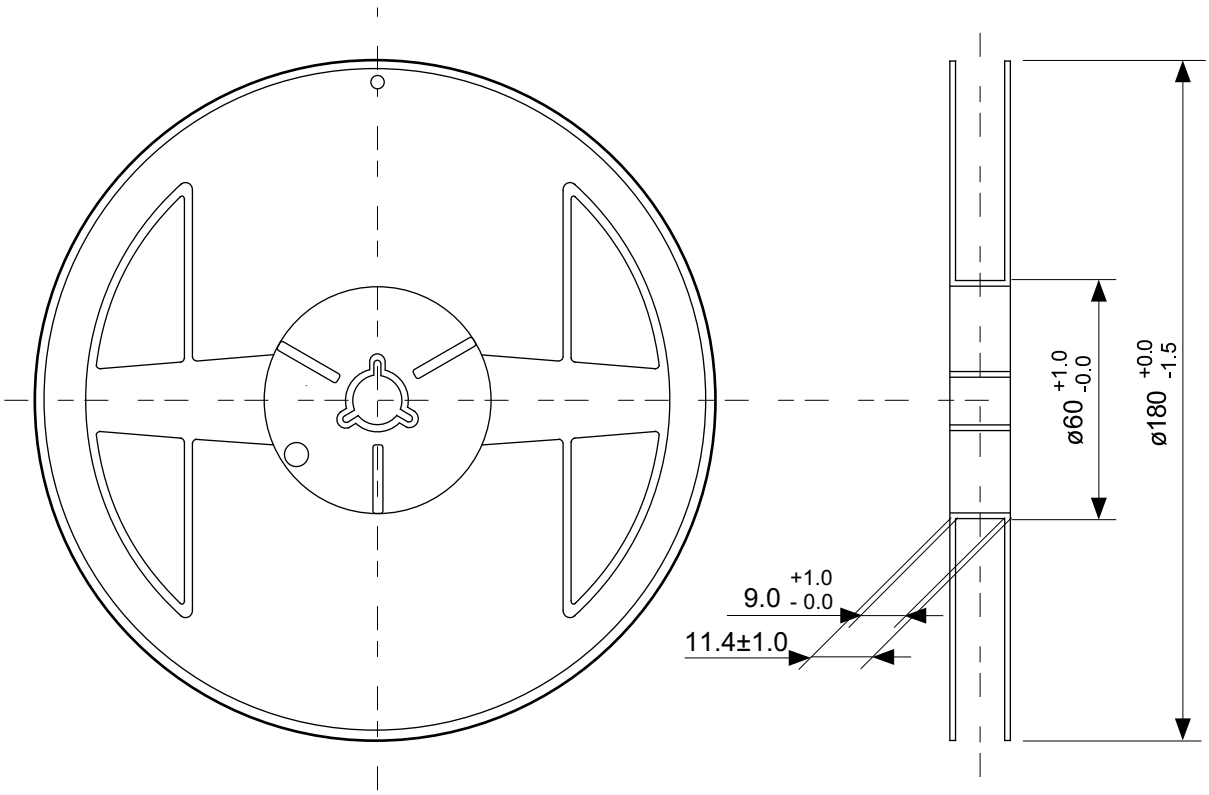
No. PM006-A-P-SD-1.1

TITLE	HSNT-6-B-PKG Dimensions
No.	PM006-A-P-SD-1.1
ANGLE	
UNIT	mm
SII Semiconductor Corporation	

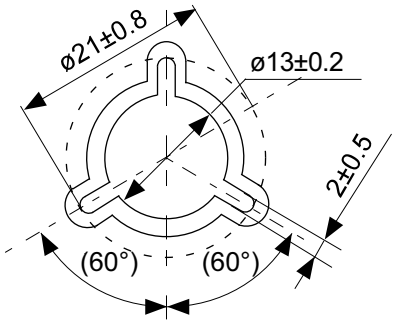


No. PM006-A-C-SD-1.0

TITLE	HSNT-6-B-Carrier Tape
No.	PM006-A-C-SD-1.0
ANGLE	
UNIT	mm
SII Semiconductor Corporation	



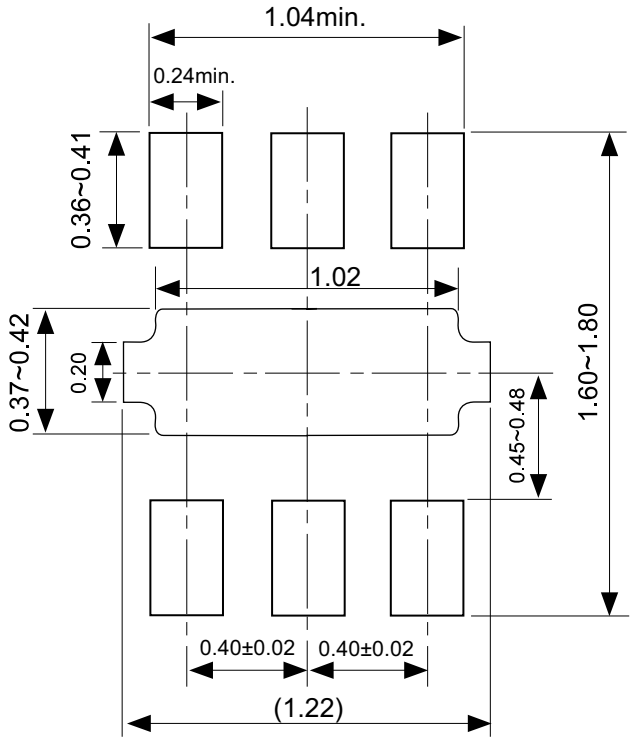
Enlarged drawing in the central part



No. PM006-A-R-SD-1.0

TITLE	HSNT-6-B-Reel		
No.	PM006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
SII Semiconductor Corporation			

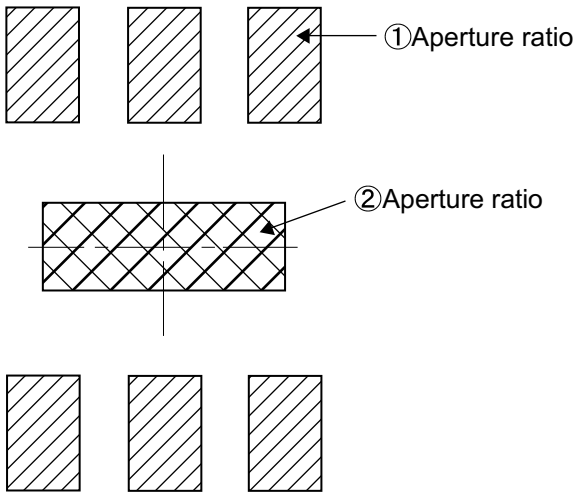
Land Pattern



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意 放熱性を確保する為に、PKGの裏面放熱板(ヒートシンク)を基板に半田付けする事を推奨いたします。

Metal Mask Pattern



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is 40%.
③ Mask thickness: t0.10mm to 0.12 mm

注意 ①リード実装部のマスク開口率は100%です。
②放熱板実装のマスク開口率は40%です。
③マスク厚み：t0.10mm ~ 0.12 mm

No. PM006-A-L-SD-2.0

TITLE	HSNT-6-B -Land Recommendation
No.	PM006-A-L-SD-2.0
ANGLE	
UNIT	mm

SII Semiconductor Corporation

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