



3.3V, 1.5GHz $\div 1/\div 2$ DIFFERENTIAL LVECL/LVPECL PROGRAMMABLE CLOCK GENERATOR AND 1:15 FANOUT BUFFER

Precision Edge[®]
SY100E222L

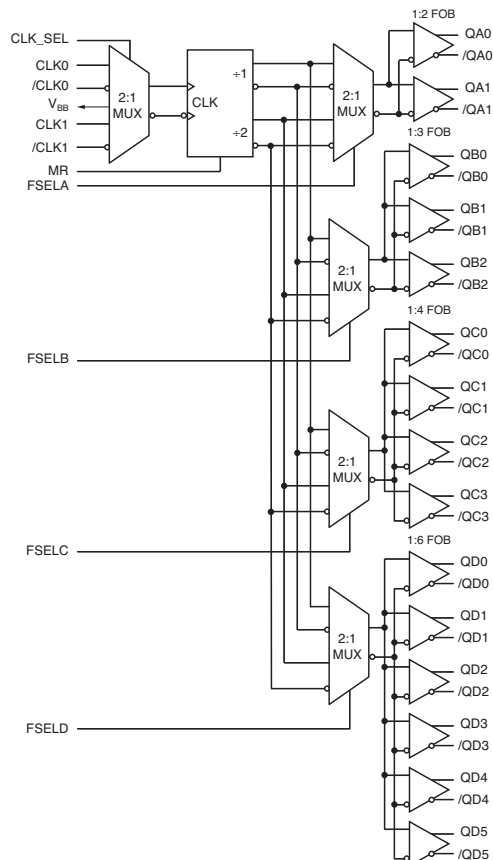
FEATURES

- Four programmable output banks and 15 total LVPECL-compatible differential outputs
- Pin-compatible, plug-in replacement to MC100LVE222FA
- f_{MAX} clock = 1.5GHz
- 50ps output-to-output skew
- Four output banks with independent $\div 1, \div 2$ frequency control
- 100k compatible I/O
- Power supply 3.3V $\pm 10\%$
- -40°C to $+85^{\circ}\text{C}$ temperature range
- Available in 52-pin LQFP package

APPLICATIONS

- SONET/SDH channel applications
- Fibre Channel multi-channel applications
- Gigabit Ethernet multi-channel applications

FUNCTIONAL BLOCK DIAGRAM



Precision Edge[®]

DESCRIPTION

The SY100E222L is a low-skew, low-jitter device capable of receiving a high-speed LVECL/LVPECL input in either a single-ended or differential configuration. For single-ended configurations, a V_{BB} output reference is supplied by the SY100E222L. A 2:1 input multiplexer selects from two differential input pairs by means of the CLK_SEL input select.

The internal programmable divider for each of the four banks generates a $\div 1$ or $\div 2$ frequency of the selected input. The $\div 1/\div 2$ divider outputs can be asynchronously synchronized with the master reset (MR) input so that the outputs will start out in a known state.

The 15 total outputs are partitioned into four independently selected output banks in a 2/3/4/6 fanout configuration. Each of the four banks can independently select the $\div 1$ or $\div 2$ output frequency by means of the four separate frequency select pins (FSELA-FSEL D) inputs.

The SY100E222L is pin-for-pin compatible with the MC100LVE222FA device.

The SY100E222L is part of a Micrel's Precision Edge[™] product family. For other integrated clock divider plus fanout buffer options, consider Micrel's SY89200 family.

All support documentation can be found on Micrel's web site at www.micrel.com.

CROSS REFERENCE TABLE

| Micrel Part Number | ON Semiconductor |
|--------------------|------------------|
| SY100E222LTI | MC100LVE222FA |
| SY100E222LTI TR | MC100LVE222FAR2 |

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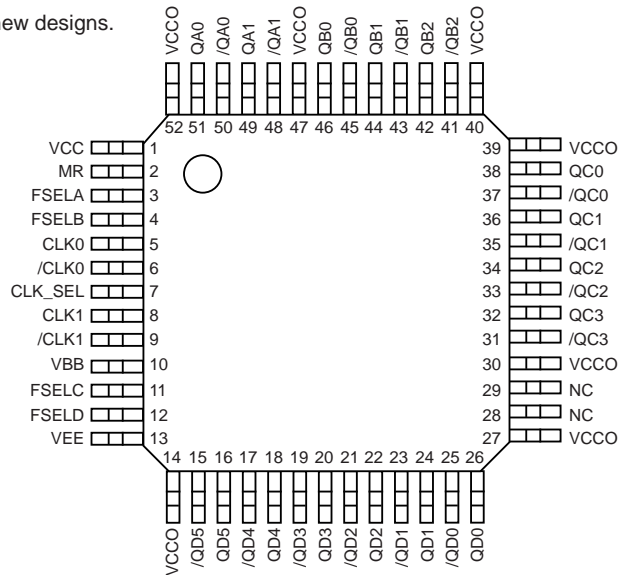
PACKAGE/ORDERING INFORMATION

Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|----------------------------------|--------------|-----------------|--|-------------|
| SY100E222LTI | LQFP-52 | Industrial | SY100E222LTI | Sn-Pb |
| SY100E222LTITR ⁽²⁾ | LQFP-52 | Industrial | SY100E222LTI | Sn-Pb |
| SY100E222LTY ⁽³⁾ | LQFP-52 | Industrial | SY100E222LTY with Pb-Free bar-line indicator | Matte-Sn |
| SY100E222LTYTR ^(2, 3) | LQFP-52 | Industrial | SY100E222LTY with Pb-Free bar-line indicator | Matte-Sn |
| SY100E222LTYTX ^(2, 4) | LQFP-52 | Industrial | SY100E222LTY with Pb-Free bar-line indicator | Matte-Sn |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.
4. EIA specification orientation.



52-Pin LQFP (LQFP-52)

PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|--|-----------------------------|--|
| 2 | MR | 100k ECL compatible: Master reset function resets all outputs to a differential LOW when MR pin goes HIGH. |
| 5, 6, 8, 9 | CLK0, /CLK0, CLK1, /CLK1 | Differential inputs: These input pairs are the differential signal inputs to the device. Inputs accept 100k LVPECL/LVECL levels. |
| 7 | CLK_SEL | 100k ECL compatible input select. LOW = CLK0, HIGH= CLK1. |
| 3 | FSELA | 100k ECL compatible bank A output select. LOW: QA0-QA1 = +1, HIGH: QA0-QA1 = +2. |
| 4 | FSELB | 100k ECL compatible bank B output select. LOW: QB0-QB2 = +1, HIGH: QB0-QB2 = +2. |
| 11 | FSELC | 100k ECL compatible bank C output select. LOW: QC0-QC3 = +1, HIGH: QC0-QC3 = +2. |
| 12 | FSELD | 100k ECL compatible bank D output select. LOW: QD0-QD5 = +1, HIGH: QD0-QD5 = +2. |
| 51, 49, 50, 48 | QA0 – QA1, /QA0 – /QA1 | Bank A 100k differential output pairs controlled by FSELA. FSELA: LOW, QA = +1, HIGH, QA = +2. |
| 46, 44, 42, 45, 43, 41 | QB0 – QB2, /QB0 – /QB2 | Bank B 100k differential output pairs controlled by FSELB. FSELB: LOW, QB = +1, HIGH, QB = +2. |
| 38, 36, 34, 32, 37, 35, 33, 31 | QC0 – QC3, /QC0 – /QC3 | Bank C 100k differential output pairs controlled by FSELC. FSELC: LOW, QC = +1, HIGH, QC = +2. |
| 26, 24, 22, 20, 18, 16, 25, 23, 21, 19, 17, 15 | QD0 – QD5, /QD0 – /QD5 | Bank D 100k differential output pairs controlled by FSELD. FSELD: LOW, QD = +1, HIGH, QD = +2. |
| 1 | VCC | Positive power supply: Bypass with 0.1μF 0.01μF low ESR capacitors. |
| 14, 27, 30, 39, 40, 47, 52 | VCCO | Positive power supply for output buffers. Bypass with 0.1μF 0.01μF low ESR capacitors. |
| 13 | VEE | Negative power supply. For LVPECL systems, VEE is GND. |
| 10 | VBB | Reference voltage. |
| 28, 29 | NC | No connect: Not internally connected (unused pins). |

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC}) -0.5V to + 4.0V
 Input Voltage (V_{IN}) -0.5V to V_{CC}
 Termination Current⁽³⁾
 Source or sink current on V_{BB} (I_{BB}) ± 0.5 mA
 DC Output Current
 LVPECL Outputs -50mA
 Lead Temperature (soldering, 10 sec.) +265°C
 Storage Temperature (T_S) -65°C to +150°C

DC ELECTRICAL CHARACTERISTICS⁽⁴⁾

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|----------------------|---|-----|-----|-----|-------|
| I_{CC} | Power Supply Current | Max. V_{CC} all inputs and outputs OPEN | | 122 | 139 | mA |

LVPECL DC ELECTRICAL CHARACTERISTICS^(4, 5)

$V_{CC} = +3.3V \pm 0.3V$; $V_{EE} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, typicals are $T_A = 25^\circ C$.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------|--|---------------------------------|-------------|------|------------|--------------------|
| V_{OH} | Output High Voltage | $R_L = 50\Omega$ to $V_{CC}-2V$ | 2215 | 2345 | 2420 | mV |
| V_{OL} | Output Low Voltage | $R_L = 50\Omega$ to $V_{CC}-2V$ | 1470 | 1595 | 1680 | mV |
| V_{IH} | Input High Voltage | | 2135 | | 2420 | mV |
| V_{IL} | Input Low Voltage | | 1490 | | 1825 | mV |
| V_{IHCMR} | Input High Voltage Common Mode Range (Differential) (CLK, /CLK) $V_{PP} < 500mV$ $V_{PP} \geq 500mV$ | Note 6 | 1.3 1.6 | | 2.9 2.9 | V V |
| V_{BB} | Output Reference Voltage | | 1.92 | | 2.04 | V |
| I_{IH} | Input HIGH Current | | | | 150 | μA |
| I_{IL} | Input LOW Current (CLK, CLK_SEL, FSEL, MR) (/CLK) | | 0.5 -300 | | | μA μA |

Notes:

1. Permanent device damage may occur if the ratings in "Absolute Maximum Ratings" section are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. Input and output parameters are for $V_{CC} = 3.3V$. They vary 1:1 with V_{CC} .
6. V_{IHCMR} is defined as the range within which the V_{IH} level may vary with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and then greater than or equal to $V_{PP(min)}$.

LVECL DC ELECTRICAL CHARACTERISTICS⁽⁵⁾

$V_{CC} = 0V$; $V_{EE} = -3.3V \pm 0.3V$; $T_A = -40^\circ C$ to $+85^\circ C$, typicals are $T_A = 25^\circ C$.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------|--|---------------------------------|--------------|-------|--------------|--------------------|
| V_{OH} | Output High Voltage | $R_L = 50\Omega$ to $V_{CC}-2V$ | -1085 | -955 | -880 | mV |
| V_{OL} | Output Low Voltage | $R_L = 50\Omega$ to $V_{CC}-2V$ | -1830 | -1705 | -1620 | mV |
| V_{IH} | Input High Voltage | | -1165 | | -880 | mV |
| V_{IL} | Input Low Voltage | | -1810 | | -1475 | mV |
| V_{IIHCMR} | Input High Voltage Common Mode Range (Differential) (CLK, /CLK) $V_{PP} < 500mV$ $V_{PP} \geq 500mV$ | Note 6 | -2.0 -1.7 | | -0.4 -0.4 | V V |
| V_{BB} | Output Reference Voltage | | -1.38 | | -1.26 | V |
| I_{IH} | Input HIGH Current | | | | 150 | μA |
| I_{IL} | Input LOW Current (CLK, CLK_SEL, FSEL, MR) (/CLK) | | 0.5 -300 | | | μA μA |

AC ELECTRICAL CHARACTERISTICS⁽⁷⁾

$V_{CC} = +3.0$ to $+3.6V$ and $V_{EE} = 0V$ or $V_{CC} = 0V$ and $V_{EE} = -3.0$ to $-3.6V$; $T_A = -40^\circ C$ to $+85^\circ C$, typicals are $T_A = 25^\circ C$.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------|----------------------------------|--|----------------------|----------------------|----------------------|-------------------|
| f_{MAX} | Maximum Operating Frequency | | 1.2 | >1.5 | | GHz |
| t_{PD} | Propagation Delay | IN (Differential), Note 8 IN (Single-ended), Note 9 MR | 1040 1090 1000 | 1210 1335 1200 | 1420 1570 1520 | ps ps ps |
| t_{SKEW} | Within-Device Skew | Note 10 | | | 50 | ps |
| | Part-to-Part Skew (Differential) | | | | 300 | ps |
| t_{JITTER} | Random Clock Jitter | | | < 1 | | ps _{RMS} |
| V_{PP} | Differential Input Swing | Note 11 | 400 | | 1000 | mV |
| t_r, t_f | Output Rise/Fall Time (Q, /Q) | (20% to 80%) | 200 | | 600 | ps |

Notes:

- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- V_{IIHCMR} is defined as the range within which the V_{IH} level may vary with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and then greater than or equal to $V_{PP(min)}$.
- High-frequency AC parameters are guaranteed by design and characterization.
- The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
- The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
- The within-device skew is defined as the worst-case difference between any two similar delay paths within a single device.
- $V_{PP(min)}$ is defined as the minimum input differential voltage, which will cause no increase in the propagation delay. The $V_{PP(min)}$ is AC limited for the SY100E222L as a differential input as low as 50 mV will still produce full ECL levels at the output.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

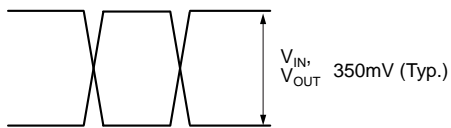


Figure 1a. Single-Ended Voltage Swing

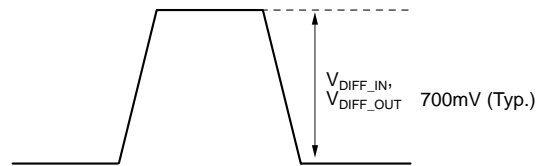
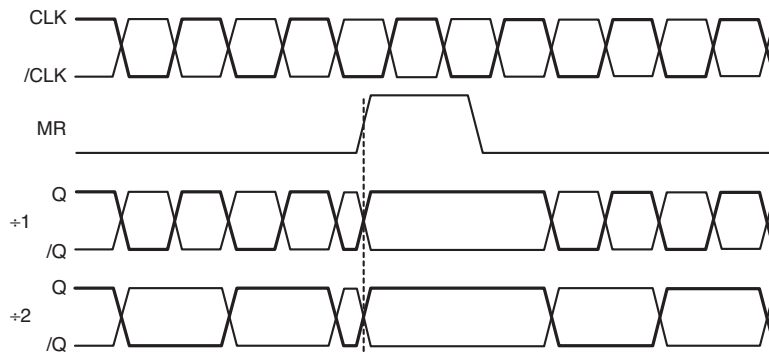


Figure 1b. Differential Voltage Swing

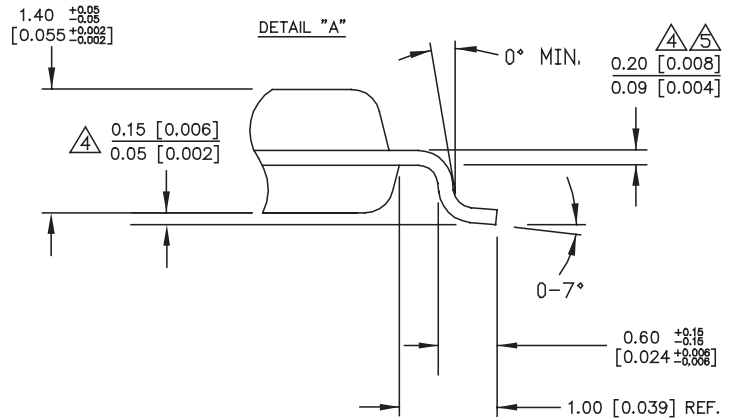
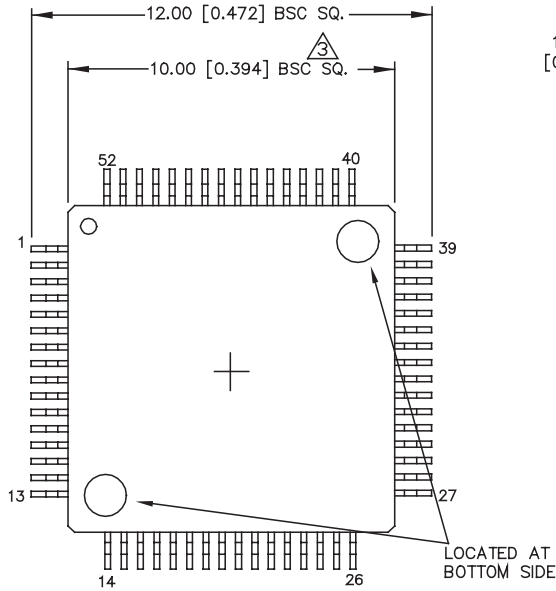
TIMING DIAGRAM



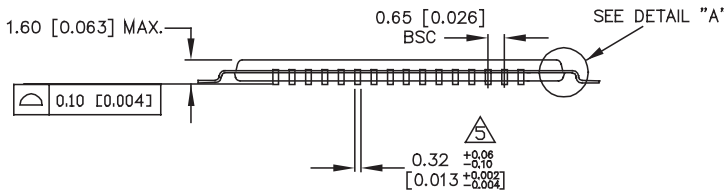
TRUTH TABLE

| MR | CLK_SEL | FSEL | Q |
|----|---------|------|----------|
| 0 | 0 | 0 | CLK0 ÷ 1 |
| 0 | 0 | 1 | CLK0 ÷ 2 |
| 0 | 1 | 0 | CLK1 ÷ 1 |
| 0 | 1 | 1 | CLK1 ÷ 2 |
| 1 | X | X | 0 |

52-PIN LQFP (LQFP-52)



- NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
 2. CONTROLLING DIMENSION: MM.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
 4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: $\frac{\text{MAX}}{\text{MIN}}$
 5. THIS DIMENSION INCLUDES LEAD FINISH.



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